Non-isolated two-inductor boost converter with improved EMI performance

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Abstract — **A new implementation of a non-isolated, two-inductor, two-switch boost converter topology that features a common ground for the source and load is described. The new circuit exhibits a significantly reduced common-mode noise compared to its counterpart that is implemented with separate source and load grounds. The EMI performance of the proposed implementation was experimentally verified on a 540-W prototype designed to operate with a -36-V to -72-V dc input-voltage range.**

1. Introduction

With the rapid growth of the Internet, telecom operators are aggressively adding new equipment to their networks so that they can still use the existing telecom infrastructure to provide Internet services. This new equipment consists primarily of data processing and networking equipment such as servers, routers, and modems. This collocation of data and telecom equipment has brought about the requirement that data processing equipment be powered by the –48-V telecom dc bus [1].

The requirement for server power supplies to operate from both ac line and –48-V dc bus puts a significant burden on the manufacturers of power supplies because of the additional effort and resources necessary to design, manufacture, and handle two versions of a power supply. Furthermore, since the present volume of the dc-input version is relatively small compared to the volume of the ac-input version, the additional engineering effort required for the design of the dc-input version might not pay off unless the dc-input version design is done by leveraging the ac-input version design to the highest extent possible.

To minimize the effort and resources required for the design of a dual-input power supply for computers for networking applications, a maximally leveraged modular design approach seems to be most cost-effective solution for the time being [2]. In this approach, the ac- and dc-input versions of the power supply use different front ends and the same output stage. Specifically, the ac-input version employs a PFC boost-converter front end, whereas the dc-input version uses a dc-dc boost converter.

The proposed modular design does not require any redesign of the output stage since both front ends provide about the same input voltage to the output stage, usually 360-400 V. In addition, by physically separating the front end and the output stage by placing them on two separate printed circuit boards and by providing the necessary interface between the boards through connectors, it is possible to achieve a modular design. Finally, the designs for both the ac and dc boost front ends can be standardized for a number of power levels. With standardized front-end modules, the design effort for the dual-input power supplies can be dramatically reduced.

Since in this modular approach the dc-dc boost converter needs to provide a boost of approximately ten times when the input voltage is at its minimum value of -36 V, at power levels above approximately 400 W the two-inductor boost topology [3]-[6] has been proven to be a good choice. In fact, when implemented with the voltage doubler output and auxiliary transformer as described in [6], the gain of the two-inductor boost dc/dc converter is four times larger than that of the corresponding conventional implementation [3]-[5]. As a result, the implementation in [6] can provide the required high gain with a reasonable value of the duty cycle ($D_{MAX} < 0.65$), which improves the conversion efficiency of the circuit.

However, in the two-inductor boost circuit described in [6], the input dc source and the load (which is a downstream isolated dc-dc converter) do not share the same ground. As a result, the circuit exhibits a relatively high common-mode noise that requires a significant amount of common-mode filter capacitance, which increases the cost and also adversely affects the power density.

In this paper, an implementation of a two-inductor, two-switch boost converter that has the same ground for the input source and load is described. The expected improvement of the common-mode noise performance of the proposed implementation has been experimentally verified on a 540-W prototype designed to operate in a –36-V to –72-V dc input-voltage range.

2. Conventional Two-Inductor Boost Converter

An implementation of the conventional non-isolated two-inductor boost converter with auxiliary transformer ATR described in [6] is shown in Fig. 1. The input side of the circuit consists of two switches

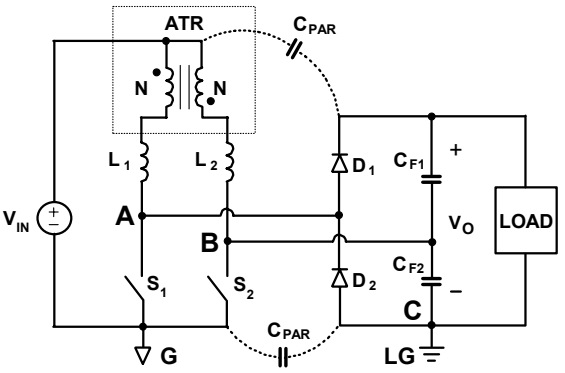

Fig. 1. Schematic diagram of conventional two-inductor boost converter with auxiliary transformer ATR [6].

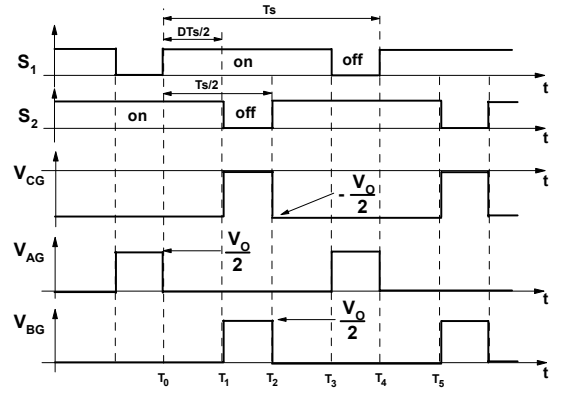

Fig. 2. Key waveforms of conventional two-inductor boost converter.

S_1 and S_2, two boost inductors L_1 and L_2, and auxiliary transformer ATR. To maximize the voltage gain of the converter, the output side of the circuit is configured as a voltage doubler rectifier that consists of boost rectifiers D_1 and D_2 and output filter capacitors C_{F1} and C_{F2} connected across the downstream dc-dc converter (the load). As can be seen from the timing diagrams of the control signals for switches S_1 and S_2 shown in Fig. 2, switches S_1 and S_2 conduct simultaneously, *i.e.*, they operate with overlapping control signals.

It should be noted that in the circuit in Fig. 1, ground G of the input dc source and load ground LG of the load are connected through switches S_1 and S_2. As a result, voltage V_{CG}, which is the difference of the potentials between load ground LG and input source ground G, is pulsating due to the switching action of switches S_1 and S_2, as illustrated in Fig. 2. This pulsating voltage V_{CG} coupled with parasitic capacitances C_{PAR} between the source-side circuit and load-side circuit is a source of severe EMI noise. In high power applications, this parasitic capacitance is relatively high because the load-side circuit of the converter contains large-size components such as capacitors C_{F1} and C_{F2}, rectifiers D_1 and D_2, and the entire primary side of the downstream dc-dc converter with its primary switches mounted on heat sinks.

The peak noise current through the parasitic capacitance CPAR can be estimated from

$$I_{NOISE(PK)} = C_{PAR(TOT)} \cdot \frac{dV_{CG}}{dt}, \qquad (1)$$

where dV_{CG}/dt is the rate of change of pulsating voltage V_{CG} and $C_{PAR(TOT)}$ is the total parasitic capacitance between the source-side circuit and the load-side circuit.

3. Two-Inductor Boost Converter with Common Ground

The proposed implementation of a two-inductor boost converter in which the input source and load have a common ground is shown in Fig. 3. As in the original circuit in Fig. 1, the input side of the circuit consists of two switches S_1 and S_2, two boost inductors L_1 and L_2, and auxiliary transformer ATR, whereas the output side of the circuit, which is configured as a voltage doubler rectifier, consists of boost rectifiers D_1 and D_2, blocking capacitor C_B, and output filter capacitors C_F connected across load R_L.

To facilitate the explanation of the circuit operation, Fig. 4 shows a simplified circuit diagram of the circuit in Fig. 3. In the simplified circuit, auxiliary transformer ATR is modeled as an ideal transformer with turns ratio n_{ATR}=1 by assuming that its magnetizing inductance is high enough that it can be neglected. In addition, it is assumed that blocking capacitor C_B and filter capacitor C_F are large enough that the voltage ripple across them is small compared to their dc voltages. Finally, in this analysis it is also

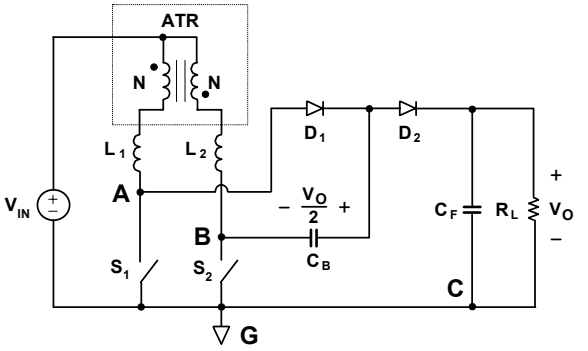

Fig. 3. Proposed two-inductor boost converter with common ground.

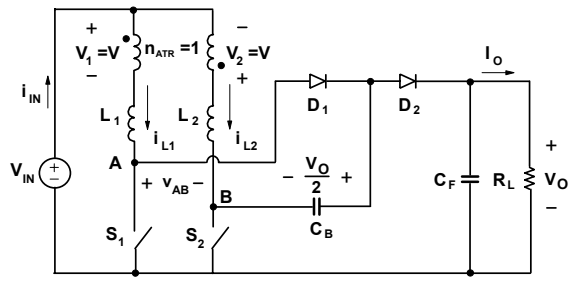

Fig. 4. Simplified circuit model of proposed converter that shows reference directions of currents and voltages.

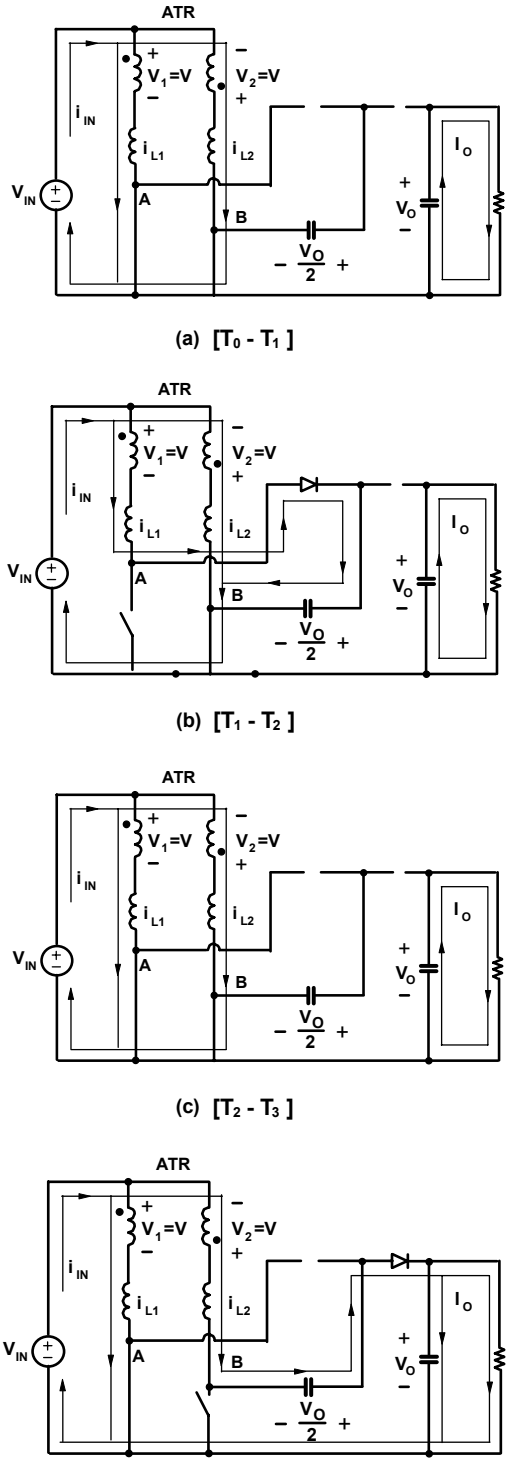

Fig. 5. Topological stages of proposed converter.

assumed that all semiconductor components are ideal, *i.e.*, they represent zero impedances in the on state and infinite impedances in the off state.

To further facilitate the analysis of operation, Fig. 5 shows the topological stages of the circuit in Fig. 3 during a switching cycle, whereas Fig. 6 shows its key

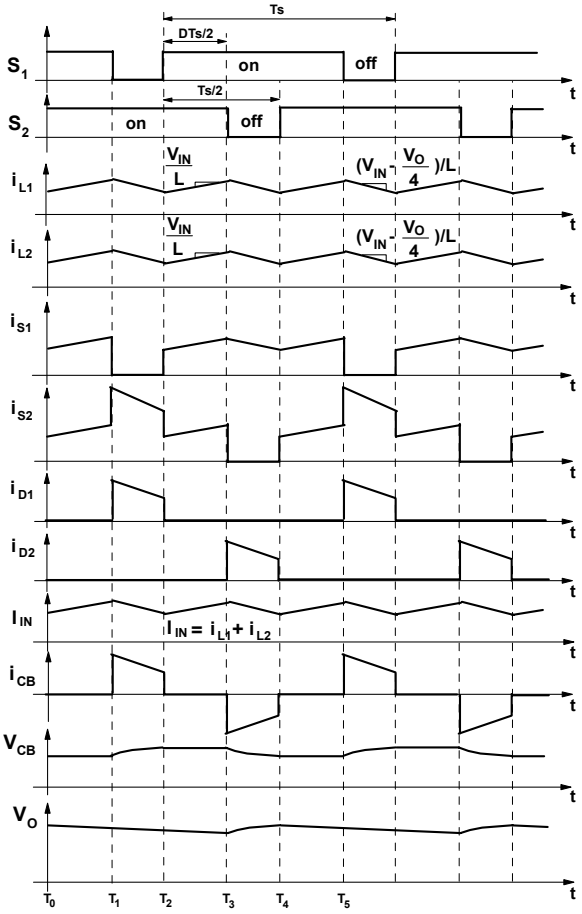

Fig. 6. Key waveforms of the proposed converter.

waveforms. The reference directions of currents and voltages plotted in Fig. 6 are shown in Fig. 4. As can be seen from the timing diagrams of the control signals for switches S_1 and S_2 shown in Fig. 6, switches S_1 and S_2 conduct simultaneously because of their overlapping control signals. The time of the simultaneous conduction, defined from the turn-on moment of one switch until the turn-off moment of the other switch, represents duty cycle D of the converter, as indicated in Fig. 6.

From Fig. 4, since inductors L_1 and L_2 are connected in series with their corresponding transformer windings, inductor currents i_{L1} and i_{L2} must be equal at any given instant if the turns ratio of the transformer is unity, *i.e.*, if n_{ATR}=1. Therefore, when both switches are on, *i.e.*, during the time interval $T_0 - T_1$ in Fig. 6, inductor currents i_{L1} and i_{L2} are increasing at the same rate. The rate of change of i_{L1} and i_{L2} can be calculated from Fig. 5(a), which represents the equivalent circuit diagram of the converter during the time interval $T_0 - T_1$. According to Fig. 5(a),

$$V_{IN} = v_1 + L_1 \frac{di_{L1}}{dt} \tag{2}$$

and

$$v_1 + L_1 \frac{di_{L1}}{dt} = -v_2 + L_2 \frac{di_{L2}}{dt}, \quad (3)$$

therefore the rates of change of i_{L1} and i_{L2} are the same, *i.e.*, $di_{L1}/dt=di_{L2}/dt$ can only be satisfied if

$$v = \frac{L_2 - L_1}{L_2 + L_1} V_{IN}, \quad (4)$$

where $v=v_1=v_2$ because $n_{ATR}=1$. Then, from Eqs. (2) and (3),

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{IN} - v}{L_1} = \frac{V_{IN} + v}{L_2}. \quad (5)$$

If both inductances have the same value $L=L_1=L_2$, it follows that $v=0$ and

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{IN}}{L}, \quad (6)$$

as indicated in Fig. 6.

Since when both switches are on and rectifiers D_1 and D_2 are reverse biased, the output side is decoupled from the input side. As a result, during this stage the load current is supplied from the filter capacitor.

When switch S_1 is turned off at $t=T_1$, inductor current i_{L1} is diverted from switch S_1 to rectifier D_1, as shown in Fig. 5(b), and the energy stored in inductor L_1 starts discharging into blocking capacitor C_B. Since current i_{L1} decreases during this stage and the currents in the windings of the transformer are always equal, current i_{L2} must decrease at the same rate. The rate of the current decrease can be found by observing the equivalent circuit in Fig. 5(b). Therefore,

$$V_{IN} = -v_2 + L_2 \frac{di_{L2}}{dt} = -v + L_2 \frac{di_{L2}}{dt} \quad (7)$$

and

$$V_{AB} = V_{CB} = -L_1 \frac{di_{L1}}{dt} - v_1 - v_2 + L_2 \frac{di_{L2}}{dt} = -2v, \quad (8)$$

where blocking capacitor voltage $V_{CB}=V_O/2$.
From Eqs. (7) and (8) and assuming $L=L_1=L_2$,

$$v = -\frac{V_{CB}}{2} = -\frac{V_O}{4} \quad (9)$$

and

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{1}{L}\left(V_{IN} - \frac{V_O}{4}\right). \quad (10)$$

Since, during the topological stage shown in Fig. 5(b), current i_{L1} charges blocking capacitor C_B, capacitor voltage V_{CB} increases. At the same time, voltage V_O across filter capacitor C_F continues to decrease because capacitor C_F continues to be discharged by the load current, as shown in Fig. 6.

When switch S_1 is turned on again at $t=T_2$, the circuit enters the topological stage shown in Fig. 5(c), which is identical to the topological stage in Fig. 5(a). During this stage both switches are on and both inductor currents i_{L1} and i_{L2} increase at the same rate given by Eq. (6). At the same time, output filter capacitor C_F is being discharged by the load current since rectifiers D_1 and D_2 are reverse biased and the output part of the circuit is decoupled from the input part.

The converter enters the final topological stage shown in Fig. 5(d) at $t=T_3$ when switch S_2 is turned off and current i_{L2} is commutated from the switch into rectifier D_2 through capacitor C_B. During this stage, energy stored in inductors L_1 and L_2 during the preceding topological stage discharges into capacitor C_F. The rate of decrease of currents i_{L1} and i_{L2} is given by Eq. (10). Voltage V_O increases due to the flow of current i_{L2} into capacitor C_F. The circuit enters a new switching cycle at $t=T_4$ when switch S_2 is turned on again.

The voltage conversion ratio of the circuit can be calculated from the volt-second balance on the boost inductors. From Figs. 5 and 6, the volt-second balance equation for L_1 is

$$V_{IN} D \frac{T_S}{2} = \left(\frac{V_O}{4} - V_{IN}\right) \cdot \left(\frac{T_S}{2} - D\frac{T_S}{2}\right) \quad (11)$$

so that

$$\frac{V_O}{V_{IN}} = \frac{4}{1 - D}. \quad (12)$$

As can be seen from Eq. (12), the output voltage of the converter in Fig. 3 is at least four times larger than the input voltage. This high conversion ratio makes the converter the best suitable for applications with a high difference between output and input voltage.

As derived in this section, the high conversion ratio of the proposed converter is identical to that of the conventional converter. However, it should be noted that the input and the output are commonly grounded, which is desirable to reduce EMI.

4. Experimental Results

To verify the EMI performance of the proposed two-inductor boost converter, a commercially available power supply (DPSN-540AB) that consists of a conventional two-inductor boost front-end converter and an isolated dc-dc second stage converter was evaluated. The power supply was designed to operate from a 36-V–75-V battery input and deliver up to 45 A at a 12-V output. In this power supply, the front-end, conventional two-inductor boost converter, delivers approximately 1.5 A at 360 V to the output stage dc-dc converter.

First, the EMI of the power supply with a conventional two-inductor-boost front-end converter was measured. After the measurement, the front stage of the power supply was modified to the proposed two-inductor boost converter. The modification was done by reconnecting the diodes and replacing the filter capacitors. All of the semiconductor switches, magnetic components, and control circuits were left the same because their voltage and current stresses were unchanged.

Since the drain voltages of switches S_1 and S_2 were clamped to the voltages of blocking capacitor C_B and filter capacitor C_F, the peak voltage stress on switches S_1 and S_2 is approximately 180 V. Since the peak current stress on switches S_1 and S_2, which occurs at full load and low line, is approximately 17 A, an IRFP264 MOSFET (V_{DSS} = 250 V, I_{D25} = 38 A, R_{DS} = 0.075 Ω) from IR was used for each of the switches.

Since output diodes D_1 and D_2 must block the output voltage and must conduct the peak load current that is approximately 1.7 A, two RHRP3060 diodes (V_{RRM} = 600 V, I_{FAVM} = 30 A) from Fairchild were used. It should be noted that, to minimize the conduction losses of the switches and output diodes, devices with much higher current ratings than required were selected.

Each boost inductor was built using a toroidal core (Magnetics, Kool-μ 77548-A7) and 45 turns of magnet wire (AWG #14). A ferrite toroidal core (Philips, Ferrite TX29/19/7.6) was used in parallel with a Kool-μ core to increase the continuous-conduction-mode operation boundary. Specifically, the Kool-μ core and the ferrite toroidal core were wound together using magnet wire.

Auxiliary transformer ATR was built using a pair of ferrite cores (Philips, ER28L-3F3) with an air gap (2 mils). Two AWG #14 magnet wires with an equal number of turns (11 turns:11 turns) were used to obtain a desired magnetizing inductance, which is approximately 100 μH. Two aluminum capacitors (680 μF, 250 VDC) were used as output capacitors C_{F1} and C_{F2} of the conventional two-inductor boost converter. Both capacitors have an equal voltage stress, which is a half of output voltage V_O, since the converter naturally balances the voltages of output capacitors C_{F1} and C_{F2}.

For the proposed two-inductor boost converter, two parallel aluminum capacitors (180 μF, 450 VDC) were used as output capacitor C_F and two parallel polypropylene capacitors (2.2 μF, 250 VDC) were used as capacitor C_B.

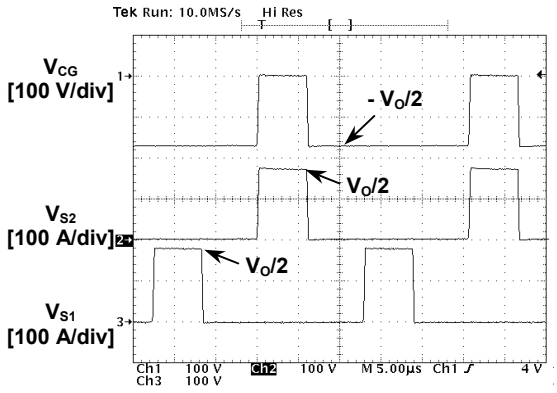

Fig. 7. Measured waveforms of conventional converter at V_{IN} = 40 V and V_O = 360 V. Time base: 5 μs/div.

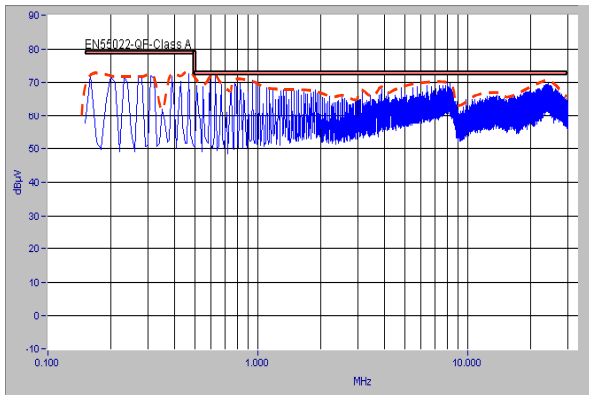

Fig. 8. Measured quasi-peak EMI of conventional converter at V_{IN} = 40 V, P_O = 240 W, and V_O = 360 V.

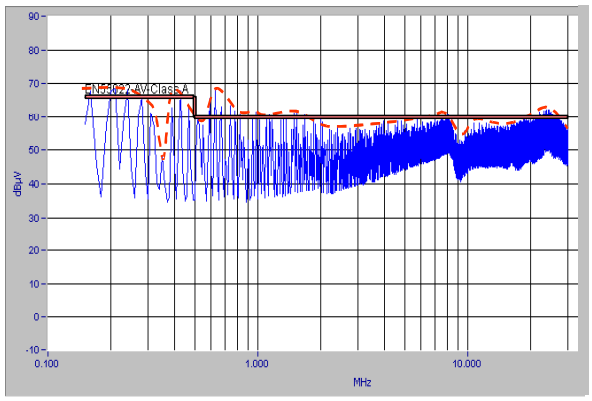

Fig. 9. Measured average EMI of conventional converter at V_{IN} = 40 V, P_O = 240 W, and V_O = 360 V.

Figure 7 shows the measured pulsating voltage V_{CG} in the conventional circuit shown in Fig. 1. The dv/dt of voltage V_{CG} coupled with a relatively large parasitic capacitance between the source-side and load side of the circuit causes strong EMI noise in the conventional two-inductor boost converter.

EMI noise was measured by using an EMI receiver (ER55C, 9 kHz-30 MHz, AFJ) and a line impedance stabilization network (LISN, NNB4/200X, Rolf Heine). The measured disturbance voltage [dBμV] was recorded by a personal computer.

Figures 8 and 9 show the measured quasi-peak EMI and the average EMI of the conventional two-inductor boost converter, respectively. Similarly, Figs. 10 and 11 show the measured quasi-peak EMI and the average EMI of the proposed two-inductor boost converter, respectively. In Figs. 8 and 10, dashed lines that represent the peak value of quasi-peak EMI of the conventional converter were added to help the comparison, whereas in Figs. 9 and 11, dashed lines that represent the peak value of the average EMI of the conventional converter were added.

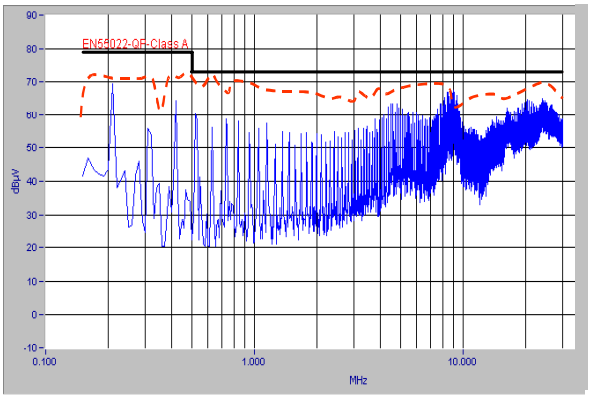

Fig. 10. Measured quasi-peak EMI of proposed converter at VIN = 40 V, PO = 240 W, and VO = 360 V. Dashed line shows the peak value of quasi-peak EMI of the conventional converter.

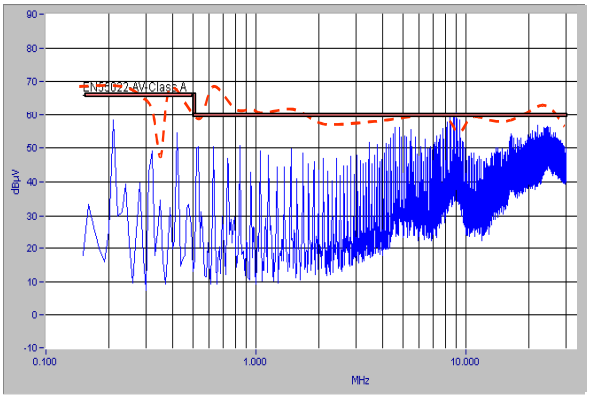

Fig. 11. Measured average EMI of proposed converter at V_{IN} = 40 V, P_O = 240 W, and V_O = 360 V. Dashed line shows the peak value of average EMI of the conventional converter.

From Fig. 8, the measured quasi-peak EMI of the conventional converter over the frequency range from 500 kHz to 1 MHz is quite high to meet the requirements of EN55022-Class A with the recommended margin which is typically 6 dBµV. Moreover, as shown in Fig. 9, the measured average EMI of the conventional converter cannot satisfy the requirements over the most of the frequency range.

As can be seen from Figs. 10 and 11, the proposed converter reduces the EMI in the entire measured frequency range. Specifically, the measured quasi-peak EMI of the proposed converter shows more than 10 dBµV margin from the requirements over the frequency range up to 4 MHz. The improvement of average EMI of the proposed converter is more pronounced as shown in Fig. 11.

It should be noted that the measured EMI of the proposed converter near 9 MHz is relatively high. Because the input source ground and the primary-stage ground of the printed circuit board (PCB) are connected by a wire to modify the prototype from the conventional converter to the proposed converter, the high frequency noise of the modified prototype was higher than expected. The EMI improvement will be more pronounced if a dedicated PCB is used. Although, the prototype of the proposed converter does not have a good PCB layout, it gives enough of a margin (> 6 dBµV) for the requirements of EN55022-Class A over the most of the frequency range.

5. Summary

A new implementation of a non-isolated, two-inductor, two-switch boost converter topology that features a common ground for the source and load has been described. The new circuit exhibits a significantly reduced common-mode noise compared to its counterpart implementing separate source and load grounds. The EMI performance of the proposed implementation was experimentally verified on a 540-W prototype. The proposed converter shows approximately 10 dBµV lower EMI than that of the conventional converter over the most of the frequency range.

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