A Comparative Study of Soft-Switched CCM Boost Rectifiers and Interleaved Variable-Frequency DCM Boost Rectifier

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Abstract – **In this paper three single-phase, high-power-factor rectifier implementations were evaluated on a comparative basis. Specifically, a zero-voltage-switching continuous-conduction-mode boost rectifier, a zero-current-zero-voltage-switching continuous-conduction-mode boost rectifier, and an interleaved variable-frequency discontinuous-conduction-mode boost rectifier were compared with respect to their efficiencies, compliance with the EN61000-3-2 specifications, complexity, and costs. The comparisons were done for the single-phase input voltage of 90 V_{rms} – 264 V_{rms} and for 0 – 1.2 kW output-power range.**

I. INTRODUCTION

In high-power off-line power supplies, a continuous-conduction-mode (CCM) boost rectifier is the preferred topology for implementing the front-end converter with active input-current shaping. However, since the dc-output voltage of the boost converter must be higher than the peak input voltage, the output voltage of the boost input-current shaper is relatively high. Due to the high output voltage, the converter requires the use of a high-voltage, fast-recovery boost rectifier. At high switching frequencies, fast-recovery rectifiers produce significant reverse-recovery-related losses when switched under "hard" switching conditions [1]. These losses can be significantly reduced and, therefore, a high efficiency can be maintained even at high switching frequencies by employing a soft-switching technique [2]-[7]. All of the proposed topologies in [2]-[7] use additional components to form an active snubber circuit that controls the turn-off di/dt rate of the boost rectifier.

The main features of the active approaches introduced in [2]-[6] is that besides soft switching of the boost rectifier they also offer soft switching of the boost switch. In addition, the approaches described in [4]-[7] offer soft switching of the auxiliary switch together with the boost switch.

Another method of achieving high efficiency while using high-voltage, fast-recovery rectifiers is to operate the boost converter at the boundary of discontinuous-conduction-mode (DCM) and CCM. The reverse-recovery-related losses are then eliminated because there is no stored charge in the boost rectifier at turn-on. Additionally, zero-voltage turn-on of the boost switch can be easily achieved. However, boundary operation requires additional input-current filtering and produces peak currents which are at least two times the input current averaged over a switching cycle. This is generally undesirable for high-power power-factor-correction (PFC) applications.

The drawbacks of the boundary operating boost converter can be alleviated if two or more converters are interleaved. Interleaving reduces the input-ripple current and peak input current while retaining the benefits of soft-switching of both boost rectifier and switch, as introduced in [8]-[9]. Specifically, an interleaving scheme utilizing voltage-mode control was introduced in [8] and an interleaving scheme utilizing hysteresis control was introduced in [9]. However, the interleaving of variable-frequency PFC boost converters, in general, requires a relatively complex interleaving circuit.

In this paper, an interleaving technique that utilizes current-mode control is proposed for the variable-frequency, boundary-operating PFC boost converter. This technique, though suitable for multiple converters, was developed for two converters which have a master-slave relationship. Specifically, the master operates at the boundary of DCM/CCM, while the slave always operates in DCM, but very close to the boundary.

The proposed interleaving circuit was evaluated and compared to two CCM single-phase, high power-factor rectifier implementations with respect to their efficiencies, compliance with the EN61000-3-2 specifications, complexity and costs. Specifically, the DCM/CCM boost interleaved converter is compared with the zero-voltage-switching (ZVS) CCM boost rectifier described in [5], and the zero-current-zero-voltage switching (ZC-ZVS) CCM boost rectifier describe in [7].

II. BRIEF REVIEW OF EVALUATED TOPOLOGIES

A. ZVS CCM Boost Rectifier [5]

The first evaluated topology, the ZVS CCM boost rectifier which employs an active snubber for reverse-recovery-loss reduction, is shown in Fig. 1. The circuit in Fig. 1 uses a snubber inductor L_S, which is connected in series with the

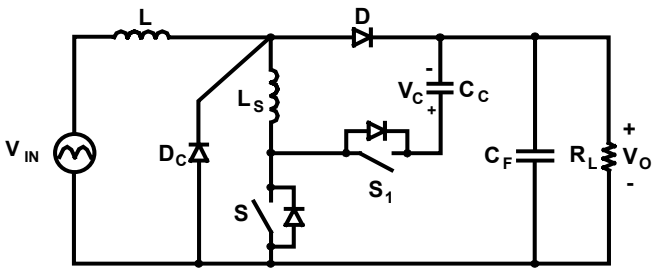

Fig. 1 Schematic diagram of ZVS CCM boost rectifier [5]

boost switch S and rectifier D, to control the di/dt rate of the rectifier when boost switch S is turned on. In addition, the series connection of auxiliary switch S_1, clamp capacitor C_C is used to discharge the energy stored in inductor L_S to the output after S is turned off. During this period, the energy stored in inductor L_S flows through the body diode of auxiliary switch S_1. Therefore, auxiliary switch S_1 can be turned on with ZVS. Before auxiliary switch S_1 turned off, the current direction of L_S was changed to achieve the charge balance of C_C. As a result, the energy stored in inductor L_S is also used to discharge the output capacitance of boost switch S prior to the switch turn-on, thus eliminating its capacitive turn-on switching loss of S. Diode D_C is employed to eliminate the parasitic ringing between the junction capacitance of rectifier D and the snubber inductor by clamping the anode of D to ground.

B. ZC-ZVS CCM Boost Rectifier [7]

The second evaluated topology, the boost converter with the ZC-ZVS switch cell, is shown in Fig. 2. The circuit in Fig. 2 also uses snubber inductor L_S, which is connected in series with main switch S and rectifier D, to control the di/dt rate of the rectifier. Along with S, and L_S, auxiliary switch S_1, clamp capacitor C_C, and clamp diode D_C form a ZC-ZVS cell as indicated by the dashed line in Fig. 2. The circuit shown in Fig. 2 improves the performance of the CCM boost converter by eliminating the switching losses with a ZC-ZVS switch cell. The ZC-ZVS cell reduces the reverse-recovery-related losses of the rectifier and provides soft switching of the main and auxiliary switches. Specifically, the main switch in the proposed ZC-ZVS cell turns off with ZCS, making the IGBT

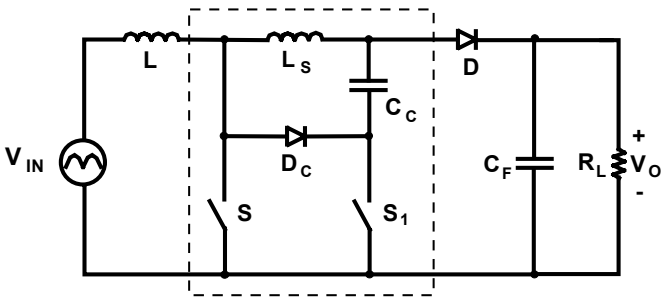

Fig. 2 Schematic diagram of ZC-ZVS CCM boost rectifier [7].

a good choice, whereas the auxiliary switch turns on with ZVS. In addition, because the proper operation of the ZC-ZVS switch cell requires that the conduction period of the main switch and the auxiliary switch overlap, the proposed switch cell is not susceptible to failures due to accidental transient overlapping of the main and auxiliary switch gate drives. Finally, the complexity and cost of the converters using the proposed technique is further reduced because the proposed ZC-ZVS switch cell requires a simple non-isolated (direct) gate drive for both switches.

C. Interleaved Variable-Frequency DCM Boost Rectifier

The third evaluated topology, two interleaved boost converters which share a common error voltage configured with a master-slave, current-mode control circuit, is shown in Fig. 3. Since the boost rectifiers operate at the boundary of DCM/CCM there are no reverse-recovery related losses and hence no need for active or passive snubber components as in [1]-[7]. Therefore, in the circuit in Fig. 3, the design challenge is shifted from the power stage to the control circuit to achieve soft-switching of the boost diode and switch.

III. IMPLEMENTATION OF INTERLEAVING CONTROL CIRCUIT

Interleaving of multiple parallel connected converters requires both good current sharing and precise control of the interleaving instant. To achieve good interleaving of two parallel connected boost converters, the peak input current of each should be 180 degrees out-of-phase. Generally, this means that one converter must turn-on at the half-period instant of the other-converter's switching interval for proper synchronization. However when the switching frequency is variable, the half-period instant becomes variable, making synchronization difficult.

Current sharing in current-mode-controlled converters can be achieved by applying a common error voltage to each converter. Generally, in current-mode control, the turn-off of the switch occurs at the instant when the sensed switch

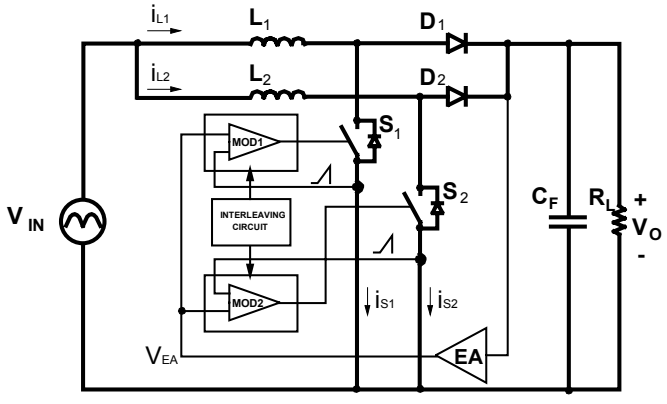

Fig. 3 Schematic diagram of interleaved, variable-frequency DCM boost rectifier with current-mode control.

current at the input of the modulator becomes equal to error voltage V_{EA}. For constant-frequency control, the turn-on instant of the switch is initiated by the controller clock. For variable-frequency control, which is required for the DCM/CCM operation, the switch is turned on shortly after the inductor current falls to zero. If the component values of the interleaved converters operating with variable-frequency were identical, each and every converter would operate at the DCM/CCM boundary, as illustrated in Fig. 4(a) for the case of two interleaved converters. However, in practice, components of interleaved converters are not likely to be the same due to the component tolerances. As a result, the operation of the individual converters in an interleaved scheme would not be the same. To illustrate the effect of the component mismatching on the operation of the variable-frequency interleaved converters, Figs. 4(b) and 4(c) show the inductor current waveforms of two interleaved converters with mismatched boost inductances, i.e., for $L_1 > L_2$. As can be seen from Figs. 4(b) and 4(c), because of the difference in the boost-inductor values, the up-slope and down-slope of the inductor current i_{L1} and i_{L2} are different. Namely, since $L_1 > L_2$, the slope of module #1 is less steep than the corresponding slopes of module #2. As a result, for the same line and load conditions, module #1 requires a lower frequency than module #2 to operate at the DCM/CCM boundary. Therefore, if power stage components of variable-frequency interleaved converters are mismatched, it is not possible to operate all individual converters at the DCM/CCM boundary.

As shown in Fig. 4(b), if module #2 is made to operate at the DCM/CCM boundary, module #1 has to operate in CCM since module #2 achieves the DCM/CCM operation at a higher frequency than module #1. On the other hand, if module #1 is made to operate at the DCM/CCM boundary, module #2 has to operate in DCM, as shown in Fig. 4(c). Therefore, in a design which eliminates reverse-recovery losses by not allowing operation in CCM, only one converter can operate at the DCM/CCM boundary, whereas all the others operate in DCM. As a result, ZVS of the switches in all converters but one is lost, unless the control circuit is sophisticated enough to wait for the charge in the output of the main switch to resonate with the boost inductance to zero.

One method of achieving interleaving between multiple converters operating with variable frequency and current mode control is to design a control circuit which imposes a master/slave relationship between converters.

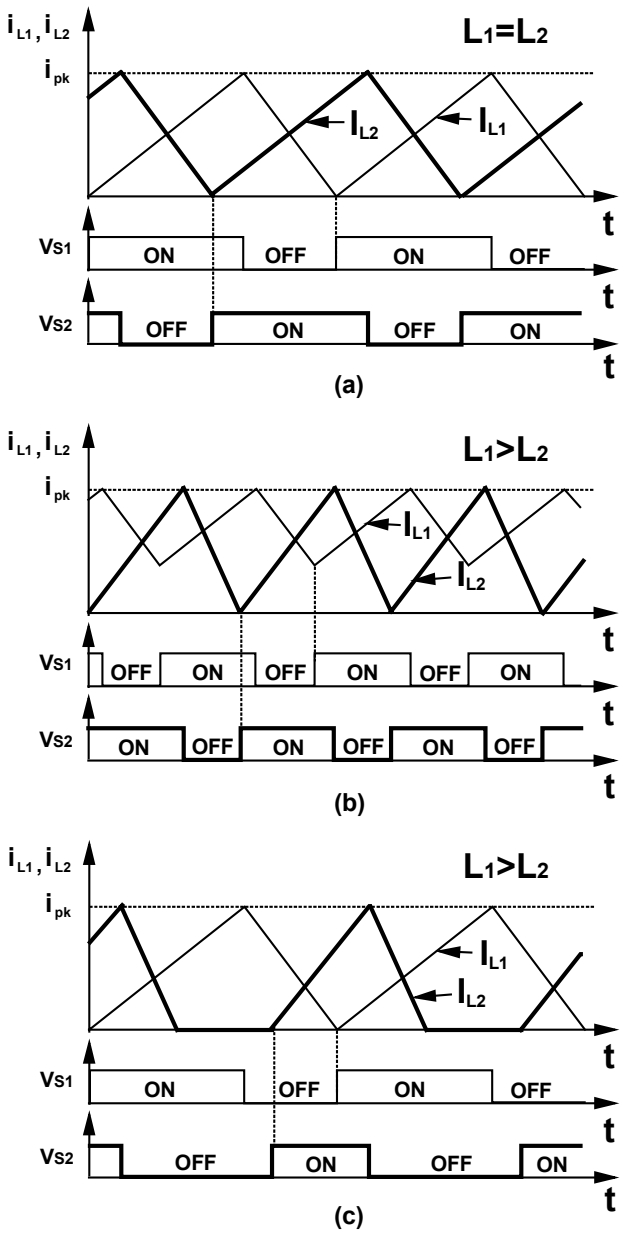

Fig. 4 General switching waveforms of two interleaved variable-frequency DCM/CCM boost rectifiers operating with current-mode control for a) converters with identical power-stage components ($L_1 = L_2$); b) converters with mismatched power-stage components ($L_1>L_2$) and module #2 with DCM/CCM operation; c) converters with mismatched power-stage components ($L_1>L_2$) and with module #1 with DCM/CCM operation.

A. Master/Slave Interleaving Approach

Interleaving current-mode controlled converters which have a master-slave relationship generally means that the slave turn-on is controlled by the master, whereas for both master and slave, turn-off is controlled by the individual converter. Since the master is chosen as the converter which operates at the boundary of DCM/CCM, steps must be taken to ensure that the slave reaches DCM before the master reaches its half-period instant. This can be achieved if the current loop gain of each converter are mismatched, either by implementing different value inductors (i.e., $L_M>L_S$), which is generally undesirable from a manufacturing point of view, or by adjusting the current sensing gain. However, it should be noted that if the gain of the current loops are mismatched, the peak of the individual inductor currents will also be mismatched. This then affects the current-sharing accuracy of the two converters.

Figure 5 illustrates the general switching waveforms of two interleaved current-mode controlled converters which have a master-slave relationship. For simplicity, the slope of the inductor currents are the same while the slope of the sensed switch current of each are different. However, there is nothing to prevent the slope of the inductor currents (i.e. the value of inductors L_S and L_M) from becoming mismatched.

When gate of master $G_{(master)}$ is high, master inductor current i_{LM} ramps up, and the voltage across master auxiliary winding $V_{auxmaster}$ is $-V_{IN}/N$. Master current-sense voltage V_{C-S}^{master} is proportional to i_{LM}, until it reaches the level of control voltage V_C. $G_{(master)}$ then goes low, diode D_M turns on, $V_{auxmaster}$ changes instantaneously to $(V_O - V_{IN})/N$, and i_{LM} is delivered to the output, while switch S_M turns off and V_{C-S}^{master} becomes zero. When i_{LM} becomes slightly negative, $G_{(master)}$ becomes high again completing one full switching cycle. The half-period instant is then determined initiating turn-on of slave gate $G_{(slave)}$. Slave inductor current i_{LS} ramps up, slave auxiliary voltage $V_{auxslave}$ is equal to $-V_{IN}/N$ and slave current-sense voltage V_{C-S}^{slave} follows i_{LS} with a slope 10% greater than V_{C-S}^{master}. When V_{C-S}^{slave} reaches V_C, $G_{(slave)}$ turns off, diode D_S turns on, $V_{auxslave}$ instantaneously changes to $(V_O-V_{IN})/N$ and i_{LS} decreases as it sources current to the output. When i_{LS} decreases to zero, the output capacitance of S_S resonates with L_S and C_{IN} until the half-period instant of the previous switching cycle of the master is reached, signaling the instant of $G_{(slave)}$ turn-on and the end of its switching cycle. While inductor L_S is discontinuous, the voltage across the auxiliary winding fluctuates between $(V_O-V_{IN})/N$ and $-V_{IN}/N$ as the output capacitance of the switch S_S rings with L_S and C_{IN}.

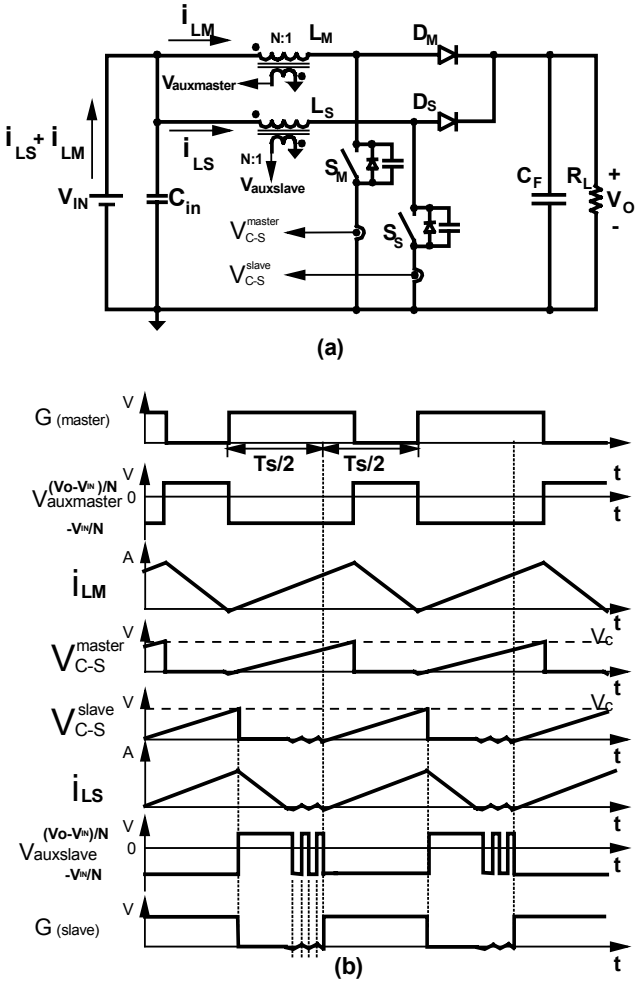

Fig. 5 General schematic and switching waveforms of two interleaved, current-mode controlled boost converters with master-slave relationship.

B. Determining Half-Period Instant of Master

A solution to determining the half-period instant of two interleaved, parallel connected boost converters operating with current-mode control is to utilize the properties of similar triangles. In general, triangles are said to be similar when their corresponding angles are equal. Figures 6 and 7 are used to facilitate the explanation of the proposed interleaving circuit.

Figure 6 is a block diagram representation of the proposed interleaving circuit. Its corresponding waveforms are depicted in Fig. 7. To determine the half-period instant of the master, information from the master's previous switching cycle is used. Since the input voltage V_{IN} is nearly constant for a switching cycle, it is reasonable to approximate that the switching frequency is nearly constant for several switching cycles.

A voltage ramp is generated with a constant slope using a current source and capacitor. V_{RAMP} is then reset at the end of a switch cycle by a pulsed reset (i.e., a pulse of a very short duration). This creates a sawtooth waveform V_{RAMP} whose slope is independent of line and load conditions, and whose peak V_{PK} is a function of the master's switching frequency.

Two peak detectors, V_{peak1} and V_{peak2}, are used to store V_{PK}. The output of each are divided by two and reset 180 degrees out-of-phase. The halved outputs of the peak detectors are then compared to V_{RAMP}. The output is a voltage waveform $V_{Ts/2}$ which operates with a 50% duty cycle and is synchronized to G_{master}. The half-period instant is reached when $V_{Ts/2}$ transitions from high to low (i.e., when V_{RAMP} reaches half the peak of the previous switching cycle) due to a property of similar triangles (i.e., a triangle whose peak is one-half that of another triangle which it is similar to has a base which is also one-half that of the other triangle).

This method of determining the instant of turn-on can be generalized for N converters. In the case of N converters, the 1/N-period instant must be determined to achieve proper interleaving, which again can be achieved using N peak detectors whose outputs are divided by N and compared against a single V_{RAMP}.

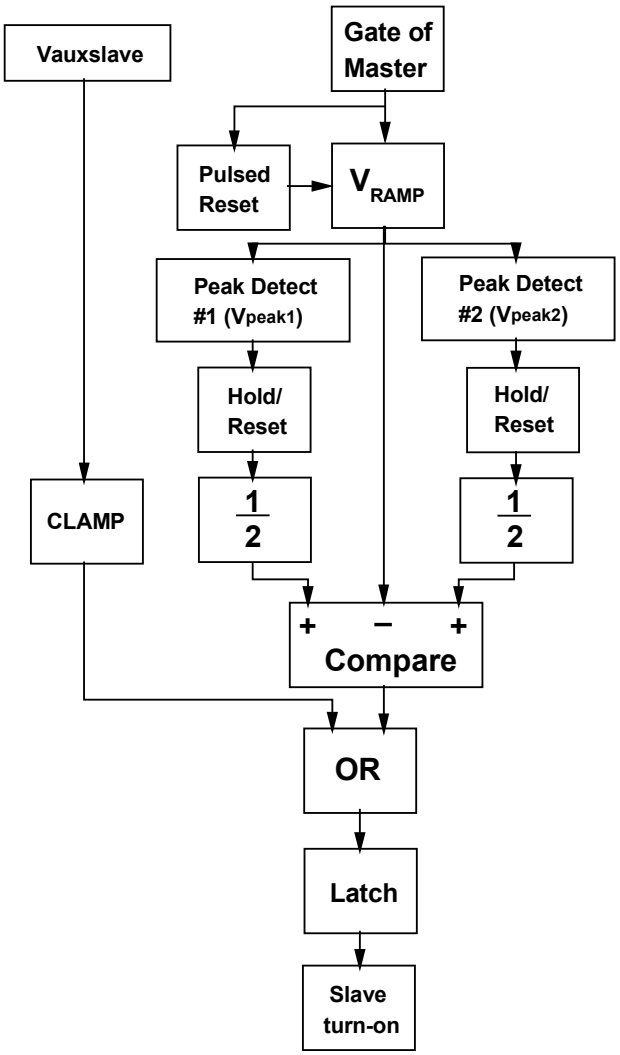

Fig. 6 Block diagram representation of proposed interleaving circuit.

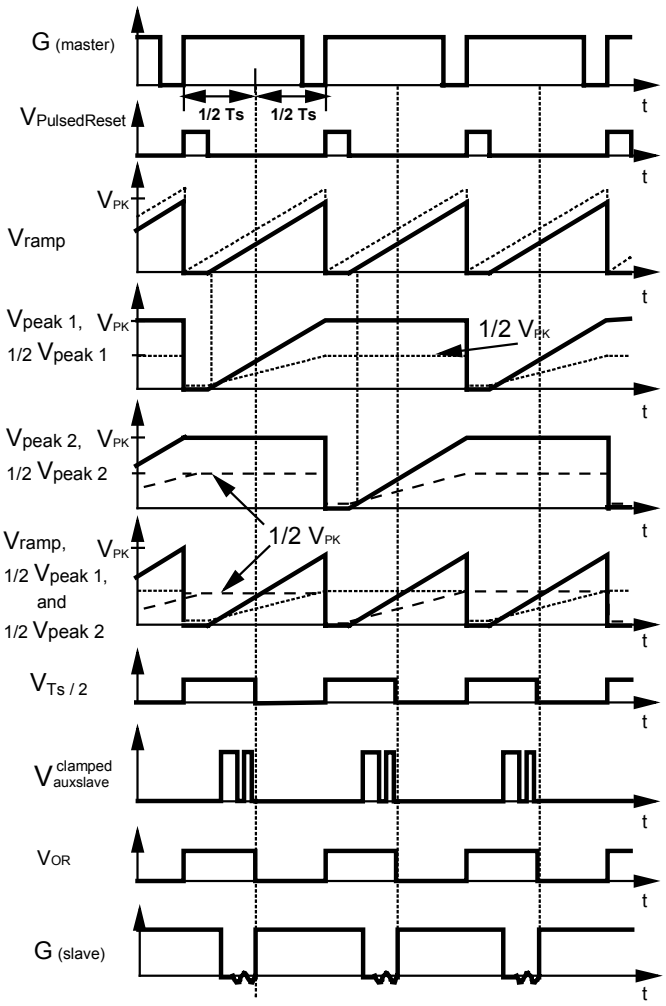

Fig. 7 Proposed interleaving control circuit waveforms.

Though the half-period instant is determined, ZVS of the main switch is not guaranteed unless the slave turns on when the charge in the output of the switch is zero. By clamping the voltage derived from the slave auxiliary winding $V_{auxslave}^{clamped}$, OR-ing it with $V_{Ts/2}$ and assuming that the resonant period is short, ZVS turn on of S_2 is achieved. It is then necessary to latch the slave converter in the on-state until the end of the on-time.

IV. Experimental Results

To verify the operation and performance of the proposed interleaving circuit, two 600-W (385-V/ 1.6-A), universal line voltage (90-264 V_{RMS}) boundary operating PFC boost converters were interleaved as in Fig. 3. The control circuit was implemented using the variable-frequency power-factor-controller integrated circuit MC33262 and standard analog devices and logic gates. The measured line-voltage and unfiltered input current waveforms at low-line (Vin = 90-V_{RMS}) and full-load (1.2-kW) are shown in Fig. 8. It can be seen from Fig. 8 that the input-ripple current has been reduced to slightly less than 50% of the input current averaged over a switching cycle. Figure 9 shows the individually measured inductor currents i_{LS}, i_{LM} and the sum $i_{LS} + i_{LM}$ which is the resulting input-ripple current. From Fig. 9 it can be seen that the master always operates at the boundary of DCM/CCM and that the slave operates very close to the boundary of DCM/CCM. The slightly mismatched peak-inductor currents are a result of mismatched master and slave current loop gains. By mismatching the current loop gains, the dead time of the slave switching cycle can be further minimized.

The proposed interleaving technique results in very good interleaving quality at low line and full load. However, as the switching frequency increases (i.e., high line and light load),

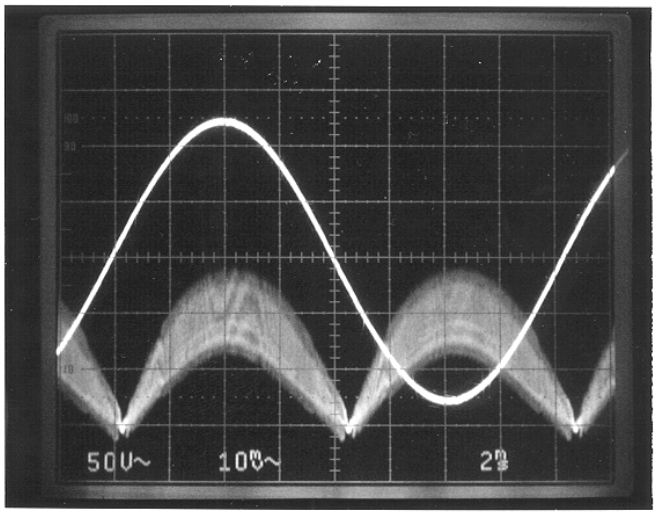

Fig. 8 Unfiltered input current (lower waveform, 10 A/div) and input voltage (upper waveform, 50 V/div) waveforms of interleaved variable-frequency DCM boost rectifier at Vin = 90 V_{RMS}, V_O = 385 V, P_O = 1.2 kW.

it was found that the interleaving quality degrades due to the effects of the pulsed reset, which prevents V_{RAMP} from spanning the entire switching cycle, and the amplitude of V_{RAMP}, which is inversely proportional to the switching frequency (i.e., V_{RAMP} decreases below 1-V). Consequently, interleaving was removed for high-line, light-load conditions since interleaving is not crucial in this range.

V. COMPARISON OF CCM VS. DCM TECHNIQUES

The performance of the three experimental power-factor-correction boost converters were evaluated for a 1.2 kW (385 V/ 3.12 A) output power and universal-line (90 – 265 V_{RMS}) input range. The power stage components which were utilized for the three experimental circuits are described in Table I. The control circuits for the CCM boost converters with ZVS (Fig. 1) and ZC-ZVS (Fig. 2) were implemented with an average-current mode PFC controller UC3854.

The input harmonic currents of these rectifiers were measured and compared with the harmonic current limits of the EN61000-3-2 regulation. The results show that the THD and PF of all three experimental boost rectifiers at the full load condition are less than 10% and higher than 99%, respectively. The THD and all harmonic currents of the three topologies well meet the EN61000-3-2 regulation over the entire input voltage and output power range.

Figure 10 shows the measured efficiencies of the experimental converters. As can be seen from Fig. 10, all three experimental circuits show good efficiency over the entire input voltage and output power range. It should be noted that for evaluation purposes, the same input filter was used for all three experimental circuits. However, the input-ripple current for the interleaved variable-frequency DCM boost converter is slightly less than 50% of the input current averaged over one switching cycle as compared to the soft-switched CCM boost, whose input-ripple current is less than 15%. Therefore, the interleaved boosts require additional input-current filtering to attenuate the input-ripple current to the same level as the other topologies. To account for the additional loss, the interleaved converter efficiency data at low line shown in Fig. 9 should be reduced by 1-2%. Generally, the interleaved variable-frequency DCM boost rectifier has a comparable efficiency with the two soft-switched CCM boost rectifiers. However, the interleaved circuit is more complex than the ZVS and ZC-ZVS boost rectifiers since it requires more components to implement the power stage, as well as the control circuit.

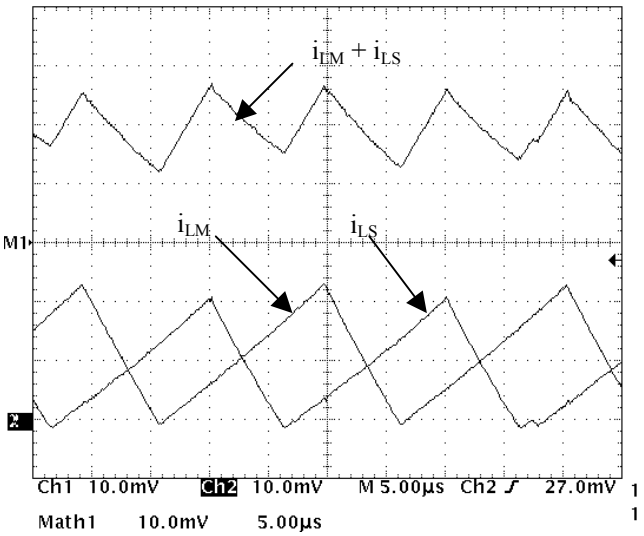

Fig. 9 Measured inductor currents at full load, Vin = 90 V_{RMS}.

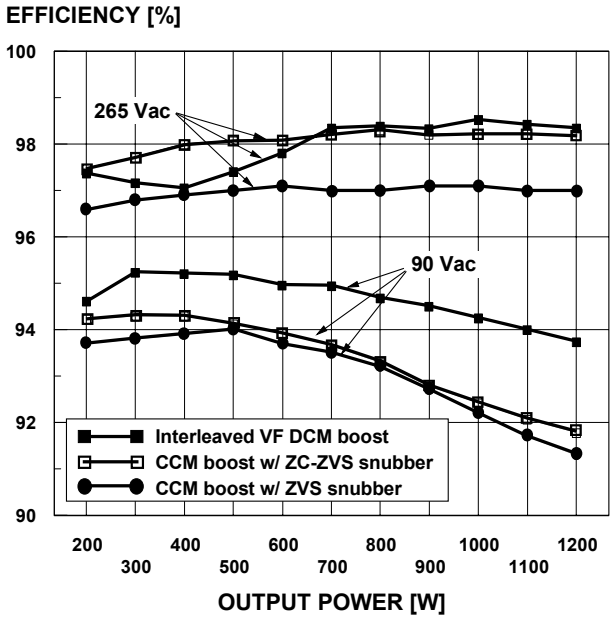

Fig. 10 Measured efficiencies of experimental rectifiers.

TABLE I

Power Stage Components for ZVS CCM, ZC-ZVS CCM, and Interleaved Variable-Frequency DCM Boost Converters

Components	ZVS CCM Boost rectifier	ZC-ZVS CCM Boost Rectifier	Interleaved Variable-Frequency DCM Boost Rectifier
Boost Switch S	IXFK48N50B (MOSFET)	IXGK50N60B (IGBT)	4 x IRFP460 (MOSFET)
Auxiliary Switch S_1	IRFP460 (MOSFET)	IRFP460 (MOSFET)	NONE
Output Diode D	2 x RHRP3060	2 x RHRP3060	2 x RHRP3015
Clamp Diode D_C	RHRP3060	RHRP3060	NONE
Clamp Capacitor C_C	6.8 µF / 100 V	6.8 µF / 100 V	NONE
Boost Inductor L	L = 0.5 mH (four 0.125 mH inductors in series). Core = toroidal core (Kool-µ 77071-A7), wire = 45 turns of magnet wire (AWG #12).	L = 0.5 mH (four 0.125 mH inductors in series). Core = toroidal core (Kool-µ 77071-A7), wire = 45 turns of magnet wire (AWG #12).	L = 2 x 79 µH (one inductor for each DCM boost power stage) Core = toroidal core (Kool-µ 77256-A7), wire = 48 turns of Litz wire (strands = 435 wire size = AWG #40).
Snubber Inductor	L_S = 3.3 µH, Core = toroidal core (Kool-µ 77312-A7), wire = 12 turns of magnet wire (AWG #12)	L_S = 3.3 µH, Core = toroidal core (Kool-µ 77312-A7), wire = 12 turns of magnet wire (AWG #12)	NONE
Output Capacitor C_F	2 × 470 µF / 450 V	2 × 470 µF / 450 V	2 × 470 µF / 450 V
Required Attenuation of DM-EMI Filter	Approximately 91 dB at 80 kHz	Approximately 91 dB at 80 kHz	Approximately 97 dB at 50 kHz
Complexity of Control Circuit	Average Current Mode Control (Moderate)	Average Current Mode Control (Moderate)	Two Variable-Frequency Control with Interleaving Circuit (Complex)
Switching Frequency f_S	80 kHz	80 kHz	50 kHz - 460 kHz

VI. CONCLUSIONS

An interleaving technique for the variable-frequency, DCM PFC boost rectifier which utilizes current-mode control is described. A comparison is made against a ZVS CCM boost rectifier and a ZC-ZVS CCM boost rectifier with respect to their efficiencies, compliance with the EN61000-3-2 specifications, complexity, and costs. The comparisons were done for the universal input voltage range 90 V_{RMS} to 264 V_{RMS} and for the load range 0 W – 1.2 kW.

It was found that the efficiency of the interleaved variable-frequency DCM boost rectifier is similar to the efficiency of the two soft-switched CCM boost rectifiers. However, the interleaved boost converter requires significantly more complex control circuit, as well as more components to implement the power stage.

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