Constant-Frequency Resonant Inverter for AC-Bus Distribution System

Yungtaek Jang and Milan M. Jovanović

Delta Products Corporation
Power Electronics Laboratory
P.O. Box 12173, 5101 Davis Drive
Research Triangle Park, NC 27709

***Abstract* — A new constant-frequency dc-ac resonant inverter that employs a coupled inductor to achieve ZVS in an entire load and input voltage range with a reduced circulating current is described. The proposed technique is suitable for ac-bus distribution power systems in data-processing equipment. The performance of the proposed approach was evaluated on a 230-W inverter that delivers 1-MHz, 27-V_{RMS} ac output voltage from a 320 V - 400 V dc input.**

I. INTRODUCTION

Generally, a high-frequency inverter employs a resonant or a soft-switching technique to reduce switching losses and, consequently, improve conversion efficiency. However, the majority of these resonant-type and soft-switched-type inverters require variable-frequency control to maintain the regulation of their outputs [1]-[3]. While variable-frequency control exhibits acceptable performance in many applications, a number of applications require constant-frequency control. One of the most notable applications that requires a constant-frequency inverter is the ac-bus distribution power system. In such a system, a constant-frequency sinusoidal or trapezoidal ac voltage is distributed to the loads for a final point-of-load conversion by load converters.

Constant-frequency control of inverters is implemented by phase control, which is also called "out-phasing modulation" [4]-[8]. In this type of control, output regulation is achieved at a constant frequency by phase shifting the switching instances of the corresponding switches in the two legs of the inverter. With no phase shift, the output delivers full power, whereas for a phase shift of 180º, the output power is reduced to zero. Generally, the parallel-resonant inverter (PRI) topology and series-parallel resonant inverter (SPRI) topology are employed in applications which require no load operation since the series-resonant inverter (SRI) topology cannot regulate the output at no load.

Figure 1 shows the circuit diagram of a conventional isolated full-bridge PRI. The parallel resonant circuit in Fig. 1 is implemented with primary-side resonant inductor L_R and secondary-side resonant capacitor C_R. However, it should be noted that the resonant capacitor could also be placed across the primary winding. Regardless of the placement of the resonant capacitor, the circuit in Fig. 1 offers a sinusoidal output voltage with relatively low harmonic distortion, as well as output voltage regulation in the entire load range from the full load down to no load. The major deficiency of the PRI is a relatively low partial-load efficiency due to a significant amount of circulating energy in its resonant tank, which is required to maintain output voltage regulation and soft-switching at lighter loads. As a result, the PRI is not suitable for applications that require low power loss at light loads such as power supplies for personal computers.

The light-load performance of the PRI can be improved by employing the SPRI topology shown in Fig. 2 [8]. In the symmetrical SPRI circuit in Fig. 2, which consists of two bridge legs and multiple resonant components, inductors L_{R1} and L_{R2} form series resonant circuits with corresponding series capacitors C_{S1} and C_{S2} and parallel resonant circuits with capacitor C_P. Because a properly designed SPRI circuit behaves like a PRI circuit at light loads and like an SRI circuit at higher loads, the SPRI can regulate the output down

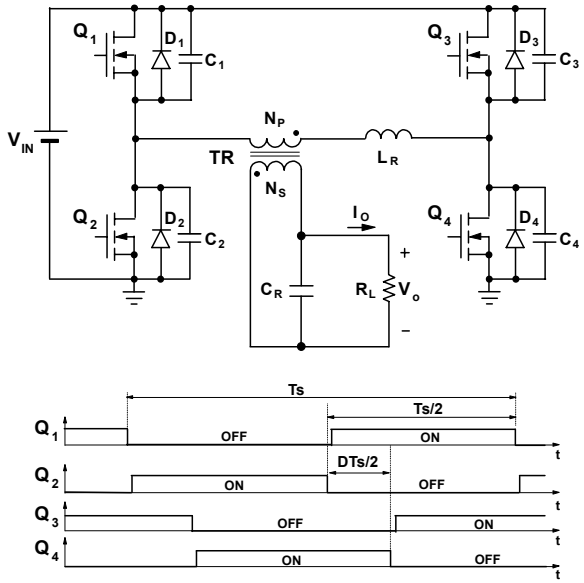

Fig. 1. Conventional parallel resonant inverter and its gate waveforms.

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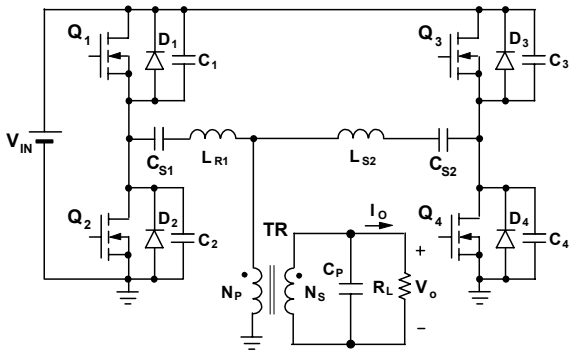

Fig. 2. Conventional class-D isolated phase-controlled series-parallel inverter [8].

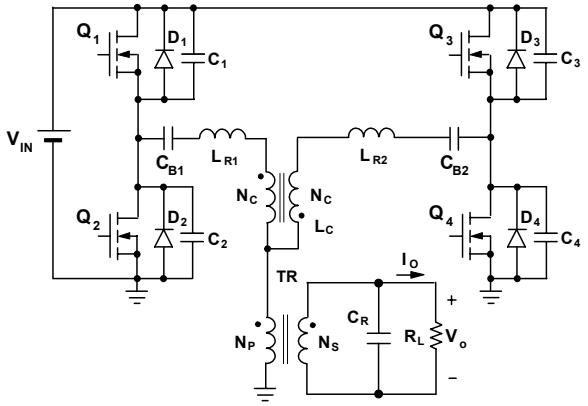

Fig. 3. Proposed parallel resonant inverter with a coupled inductor.

to no load with improved partial-load efficiency. Nevertheless, although the circulating energy in the SPRI is reduced compared to that of the PRI, the SPRI still circulates an unnecessarily high amount of energy to maintain soft switching in the entire load and input-voltage range. Moreover, because the Q-factor of a properly designed SPRI that minimizes circulating energy is usually lower than the corresponding Q-factor of the PRI, the output voltage of the SPRI typically exhibits more harmonic distortions than the output voltage of the PRI.

In this paper, a new constant-frequency, dc-ac inverter that employs a coupled inductor to achieve ZVS in a wide range of load currents and input voltages with reduced circulating energy is described. The output voltage regulation in the proposed inverter is achieved by constant-frequency phase-shift control. The performance of the proposed constant-frequency sinusoidal inverter was experimentally verified on a 1-MHz, 230-W prototype that was designed to operate from a 320 V - 400 V dc input and deliver 27-V_{RMS} ac output voltage.

II. Parallel Resonant Inverter with a Coupled Inductor

The proposed inverter that employs a coupled inductor on its primary side to extend the ZVS range of its switches with minimum circulating energy and conduction loss is shown in Fig. 3. The circuit in Fig. 3 is an isolated PRI, which utilizes a parallel resonant-tank circuit consisting of primary side resonant inductors L_{R1} and L_{R2} and secondary-side resonant capacitor C_R to generate a sinusoidal voltage at the output. One terminal for each of the two resonant inductors is connected to its corresponding inverter leg through a blocking capacitor, while the other terminal is connected with its corresponding winding in coupled inductor L_C, whose common terminal is connected to transformer TR. The two primary capacitors, C_{B1} and C_{B2} are used to prevent saturation in the coupled inductor and in transformer cores by blocking the flow of the dc current through L_C and TR. Generally, in the PRI these capacitors are selected large enough so that their voltages are approximately constant during a switching cycle.

The proposed inverter circuit shown in Fig. 3 utilizes the sum of the energy stored in resonant inductors L_{R1} and L_{R2} and the magnetizing inductance of coupled inductor L_C to discharge the capacitance across the switch that is about to be turned on and, consequently, achieve ZVS. Moreover, since coupled inductor L_C can transfer current (energy) from the winding in one bridge leg to another, the circuit has the unique characteristic that all switches are turned off when they carry a current of the same magnitude. As a result, the energy available for the discharge of the capacitance of the switch is the same for all switches. In addition, the proposed circuit can achieve ZVS of the switches at no load by properly selecting the value of the magnetizing inductance of the coupled inductor. In the proposed circuit, since the energy required for ZVS is mainly provided by the energy stored in the magnetizing inductance of the coupled inductor, the circulating energy of the resonant tank circuit can be

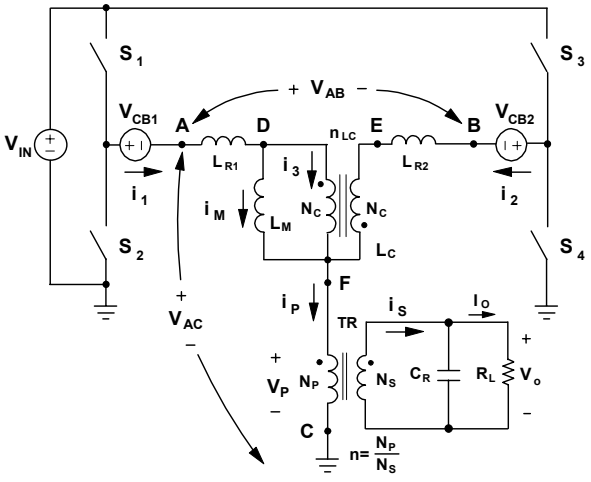

Fig. 4. Simplified circuit diagram of the proposed inverter shown in Fig. 3 along with reference directions of key currents and voltages.

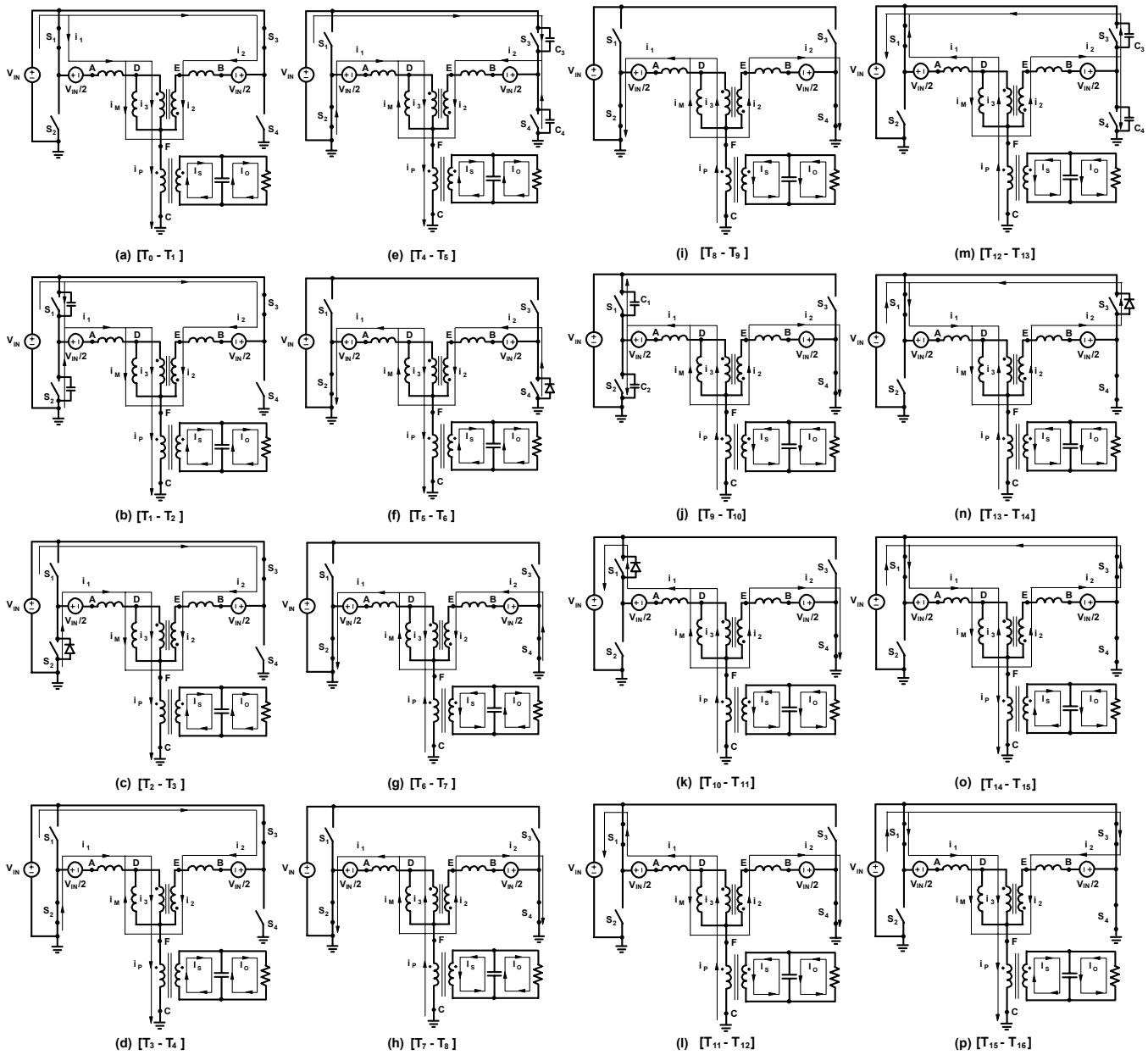

Fig. 5. Topological stages during a switching period.

minimized, which significantly improves partial-load efficiency.

To facilitate the explanation of the operation of the circuit in Fig.3, Fig. 4 shows its simplified circuit diagram. In the simplified circuit, it is assumed that the capacitance of blocking capacitors C_{B1} and C_{B2} is large enough so that the capacitors can be modeled as constant voltage sources. Because the average voltages of the coupled inductor windings and the transformer windings during a switching cycle are zero and because the pair of switches in each bridge leg operates with 50% duty cycle when phase-shift control is used, the magnitude of voltage sources V_{CB1} and V_{CB2} in Fig. 4 is equal to $V_{IN}/2$, *i.e.*, $V_{CB1}=V_{CB2}=V_{IN}/2$.

To further simplify the analysis, it is also assumed that the resistance of the conducting semiconductor switches is zero, whereas the resistance of the non-conducting switches is infinite. In addition, small leakage inductances in the coupled inductor and transformer, as well as a large magnetizing inductance in the transformer are neglected because their effect on the operation of the converter is negligible. The magnetizing inductance of coupled inductor L_C and output capacitances of primary switches $C_1 – C_4$ are not neglected in this analysis since they play a major role in the operation of

the circuit. In Fig. 4, coupled inductor L_C is modeled as an ideal transformer with turns ratio n_{LC}=1 and with magnetizing inductance L_M parallel to winding DF. The number of turns for each of the windings of L_C is N_C.

Finally, to further facilitate the analysis, Fig. 5 shows the topological stages of the converter during a switching cycle, whereas Fig. 6 shows the key waveforms.

As can be seen from Fig. 4, because the turns ratio of the windings of L_C is unity (n_{LC}=1), current i_3 flowing through winding DF is always equal to current i_2 flowing through winding EF, *i.e.*, $i_3=i_2$. As a result,

$$i_1 = i_3 + i_M = i_2 + i_M , \tag{1}$$

and since

$$i_P = i_1 + i_2 \tag{2}$$

the relationship between currents i_1, i_2, i_M, and i_P can be expressed as

$$i_1 = \frac{1}{2}\left(i_P + i_M\right) \tag{3}$$

and

$$i_2 = \frac{1}{2}\left(i_P - i_M\right). \tag{4}$$

As shown in Fig. 6, during the time interval T_0–T_1, switch S_1 in leg S_1-S_2 and switch S_3 in leg S_3-S_4 are closed and currents i_1 and i_2 flow through the corresponding switch, blocking capacitor, resonant inductor, and winding of the coupled inductor into the primary of the transformer, as can be seen in the equivalent circuit in Fig. 5(a). From Fig. 5(a), it can also be seen that voltage v_{AB} must be zero during this topological stage since voltage sources $V_{CB1}=V_{IN}/2$ and $V_{CB2}=V_{IN}/2$ are connected in opposition through closed switches S_1 and S_3. Furthermore, because of the winding orientation of coupled inductor L_C (dot positions in Fig. 5(a)),

$$v_{AB} = v_{AD} + v_{DF} + v_{FE} + v_{EB} =$$
$$L_{R1}\frac{di_1}{dt} + v_{DF} + v_{FE} - L_{R2}\frac{di_2}{dt} = 0 \tag{5}$$

can only be maintained if the voltages across the couple inductor windings are zero. Namely, for a relatively large magnetizing inductance L_M, magnetizing current i_M is virtually constant during the T_0–T_1 interval so that $di_1/dt=di_2/dt$ and, therefore, for $L_{R1}=L_{R2}$, $v_{AD}=-v_{EB}$. As a result, relationship $v_{AB}=v_{AD}+v_{DF}+v_{FE}+v_{EB}= v_{DF}+v_{FE}=0$ can only be fulfilled if $v_{DF}=v_{FE}=0$ since both v_{DF} and v_{FE} are positive (*i.e.*, have same polarity). As shown in Fig. 6(j), in this topological stage $v_{AC}=v_{BC}=V_{IN}-V_{IN}/2=V_{IN}/2$.

When at $t=T_1$, switch S_1 is turned off, and current i_1 is diverted from the transistor of switch S_1 to its output capacitance C_1, as shown in Fig. 5(b). In this topological stage, current i_1 charges capacitor C_1 and discharges capacitor C_2 at the same rate since the sum of the capacitor voltages is equal to constant voltage V_{IN}, as illustrated in Figs. 6(e) and (f). As a result, the potential of point A starts decreasing causing a decrease of voltages v_{AB} and v_{AC}.

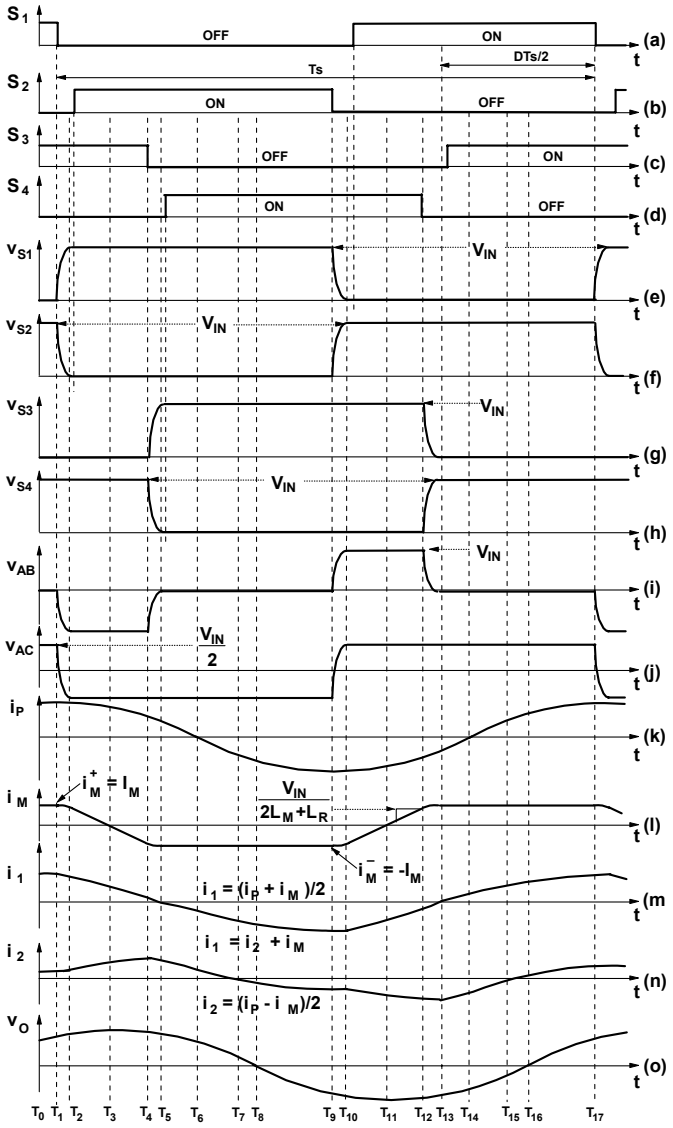

Fig. 6. Key waveforms.

Namely, v_{AB} decreases from zero toward negative V_{IN}, whereas v_{AC} decreases from $V_{IN}/2$ toward negative $V_{IN}/2$, as illustrated in Figs. 6(i) and (j). After capacitor C_2 is fully discharged, *i.e.*, when voltage v_{S2} reaches zero, current i_1 begins flowing through antiparallel diode D_2 of switch S_2, as shown in Fig. 5(c). Due to negative voltage $V_{IN}/2$ applied across series connected resonant inductor L_{R1} and magnetizing inductance L_M of coupled inductor L_C, magnetizing current i_M decreases with a rate of approximately $(V_{IN}/2)/(L_M+L_{R1})$. At the same time, primary current i_P decreases in a resonant fashion. As a result, current $i_1=(i_P+i_M)/2$ decreases, whereas current $i_2=(i_P-i_M)/2$ increases. To achieve zero-voltage turn on of S_2, it is necessary to turn on S_2 while its antiparallel diode D_2 is conducting. In Fig. 6, S_2 is turned on immediately after v_{S2} has fallen to zero.

After $t=T_3$, when magnetizing current i_M becomes zero, its magnitude continues to increase in the negative direction, as shown in Fig. 5(d). As a result, current i_1 continues to decrease, whereas current i_2 continues to increase, as seen from waveforms in Figs. 6(m) and (n). At $t=T_4$, switch S_3 is turned off so that current i_2 is diverted from the transistor of switch S_3 to its output capacitance C_3, as shown in Fig. 5(e). During this transition C_3 is charging, while C_4 is discharging at the same rate, voltage v_{S3} increases from zero toward V_{IN}, whereas voltage v_{S4} decreases from V_{IN} to zero, as illustrated in Figs. 6(g) and (h). Also, since, during this topological stage, the potential of point B decreases from $V_{IN}/2$ to $-V_{IN}/2$ while the potential of point A is constant at $-V_{IN}/2$, voltage v_{AB} increases from $-V_{IN}$ to zero. To achieve ZVS of switch S_4, the switch needs to be turned on while its antiparallel diode is conducting, *i.e.*, during the T_5-T_6 interval. In Fig. 6, S_4 is turned on immediately after $t=T_5$, *i.e.*, immediately after v_{S4} falls to zero to minimize the conduction loss since the switch conduction loss is lower than the conduction loss of its antiparallel diode. At $t=T_6$, resonant primary current i_P changes direction from positive to negative, and the inverter enters the topological stage shown in Fig. 5(g). Because of resonant capacitor C_R connected in parallel with the load, the output voltage lags the primary current, *i.e.*, it is still positive at $t=T_6$. During the stage in Fig. 5(g), currents i_1 and i_2 continue to decrease. After current i_2 reaches zero at $t=T_7$, it continues to increase in the negative direction, as shown in Fig. 6(n). This topological stage, shown in Fig. 5(h), ends at $t=T_8$ when sinusoidal output voltage v_O crosses zero. During the next topological stage, shown in Fig. 5(i), the output voltage continues to resonate in the negative direction.

The second half of a switching cycle starts at $t=T_9$, when S_2 is turned off. If the switching frequency of the inverter is higher than the resonant frequency of the resonant-tank circuits, switch S_2 is turned off when currents i_1, i_2, and i_P are negative. As a result, after S_2 is turned off, negative current i_1 charges capacitance C_2 of switch S_2 and discharges capacitance C_1 of switch S_1, as shown in Fig. 5(j). During this switching transition, voltage v_{AB} increases from zero to V_{IN}, while primary voltage v_{AC} increases from $-V_{IN}/2$ to $V_{IN}/2$. This topological stage ends at $t=T_{10}$ when voltage v_{S1} across switch S_1 reaches zero and antiparallel diode D_1 of switch S_1 starts conducting current i_1, as shown in Fig. 5(k). To achieve ZVS of switch S_1, switch S_1 needs to be turned on while D_1 is conducting. In Fig. 6, switch S_1 is turned on immediately after v_{S1} has fallen to zero. Since, after switch S_2 is turned off, voltage v_{AB} starts increasing, magnetizing current i_M starts increasing as well, as can be seen from Fig. 6(l). At $t=T_{11}$, i_M becomes positive, as shown in both Fig. 5(l) and Fig. 6(l). Finally, at $t=T_{12}$ switch S_4 is turned off, which initiates switching transition in the S_3-S_4 leg. Because, during this transition, C_3 is discharging and C_4 is charging, the potential of point B is increasing from $-V_{IN}/2$ to $V_{IN}/2$. Since, during this time, the potential of point A is constant at $V_{IN}/2$, voltage v_{AB} is decreasing from V_{IN} to zero. At $t=T_{13}$ capacitance of switch S_3 is fully discharged and current i_2 begins flowing through antiparallel diode D_3 of switch S_3, as shown in Fig. 5(n). To achieve ZVS, switch S_3 is turned on shortly after D_3 starts conducting. During the topological stage in Fig. 5(n), primary current i_P, current i_1, and current i_2 continue to increase from negative values toward positive values, as seen from waveforms in Figs. 6(k), (m), and (n). Current i_1 becomes positive at $t=T_{14}$, whereas current i_2 becomes positive at $t=T_{15}$, which completes a cycle of operation of the circuit. The next switching cycle is initiated at $t=T_{17}$.

As can be seen from the waveforms in Fig. 6, the commutation of the switches in the S_1-S_2 leg is initiated when current $i_1 = i_2 + i_M = (i_P + i_M)/2$ is maximal, *i.e.*, when $i_1 = (i_P + I_M^+)/2$. Also, the commutation of the switches in the S_3-S_4 leg is initiated when current $i_2 = (i_P - i_M)/2$ is maximal, *i.e.*, when $i_2 = (i_P - I_M^-)/2 = (i_P + I_M^+)/2$. Therefore, in the proposed circuit, all primary switches are commutated with approximately the same magnitude current, which is a unique characteristic of the circuit. Specifically, the charging and discharging of the capacitances of switches in the S_1-S_2 leg is done by the sum of the energy stored in resonant inductor L_{R1} and the energy stored in the magnetizing inductance of coupled inductor L_C, whereas the charging and discharging of the capacitances of switches in the S_3-S_4 leg is done by the sum of the energy stored in L_{R2} and L_M. To achieve ZVS of the bridge switches, the sum of the energy stored in the magnetizing inductance of the coupled inductor and the energy stored in the resonant inductor of the corresponding bridge leg must be high enough to fully discharge the capacitance of the switch that is about to be turned on. Generally, this ZVS condition can be expressed as

$$\frac{1}{2}\left[\frac{1}{2}L_R i_P^2 + \frac{1}{2}L_M I_M^2\right] \geq CV_{IN}^2, \qquad (6)$$

where $C=C_1=C_2=C_3=C_4$ is the total capacitance across the primary switch, which, beside output capacitance C_{OSS} of the switch, also includes any externally added capacitance.

Since from Fig. 4, primary current i_P is

$$\vec{i}_P = \frac{1}{n}\cdot\vec{v}_O\left(\frac{1}{R_L} + \frac{1}{j\cdot 2\cdot\pi\cdot f_S\cdot C_R}\right), \qquad (7)$$

it can be seen that energy stored in resonant inductors L_{R1} and L_{R2} is dependent on the load, as well as resonant capacitor C_R. At no load ($R_L=\infty$), the primary current is the reflected current flowing through resonant capacitor C_R. This current represents the circulating current of the converter that is used to provide the energy required for the resonant inductors to achieve ZVS. In the proposed circuit, this circulating current can be minimized because all of the ZVS energy can be provided by the energy stored in the magnetizing inductance of the transformer. If the energy

stored in the magnetizing inductance is selected so that at the maximum input voltage $V_{IN(max)}$,

$$L_M I_M^2 \geq 4CV_{IN(max)}^2, \quad (8)$$

ZVS will be achieved in the entire load and input-voltage range regardless of the value of C_R.

The value of L_M required to achieve ZVS at no load can be calculated from Fig. 6 by observing that, during time interval T_{10}-T_{12}, magnetizing current i_M changes linearly from maximum negative value I_M=-I_M to maximum positive value I_{+M},=I_M, *i.e.*, i_M changes for 2I_M, due to a positive voltage of $V_{IN}/2$ impressed across the series connection of L_{R1} and L_C. From the equivalent circuit in Fig. 5(k), it can be derived that the rate of change of magnetizing current i_M during the T_{10}-T_{12} time interval is

$$\frac{di_M}{dt} = \frac{V_{IN}}{2L_M + L_R}, \quad (9)$$

where L_R=L_{R1}=L_{R2}.

Since, according to Fig. 6, the time interval T_{10}-T_{12} is approximately equal to

(1-D)T_S/2, where D is a duty cycle and T_S is a switching period, I_M can be calculated from

$$V_{IN} = (2L_M + L_R) \cdot \frac{2I_M}{(1-D)\frac{T_S}{2}} \quad (10)$$

as

$$I_M = \frac{(1-D)V_{IN}}{4 \cdot (2L_M + L_R) \cdot f_S}, \quad (11)$$

where f_S=1/T_S is the switching frequency. Since D≈0 at no load because the two bridge legs must be out of phase, the ZVS condition at no load and high line from Eqs. (8) and (11) is

$$L_M \cdot \left(\frac{V_{IN(max)}}{4 \cdot (2L_M + L_R) \cdot f_S} \right)^2 \geq 4CV_{IN(max)}^2. \quad (12)$$

Finally, from Eq. (12), the approximate value of L_M required to maintain ZVS at no load and high line is

$$L_M \leq \frac{1}{256Cf_S^2}, \quad (13)$$

assuming that 2L_M >> L_R.

As can be seen from Fig. 4, current i_M flowing through magnetizing inductance L_M introduces a current asymmetry in the two bridge legs. Namely, the coupling of windings DF and FE causes current i_2 flowing through winding FE to equal current i_3 flowing through winding DF, so that i_1=i_2+i_M. Therefore, in the proposed circuit, leading leg S_1-S_2 always carries a higher current than lagging leg S_3-S_4; the difference being magnetizing current i_M.

Since, in the circuit in Fig. 3, primary current i_P=i_1+i_2 is divided between the two bridge legs, *i.e.*, it is effectively carried by two parallel current paths, the minimum total conduction loss for the primary switches is obtained if equal currents flow through both legs of the bridge. With equal current distribution between the bridge legs, the total conduction loss of the bridge can be cut in half because the two conducting switches of the bridge carry only one half of primary current i_P. Therefore, to simultaneously achieve ZVS at no load and minimize the bridge conduction loss in the circuit in Fig. 3, it is necessary to select the maximum magnetizing inductance L_M determined by Eq. (13) so that the imbalance of the leg currents is minimized. Furthermore, if this minimized current imbalance is still significant, *i.e.*, if current i_2 in lagging lag S_3-S_4 is significantly lower than current i_1 in the leading leg S_1-S_2, different size switches can be selected for the two legs, which may reduce the cost of the implementation without sacrificing the circuit performance. Phase-shift control of the proposed circuit can be implemented with any of the commercially available phase-shift IC controllers.

III. Experimental Results

The performance of the proposed inverter circuit was verified on a 1-MHz, 230-W prototype circuit that was designed to operate from a 320 V - 400 V dc input and deliver 27-V_{RMS} ac output voltage. The experimental circuit was implemented with the following components: switches Q_1-Q_4 = IRF820, blocking capacitors C_{B1} and C_{B2} = 0.1 μF/400 V polypropylene capacitor, and resonant capacitor C_R = 56 nF multi-layer ceramic capacitor. The core of transformer TR is a combination of E22/6/16-3F4 and PLT22/16/2.5-3F4. The primary and secondary windings of transformer TR are five turns of Litz wire (150 strands, AWG #42) and a single turn of two parallel connected copper foils (width = 5mm, thickness = 7 mils), respectively. As shown in Fig. 7, resonant inductors L_{R1} and L_{R2} and coupled inductor L_C are integrated on the same core using two

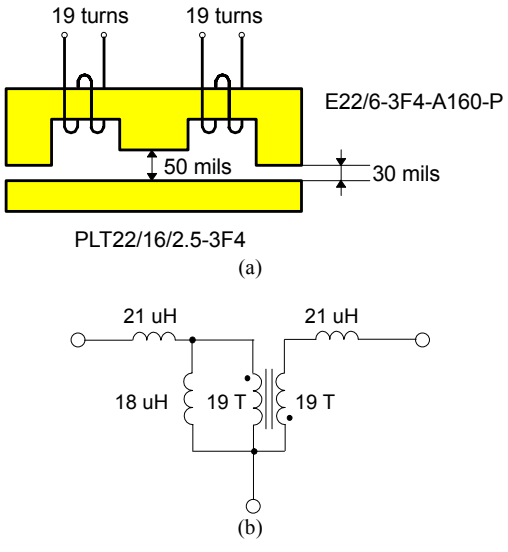

Fig. 7. Integrated magnetic which contains coupled inductor LC and resonant inductor L_{R1} and L_{R2}: (a) winding structure; (b) equivalent circuit diagram.

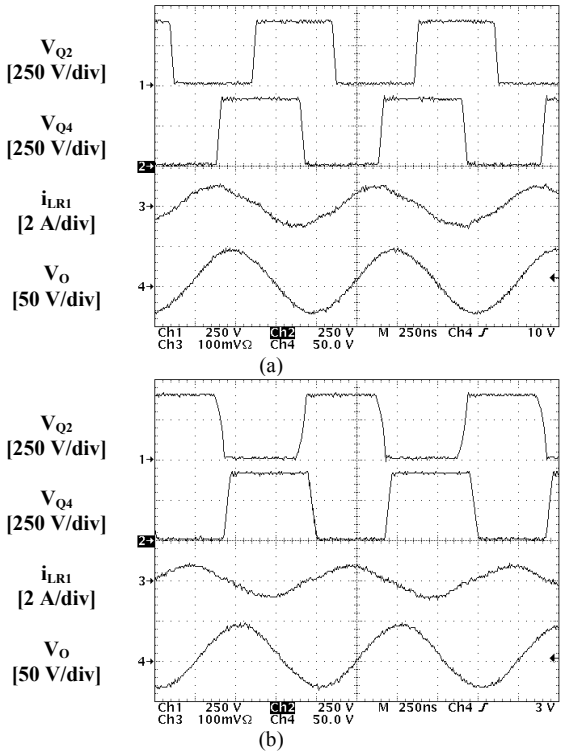

Fig. 8. Measured waveforms at V_{IN}=400 V, V_O=27.1 V_{RMS},: (a) P_O=230 W and (b) P_O=9.2 W. Time base: 250 ns/div.

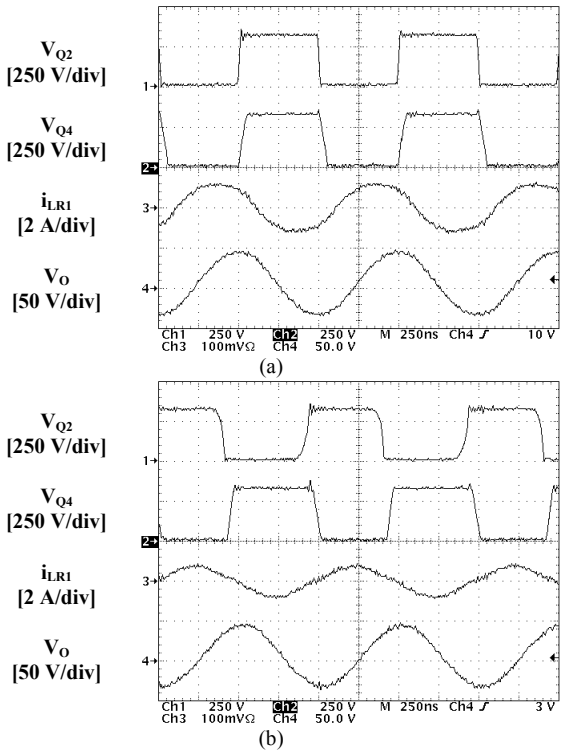

Fig. 9. Measured waveforms at V_{IN}=320 V, V_O=27.6 V_{RMS},: (a) P_O=230 W and (b) P_O=9.2 W. Time base: 250 ns/div.

windings with 19 turns each. In fact, the leakage inductance of the coupled inductor in Fig. 7 is utilized as resonant inductors L_{R1} and L_{R2}. The leakage inductance of the coupled inductor is adjusted so that L_{R1}=L_{R2} = 21 μH, whereas its magnetizing inductance L_M is approximately 18 μH. The control circuit was implemented with a constant-frequency phase-shift controller UC3875.

Figures 8 and 9 show the measured waveforms of the proposed inverter at full load and 4% load with 320 V and 400 V input voltage, respectively. All the switches operate with ZVS in all conditions. Moreover, the peak-to-peak current of the resonant inductor at 4% load is approximately 65% of that at the full load. As a result, the conduction loss at light load is approximately 42% of that at the full load. It should be noted that the peak-to-peak current of the resonant inductor in the conventional inverter at light load is often greater than that of the full load condition [8].

IV. Summary

A new constant-frequency dc-ac resonant inverter that employs a coupled inductor to achieve ZVS in the entire load and input voltage range with a reduced circulating current has been described. The performance of the proposed approach was evaluated on a 230-W inverter that delivers 1-MHz, 27-VRMS ac output voltage from a 320 V - 400 V dc input. The results shows all the switches operate with ZVS in all conditions. Moreover, the conduction losses at light loads are greatly reduced.

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