A Design Approach for Server Power Supplies for Networking Applications

Laszlo Huber and Milan M. Jovanović

Delta Products Corporation
Power Electronics Laboratory
P.O. Box 12173
5101 Davis Drive
Research Triangle Park, NC 27709

Abstract - Present specifications for computer power supplies for networking applications call for designs with dual inputs: the universal ac-line input and the 48-V nominal dc input. In this paper, a design and evaluation of the dc-input version of a 900-W server power supply is presented. The dc-input version of this power supply is leveraged from the ac-input version by using the same output stage, and by replacing the ac front-end in the ac-input version with a dc front end which provides the same input voltage to the output stage. By adopting this design approach, it is possible to achieve design modularity, design standardization, minimize the design time, optimize utilization of resources, and minimize the cost. The dc-input version uses a cascade connection of two dc boost converters because of its superior performance compared with other topologies.

I. INTRODUCTION

With a rapid growth of the Internet, telecom operators are aggressively adding new equipment to their networks so that they can use the existing telecom infrastructure to provide Internet services. This new equipment consists primarily of data processing and networking equipment such as servers, routers, and modems. This collocation of the data and telecom equipment has brought about new requirements for powering data processing equipment [1].

Generally, the computer and telecommunication industries employ different power system architectures because of different requirements on their reliability and availability performance, as well as reserve time in the case of an ac outage. The telecom industry uses a -48-V-bus distributed power system, which is backed up by a -48-V dc battery plant. The battery plant usually provides many hours of reserve time. The computer industry employs uninterruptible power supplies (UPSs) to provide reserve time during blackouts. Typically, an UPS system provides up to 30 minutes of the reserve time, which is by far much shorter than the reserve time required by telecommunication systems. As a result, powering of power supplies from the -48-V telecom dc bus is a natural choice for data processing equipment placed in the telecom environment. In fact, present specifications for power supplies for computers for networking applications already call for designs with dual inputs: the universal ac-line input and the 48-V nominal dc input.

The requirement for the dual input-voltage power supplies puts a significant burden on the power supplies manufacturers because of the additional efforts and resources necessary to design, manufacture, and handle two versions of a power supply. Furthermore, since presently the volume of the dc-input version is still a small fraction of the volume of the ac-input version, the additional engineering effort required for the design of the dc-input version might not pay off, unless the dc-input version design is done by leveraging the ac-input version design to the highest extent possible.

To minimize the effort and resources required for the design of a dual-input power supply for computers for networking applications, a maximally leveraged, modular design approach is proposed in this paper. In this approach, the ac- and dc-input versions of the power supply use different front ends and the same output stage, as shown in Fig. 1. Specifically, the ac-input version employs a PFC boost-converter front end, whereas the dc-input version uses a cascade connection of two dc/dc boost converters. The implementation with two cascaded boost converters was selected because of its superior performance compared with other topologies.

The proposed modular design does not require any redesign of the output stage since both front ends provide the same input voltage to the output stage, usually, 380 V. In addition, by physically separating the front end and the output
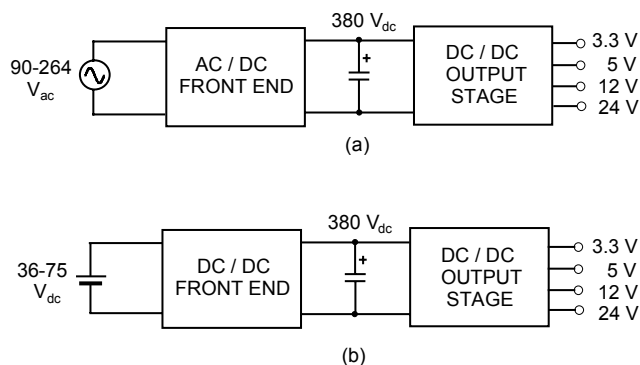

Fig. 1 Block diagram of (a) ac-input version and (b) dc-input version of computer power supplies for networking applications. Note that the dc/dc output stage is the same in both versions.
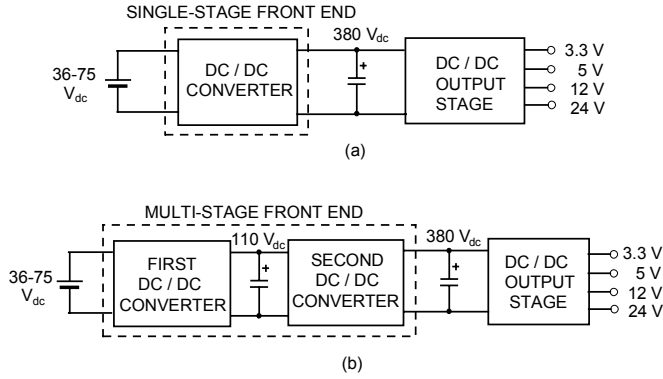
Fig. 2 Block diagram of dc-input version of computer power supplies for networking applications with (a) single-stage front end and (b) multi-stage front end.

stage by placing them on two separate printed circuit boards, and by providing the necessary interface between the boards through connectors, it is possible to achieve a modular design. Finally, the designs for both the ac and dc boost front ends can be standardized for a number of power levels. With standardized front-end modules, the design effort for the dual-input power supplies can be dramatically reduced.

The proposed modular approach with two cascaded dc/dc boost converters is evaluated on the dc-input front end for a 900-W server power supply for networking applications.

II. TOPOLOGY EVALUATION

Generally, the front-end in the dc-input version of computer power supplies for networking applications can be implemented as a single-stage or multi-stage converter as illustrated in Fig. 2. Since the safety isolation is achieved in the dc/dc output stage, the front end does not need to be isolated.

A. Single-Stage Front End

The simplest single-stage topology for the dc-input front end is the boost converter, shown in Fig. 3. Because of the 380-V output voltage, for boost switch Q_B, 500-V MOSFETs or IGBTs, and for boost diode D_B, 500/600-V fast-recovery diodes should be used. The maximum duty cycle, obtained at the minimum input voltage of $V_{imin} = 36$ V, is approximately 0.9. This large duty cycle results in a high current stress in the boost switch. Therefore, a hard-switched single-stage
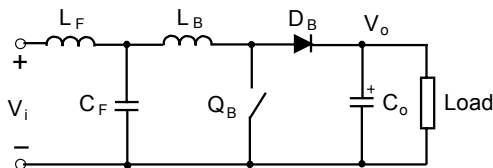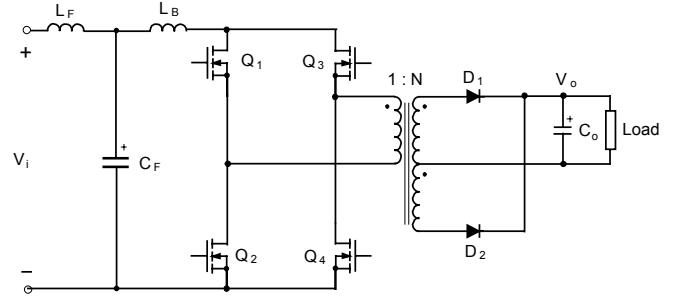

Fig. 4 Full-bridge isolated boost converter

boost converter could be employed only at lower output power levels, typically below 200-350 W, depending on the number of MOSFETs connected in parallel. With a passive snubber (e.g., [2]), the output power of the single-stage boost converter can be increased up to 350-400 W, whereas with an active soft-switching (e.g., [3]), the output power could be as high as 400-450 W.

To further increase the output power level, lower-voltage-rated MOSFETs should be used. Generally, the 150/200-V MOSFETs have a significantly lower on-state resistance than the 500-V MOSFETs. To achieve a lower voltage stress on the boost switch, the high output voltage seen by the boost switch in Fig. 3 has to be decreased through a transformer. A possible topology is the full-bridge isolated boost converter [4], shown in Fig. 4. Unfortunately, in this topology the voltage stress on the secondary-side diodes is doubled. As a result, less efficient 900/1000-V fast-recovery-type rectifiers must be used for D_1 and D_2 in Fig. 4. Due to a very high primary-side current at the minimum input voltage, the parasitic inductances of the circuit have a profound effect on the circuit's performance. Generally, the leakage inductance of the transformer as well as the parasitic inductances of the primary-side current traces should be minimized to reduce the ringing associated with these inductances.

B. Two-Stage Front End

The simplest two-stage topology for the dc-input front end is the cascade connection of two boost converters as shown in Fig. 5. If the intermediate voltage between the two boost stages is selected in the range $V_{o1} = 100$-125 V, then in the first stage 150-200 V MOSFETs and 150-200 V Schottky diodes can be employed. The Schottky diodes have two significant advantages over the corresponding fast-recovery

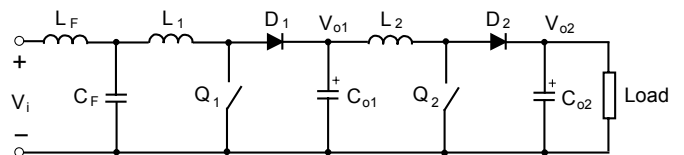Fig. 3 Basic boost converter

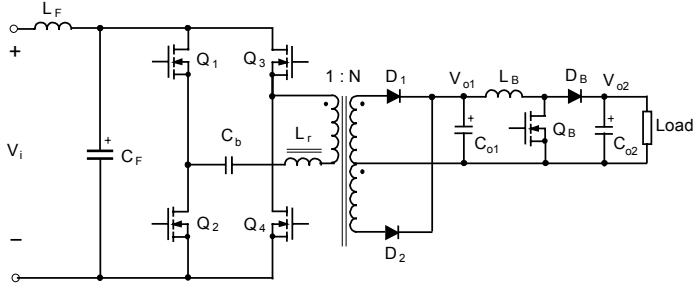
Fig. 5 Two cascaded boost converters

Fig. 6 Cascaded dc/dc transformer and boost converter

diodes: lower forward-voltage drop and no reverse recovery. At the same time, the second boost stage can be implemented as the corresponding PFC boost stage in the ac-input version. A boost converter supplied from a 100-125-V dc power source exhibits a similar efficiency as the corresponding PFC boost converter supplied from a 100-125-V_{rms} ac power source (typically, above 95%). Depending on the maximum output power level, two or three MOSFETs should be connected in parallel in both boost stages. Both boost stages can operate with hard switching. For improved performance, the second boost stage can be implemented with soft switching [2], [3].

At higher output power levels, typically above 1000-1500 W at the output of the front end, a possible alternative to paralleling of the MOSFETs is paralleling of the boost-converter modules, especially in the first boost stage. The paralleled modules can be interleaved, which significantly reduces the current ripple, and, therefore, the size of the filter at both the input and output of the converter. However, the interleaving of converters requires a more complex control circuit in order to achieve a good current sharing between the paralleled converters.

Another possible two-stage topology for the dc-input front end is the cascade connection of a dc/dc transformer as the first stage and the basic boost converter as the second stage, as shown in Fig. 6. The dc/dc transformer operates in open loop, with a constant duty cycle of approximately 50%. If the turns ratio of the transformer in Fig. 6 is selected as $N = 5$-5.5, then 100-150-V MOSFETs can be employed for switches Q_1-Q_4. For secondary-side rectifiers D_1 and D_2, 900/1000-V fast-recovery diodes should be used. Capacitor C_b in Fig. 6 is the blocking capacitor, which should be carefully selected because of the large rms value of the primary-side current. Inductor L_r in Fig. 6 represents the equivalent series inductance. Unfortunately, the dc/dc transformer stage in Fig. 6 suffers from a significant drawback. Because intermediate voltage V_{o1} is not regulated, at light loads voltage V_{o1} can significantly increase above the level determined by the product of the input voltage and the transformer's turns ratio. In fact, at light loads, inductor L_r operates in the discontinuous conduction mode (DCM). The initial value of the current through L_r at the beginning of each switching cycle is determined by the resonance between L_r

and the capacitance of rectifiers D_1 and D_2. To reset the current through L_r at light loads, voltage V_{o1} reflected to the primary side of the transformer has to be larger than the input voltage. At very light loads, the increase of voltage V_{o1} can become substantial. To limit this increase of V_{o1}, the initial value of the current through L_r has to be reduced. This can be achieved by increasing the value of L_r, i.e., by adding an extra inductor in series with the primary winding of the transformer. However, a smaller initial value of the current through L_r will result in a larger peak value of the primary current at full load. The problem of the uncontrolled increase of the intermediate voltage at light loads can be fully eliminated only by employing a more complex circuitry.

Generally, it can be concluded that the bridge-type topologies in Figs. 4 and 6 are less attractive than the single–or two-stage boost-converter topologies because they require an extra transformer, more complex control with high-side drivers, and must employ less-efficient and more-expensive high-voltage fast-recovery rectifiers.

III. DESIGN OF TWO CASCADED BOOST CONVERTERS

The design of the dc-input front end with two cascaded boost converters is illustrated on a 900-W server power supply for networking applications. The front end is designed for an input voltage range of $V_i = 40$-75 V, output voltage $V_{o2} = 375$ V, output power range of 50-1200 W, and hold-up time requirement of 8 msec at nominal input voltage $V_{inom} = 48$ V. It should be noted that the maximum output power of the front end (1200 W) is obtained by assuming 75% efficiency of the output stage of the 900-W server power supply.

A. Power Stage

In order to use 150-V power devices in the first boost stage, intermediate voltage V_{o1} in Fig. 5 should be designed to be in the range 100 V to 120 V. As V_{o1} increases, the efficiency of the first boost stage decreases while the efficiency of the second boost stage increases. Furthermore, as V_{o1} increases, the voltage stress on boost switch Q_1 and boost diode D_1 increases. The optimal value of intermediate voltage V_{o1} should be found experimentally. For the first design iteration, $V_{o1} = 110$ V was chosen. The two boost stages operate at the same switching frequency. Their operation should be synchronized in order to minimize the noise interaction between them. First, the design of the second boost stage is presented.

1) Second Boost Stage: The second boost stage is designed by leveraging the design of the corresponding PFC stage in the ac-input version of the power supply, i.e., by employing the same major components as in the corresponding PFC stage in the ac-input version. The same switching frequency, $f_S = 80$ kHz, was selected.

The maximum average input current of the second boost converter is

$$I_{i2ave\max} = \frac{P_{o2\max}}{\eta_2\, V_{i2}} = \frac{1200}{0.96\cdot110} = 11.36\,\text{A} \;,\qquad(1)$$

where $\eta_2 = 0.96$ is the assumed efficiency of the second boost stage. The duty cycle is obtained as

$$D_2 = 1 - \frac{V_{i2}}{V_{o2}} = 1 - \frac{110}{375} = 0.707 \;.\qquad(2)$$

From (1) and (2), the maximum rms current of boost switch Q_2 is

$$I_{Q2rms\max} = I_{i2ave\max}\sqrt{D_2} = 9.55\,\text{A} \;,\qquad(3)$$

and the maximum average current of boost diode D_2 is

$$I_{D2ave\max} = I_{i2ave\max}(1 - D_2) = 3.33\,\text{A} \;.\qquad(4)$$

Using the experience from the corresponding PFC stage in the ac-input version of the power supply, boost switch Q_2 is implemented with two IRFP22N50A (500 V, 22 A, 0.23 Ω, TO-247) power MOSFETs from IR connected in parallel, and diode D_2 is implemented with a single hyperfast diode with soft recovery characteristic RHRP3060 (30 A, 600 V, TO-220) from Harris. A 69-mm x 4-mm aluminum plate of 7" length with 10 fins (10 mm x 2 mm) is used as the heatsink.

The desired value of boost inductor L_2 is around 0.5 mH [3]. Boost inductor L_2 is implemented with two toroidal cores Kool Mμ 77071-A7 (Magnetics), each with 68 turns of copper wire AWG16.

The maximum rms ripple current through the output filter capacitor is obtained as

$$I_{Co2rms\max} = \sqrt{8.03^2\cdot0.293 + 3.33^2\cdot0.707} = 5.17\,\text{A} \;.\quad(5)$$

To handle this large ripple current, two paralleled aluminum electrolytic capacitors of 470 μF/450 V (Nippon Chemi-Con) are used. The two paralleled 470 μF/450 V capacitors also satisfy the 8-msec hold-up time requirement:

$$T_H = C_{o2}\cdot\frac{V_{o2nom}^2 - V_{o2\min}^2}{2\cdot P_{o2\max}} = 17.44\,\text{msec} \;,\qquad(6)$$

where $V_{o2\min} = 310\,\text{V}$ is used as in the corresponding PFC stage in the ac-input version. The actual hold-up time will be even longer because of the stored energy in the intermediate capacitor, C_{o1}.

2) First Boost Stage: The maximum average input current of the first boost converter is

$$I_{i1ave\max} = \frac{P_{o2\max}}{\eta_1\,\eta_2\, V_{i1\min}} = \frac{1200}{0.94\cdot0.96\cdot40} = 33.25\,\text{A} \;,\quad(7)$$

where $\eta_1 = 0.94$ is the assumed efficiency of the first boost stage. The variation of the duty cycle is from

$$D_{1\min} = 1 - \frac{V_{i1\max}}{V_{o1}} = 1 - \frac{75}{110} = 0.318 \;,\qquad(8)$$

to

$$D_{1\max} = 1 - \frac{V_{i1\min}}{V_{o1}} = 1 - \frac{40}{110} = 0.636 \;.\qquad(9)$$

From (7) and (9), the maximum rms current of boost switch Q_1 is

$$I_{Q1rms\max} = I_{i1ave\max}\sqrt{D_{1\max}} = 26.5\,\text{A} \;,\qquad(10)$$

and the maximum average current of boost diode D_1 is

$$I_{D1ave\max} = I_{i1ave\max}(1 - D_{1\max}) = 12.1\,\text{A} \;.\qquad(11)$$

Boost switch Q_1 is implemented with three IRF3415 (150 V, 43 A, 0.042 Ω, TO-220) power MOSFETs from IR connected in parallel, and diode D_1 is implemented with a single center-tap Schottky rectifier 30CPQ150 (30 A, 150 V, TO-247) from IR. A 69-mm x 4-mm aluminum plate of 7" length with 10 fins (10 mm x 2 mm) is used as the heatsink.

Boost inductor L_1 is designed to achieve a ripple current with an amplitude ($\Delta i_{L1}/2$) equal to 5-10% of the maximum average input current $I_{i1ave\max}$, i.e.,

$$\Delta i_{L1} = \frac{V_{i1\min}\, D_{1\max}}{L_1\, f_S} = (10\ldots20\%)\cdot I_{i1ave\max} \;.\qquad(12)$$

From (7), (9), and (12), it follows that the range of L_1 is

$$L_1 = \frac{40\cdot0.636}{(3.325\ldots6.65)\cdot80\text{k}} = 48\ldots96\,\mu\text{H} \;.\qquad(13)$$

Boost inductor L_1 is implemented with two pairs of toroidal cores Kool Mμ 77071-A7 (Magnetics), each pair with 23 turns of two strands of copper wire AWG14.

The maximum ripple current across the output filter capacitor, C_{o1}, is obtained as

$$I_{Co1rms\max} = \sqrt{21.15^2\cdot0.364 + 12.1^2\cdot0.636} = 16\,\text{A} \;.\,(14)$$

To handle this large ripple current, three paralleled aluminum electrolytic capacitors of 330 μF/160 V (Panasonic) and one metallized polyester film capacitor of 47 μF/150 V (Vishay) are used.

B. Control Circuit

Major issues of the control circuit design are the synchronization between the two boost PWM controllers, the voltage-mode control, and the employment of high-current gate drives to drive the paralleled MOSFETs.

An oscillator based on the integrated timer 555 generates the synchronization pulses and the ramp signal for the voltage-mode control. The PWM controllers of the two boost stages are built around the integrated controllers 3843. For driving the paralleled MOSFETs, the integrated MOSFET drivers 4420 are used.
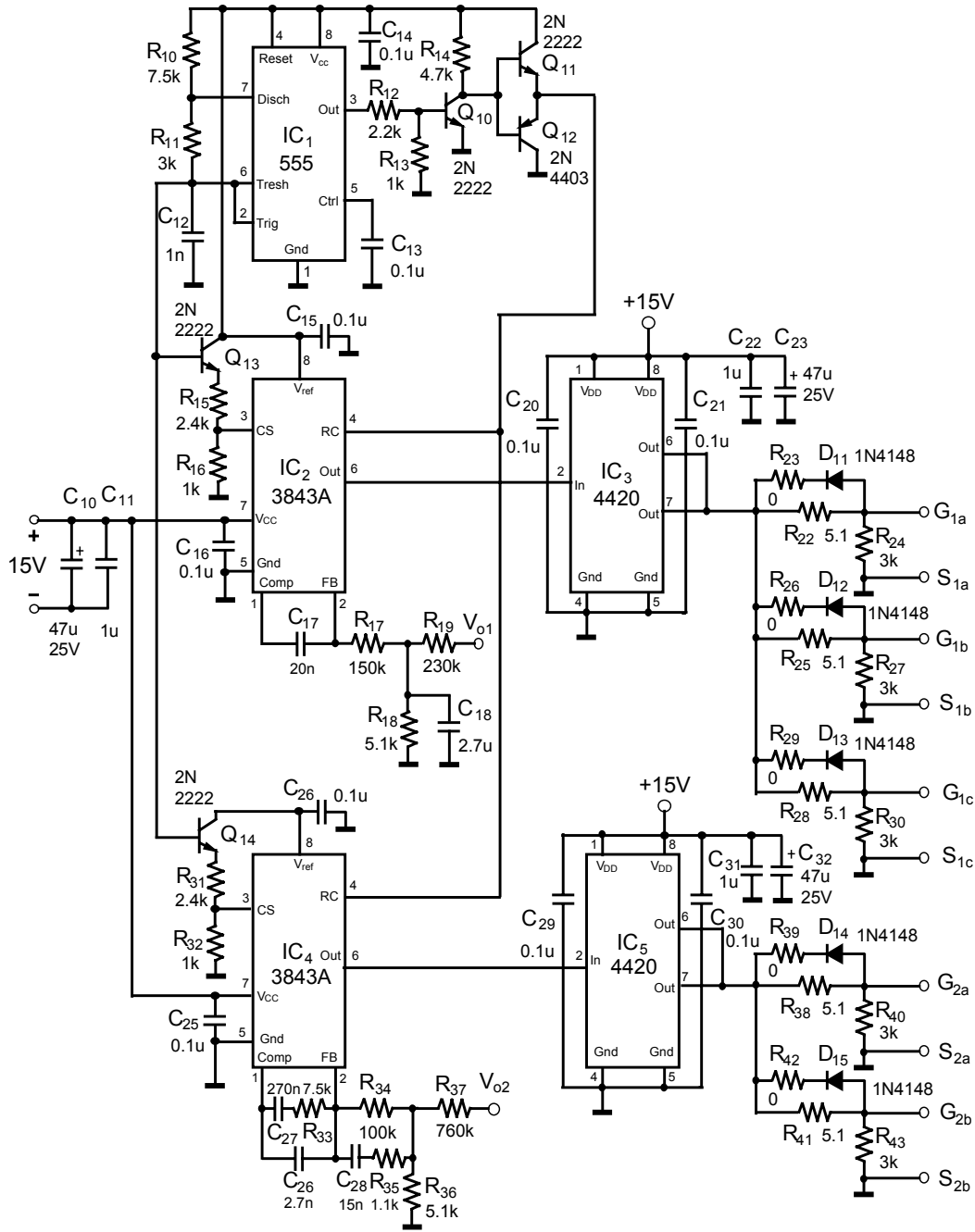
Fig. 7 Control circuit schematic

The schematic of the control circuit is shown in Fig. 7.

C. Layout

Major issues of the layout design are the requirement for a symmetrical layout of the paralleled MOSFETs and a proper connection between the power-ground plane and the control-ground plane.

IV. EXPERIMENTAL RESULTS

The measured performance of the two stand-alone boost stages is presented first. Tables I and II show temperature, voltage-stress, and efficiency measurements versus intermediate voltage V_{o1} at worst case (minimum input voltage and maximum load). As can be seen, with increasing voltage V_{o1}, the efficiency of the first boost stage decreases

while the efficiency of the second boost stage increases. At the same time, with increasing voltage V_{o1}, the voltage stress on the paralleled MOSFETs as well as on the diodes in the first boost stage increases while in the second boost stage it decreases.

TABLE I
MEASURED PERFORMANCE OF STAND-ALONE
FIRST BOOST STAGE
(V_{i1} = 40 V, P_{o1} = 1250 W, T_{amb} = 24°C)

V_{o1} [V]	$T(Q_{1a})$ [^{o}C]	$T(Q_{1b})$ [^{o}C]	$T(Q_{1c})$ [^{o}C]	$T(D_1)$ [^{o}C]	V_{DS1max} [V]	η_1 [%]
100	60	61	64	57	124	93.64
105	61	62	65	57	130	93.57
110	63	64	67	57	134	93.46
115	64	66	68	57	140	93.35
120	66	68	70	58	146	93.28

TABLE II
MEASURED PERFORMANCE OF STAND-ALONE
SECOND BOOST STAGE
(V_{o2} = 375 V, P_{o2} = 1200 W, T_{amb} = 24°C)

V_{i2} [V]	$T(Q_{2a})$ [^{o}C]	$T(Q_{2b})$ [^{o}C]	$T(D_2)$ [^{o}C]	V_{DS2max} [V]	η_2 [%]
100	78	82	71	484	94.71
105	72	76	67	480	95.19
110	68	72	64	476	95.51
115	64	68	62	472	95.88
120	61	65	60	470	96.09

TABLE III
MEASURED PERFORMANCE OF TWO CASCADED BOOST STAGES
(V_{i1} = 40 V, V_{o2} = 375 V P_{o2} = 1200 W, T_{amb} = 24°C)

V_{o1} [V]	$T(Q_{1a})$ [^{o}C]	$T(Q_{1b})$ [^{o}C]	$T(Q_{1c})$ [^{o}C]	$T(D_1)$ [^{o}C]	$T(Q_{2a})$ [^{o}C]	$T(Q_{2b})$ [^{o}C]	$T(D_2)$ [^{o}C]	η [%]
100	62	63	66	59	80	85	74	89.02
105	64	65	68	60	76	80	72	89.34
110	66	67	70	60	73	77	70	89.58
115	67	68	71	60	69	73	67	89.80
120	68	70	73	60	66	70	66	89.96

TABLE IV
MEASURED PERFORMANCE OF TWO CASCADED BOOST STAGES
(V_{o1} = 115 V, V_{o2} = 375 V P_{o2} = 1200 W, T_{amb} = 24°C)

V_i [V]	$T(Q_{1a})$ [^{o}C]	$T(Q_{1b})$ [^{o}C]	$T(Q_{1c})$ [^{o}C]	$T(D_1)$ [^{o}C]	$T(Q_{2a})$ [^{o}C]	$T(Q_{2b})$ [^{o}C]	$T(D_2)$ [^{o}C]	η [%]
40	67	68	71	60	69	73	67	89.80
48	55	56	58	53	68	72	66	91.67
60	46	47	49	48	67	71	65	93.02
75	44	44	45	45	67	70	65	93.75

Measured performance of the two cascaded boost stages versus intermediate voltage V_{o1} at worst case is shown in Table III. With increasing voltage V_{o1}, the total efficiency increases. It should be noticed that the total efficiency is slightly higher than the product of the efficiencies of the two stand-alone boost stages, which is mostly the result of the slightly reduced ripple current across the intermediate capacitor, C_{o1} in Fig. 5. All the temperatures in Table III are a few ^{o}C higher than the corresponding temperatures in Tables I and II, which is the result of the increased ambient temperature inside the power supply chassis due to a higher total power dissipation.

From Tables I-III, it can be concluded that the intermediate voltage should be selected as large as possible, by keeping enough safety margin of the maximum voltage stress on the MOSFETs and diodes in the first boost stage. It is a good design trade-off to select V_{o1} = 115 V. Full-load efficiency and temperature measurements at V_{o1} = 115 V for the entire

input voltage range V_i = 40-75 V are shown in Table IV. As can be seen, with increasing input voltage V_i, the temperature of the paralleled MOSFETs and the temperature of the Schottky diodes in the first boost stage significantly decrease (because the input current decreases) while the temperature of the paralleled MOSFETs and the temperature of the diode in the second boost stage are almost constant, i.e., they only slightly decrease which is the result of the slightly decreased ambient temperature inside the power supply chassis due to a lower total power dissipation.

If in some applications the temperatures of the power devices in the second boost stage are required to be lower than the values presented in Table IV, boost switch Q_2 could be implemented with three paralleled MOSFETs or the whole second boost stage could be implemented with a passive snubber or active soft switching. For example, by using the active soft switching technique presented in [3], the temperature of the power devices at T_{amb} = 24°C can be kept below 45°C, while the efficiency of the second boost stage can be improved by approximately 1%.

V. SUMMARY

A 1.2-kW, dc-input front-end for a 900-W server power supply for networking applications is implemented by using a cascade connection of two boost converters because of its superior performance compared with other topologies. The boost converter in the first stage boosts the input voltage in

the range of 40-75 V to 115 V, whereas the boost converter in the second stage gives an additional boost to 375 V. Due to a relatively low output voltage of the first boost stage, this stage is implemented with 150-V MOSFETs and Schottky rectifiers, which maximize the conversion efficiency. The second boost stage is implemented as the corresponding PFC boost stage in the ac-input version of the power supply. It was found that the overall efficiency of the two-stage boost-converter dc-input front end at low input voltage (40 Vdc) is approximately the same as the efficiency of the ac-input PFC boost converter at low line (85 Vac). It should be noted that at lower power levels, a single-stage boost converter is also a viable approach because it enables the minimization of the component count, size, and cost of the front end.

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