

Practical Issues of Input/Output Impedance Measurements in Switching Power Supplies and Application of Measured Data to Stability Analysis

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Abstract - Measurements of converter input and output impedances are conducted to verify that the power system has been correctly modeled and designed. Many impedance measurement setups presented in the past are useful for tutorial purposes, but in practice their application is limited to low-power supplies. This paper presents practical impedance measurement circuits, which provide reliable measurements for a wide class of power supplies. The measured impedance data was applied to stability analysis of the computer distributed power system.

I. INTRODUCTION

Due to increased performance demands in data-processing applications, distributed power systems (DPS) are becoming popular solution to power the next generation of information technology hardware. Typical DPS for computer applications consists of an off-line ac-dc power supply and several point-of-load (POL) converters. DPS design for stability and dynamic performance is a challenging task. Namely, ac-dc power supplies and POL converters are designed for predefined stand-alone input and load conditions, e.g., for an ideal input voltage source and a resistive load. However, the predefined conditions are hardly met in DPS. Therefore, the dynamic performance of the power converter within the DPS can be very different from that in the stand-alone operation. Specifically, each individual converter may have well-designed control loops in a stand-alone operation, but exhibit deteriorated performance within a DPS.

Generally, converter input and output impedances are used for verification of the power system stability and dynamic performance. Numerous impedance measurement setups were presented in [1]-[3], but they each suffer from different drawbacks. Setups in [2] have poor thermal stability of the measurement operating point. Other setups [1]-[2] do not provide excitation signals large enough for the measurement. Hence, in practice their applications are limited to low-current power supplies.

The purpose of this paper is to discuss the practical issues of input/output impedance measurements in switching power supplies and to propose suitable impedance measurement circuits which provide reliable data for a wide class of power supplies. Application of measured impedance data for

stability analysis is also discussed. The paper is organized as follows. Sections II and III explain limitations of the existing measurement setups and propose more practical circuits for measuring output and input impedances, respectively. Section IV describes applications of measured impedance data to stability analysis of the power systems. Section V summarizes the paper.

II. MEASUREMENT OF CONVERTER OUTPUT IMPEDANCE

Output impedance of the converter is defined as

$$Z_O = -\hat{V}_O / \hat{i}_O, \quad (1)$$

where small-signal voltages and currents are shown in Fig. 1.

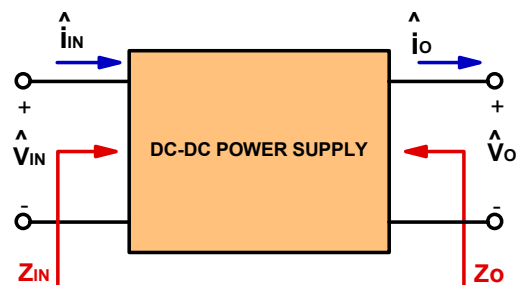


Fig. 1. Terminal voltages and currents of dc-dc power supply.

Output impedance is useful for analysis of the load transient response, system stability and source/load interactions. The magnitude and phase of output impedance are measured with a frequency-response analyzer. The principle of operation of a frequency-response analyzer is explained in [1] and [2]. Two typical setups for measuring the converter output impedance are shown in Figs. 2(a) and 2(b) [1]-[2]. Source $I_{O(DC)}$ in Fig. 2 is implemented by an electronic load operating in the constant-current mode. In both setups power supply output impedance is calculated based on V_{REF} and V_{TEST} signal measurements as

$$Z_O = -R_S \cdot \frac{V_{TEST}}{V_{REF}}, \quad (2)$$

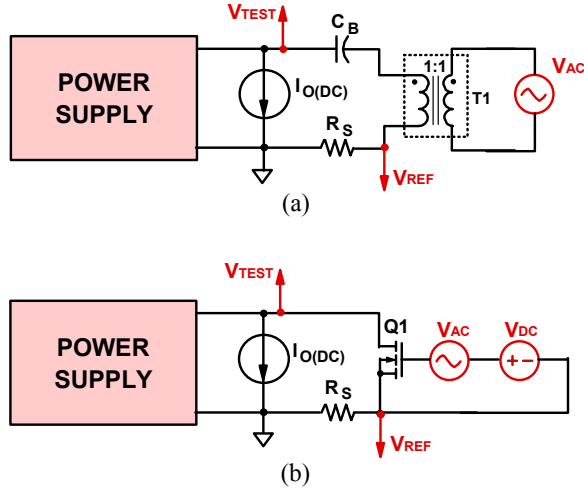


Fig. 2. Output impedance measurement circuits described in [1] and [2].

where R_S is the current sensing resistor value.

The major drawback of the circuit in Fig. 2(a) is the low magnitude of the injected current, which is limited by the relatively low power of the frequency-response analyzer sweep generator output signal V_{AC} . The circuit in Fig. 2(b) is free of this drawback since sweep generator output signal V_{AC} is amplified by MOSFET Q1. Therefore, it can be applied to output impedance measurement of high-current supplies. The disadvantage of this circuit is that device Q1 is powered by the power supply under test that prevents measurements while the power supply is turned off. Measurements while the power supply is off are meaningful for the following reason. For power supplies with a single-stage output filter, they show just the impedance of the filter output capacitor, which is easy to recognize. The impedance of the output capacitor is actually the high-frequency asymptote of the closed-loop output impedance of the operating power supply. Namely, output impedances of the turned-off and turned-on power supplies must coincide above both the resonant frequency of the output LC filter and the crossover frequency of the feedback loop. Therefore, impedance measurements of the turned-off power supply provide quite useful information, which helps to verify whether the measurement data for the turned-on power supply is valid. The second disadvantage of the circuit in Fig. 2(b) is poor thermal stability of Q1 operating point. Namely, the drain current of Q1 heavily depends on device transconductance G_M and gate threshold voltage V_{TH} that both change significantly with temperature.

The proposed circuit for output impedance measurement is shown in Fig. 3(a). As in the circuit in Fig. 2(a), a current is injected into the power supply output through transformer winding N_S and blocking capacitor C_{B2} . However, unlike the circuit in Fig. 2(a), the sweep generator signal V_{AC} is processed by a class A amplifier which includes device Q1, resistors R1-R5, blocking capacitors C_{B1} and C_{B2} , and

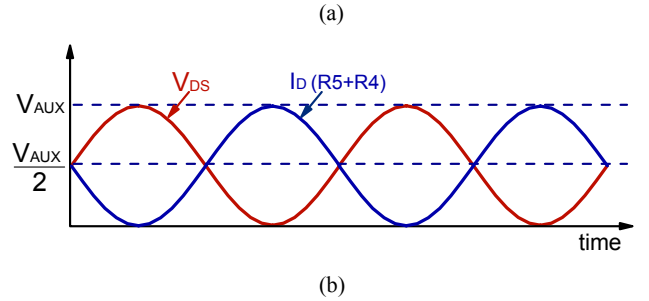
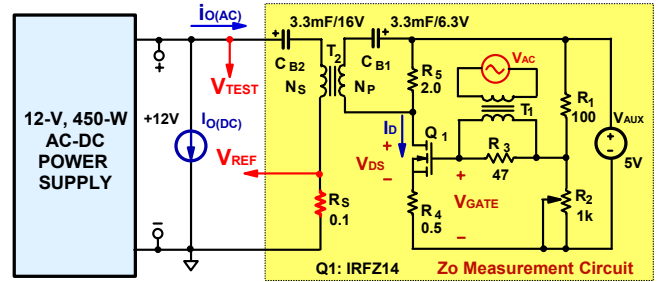


Fig. 3. Proposed circuit for output impedance measurement: (a) circuit diagram, (b) key waveforms.

transformer T2. Frequency-response analyzer output signal V_{AC} is coupled into the amplifier circuit through isolation transformer T1, which is often an accessory of commercial analyzers.

The design considerations for the measurement circuit are as follows. The purpose of resistor R3 is to maintain Q1 operating point when transformer T1 is disconnected from the circuit. Therefore, R3 value is quite arbitrary, but usually is selected in the range 20-100 Ω . Resistors R1, R2, and R4 set the dc drain current of transistor Q1. The purpose of resistor R4 is to provide thermal stability of the Q1 drain current. In the presence of R4, drain current I_D is related to gate voltage V_{GATE} as

$$I_D = \frac{G_M \cdot (V_{GATE} - V_{TH})}{1 + R_4 \cdot G_M} \quad (3)$$

Equation (3) clearly indicates that resistor R4 reduces sensitivity of the drain current to variation of device parameters G_M and V_{TH} . Practically, the voltage drop across R4 is selected to be comparable to voltage difference $(V_{GATE} - V_{TH})$.

The waveforms of the Q1 drain-source voltage and of the voltage across resistors R4 and R5 for the highest excitation signal level are shown in Fig. 3(b). Based on Fig. 3(b), it is evident that dc voltage drop $I_{D(DC)} \cdot (R_4 + R_5)$ is equal to half of the V_{AUX} magnitude and the peak value of the drain current ac component $I_{D(AC)}$ cannot exceed its dc value, i.e.

$$I_{D(AC)} \leq I_{D(DC)} = \frac{V_{AUX}/2}{R_4 + R_5} \quad (4)$$

To achieve $I_{D(AC)}=1A$ at $V_{AUX}=5V$, the sum of resistances $R4$ and $R5$ should be equal to 2.5Ω . The values of capacitors C_{B1} and C_{B2} are selected to provide much lower impedance for current $I_{D(AC)}$ than resistor $R5$ does. Namely,

$$\frac{1}{2 \cdot \pi \cdot f_{MIN} \cdot C_B} \ll R5, \quad (5)$$

where f_{MIN} is the lowest frequency of the measurement range. For example, for $f_{MIN}=100$ Hz and $R5=2 \Omega$, required blocking capacitor value should be much higher than $796 \mu F$. The values of resistive divider components $R1$ and $R2$ are selected to produce voltage $I_{D(DC)} \cdot (R4+1/G_M) + V_{TH}$ at the divider output.

Transformer T2 should be able to operate in the entire measurement frequency range, i.e., to have a wide bandwidth. Namely, the transformer must have high magnetizing inductance to operate in the low-frequency range and low leakage inductance to operate in the high-frequency range. The requirement of the low leakage inductance limits the number of winding turns. Therefore, to satisfy the requirement of high magnetizing inductance at low frequencies, a high-permeability core with a high cross-sectional area must be selected. To provide measurements in the 100 Hz – 1MHz range, transformer T2 was designed to have ETD-44-3F3 ferrite core and also single-layer primary and secondary windings of 85 turns of AWG #28 wire. Since dc currents through the transformer primary and secondary windings are blocked by capacitors C_{B1} and C_{B2} , no gapping of the transformer core is necessary. The measured magnetizing and leakage inductances of transformer T2 were 25 mH and 14 μH , respectively.

Finally it should be noted that MOSFET Q1 requires a heatsink which can handle $1/2 \cdot I_{D(DC)} \cdot V_{AUX}$ power dissipated in the device.

The designed measurement circuit in Fig. 3(a) with the component values shown in the Figure was powerful enough to excite the high-current power supplies with loads up to 50-75 A and successfully measure their output impedances.

As an example, the proposed circuit was applied to measure the output impedance of the 12-V output of the 450-W ac-dc power supply for a server computer. This power supply had a two-switch forward topology with a single-stage output filter and operated with current-mode control. The measured data, as well as the data calculated based on the analytical small-signal model [4], are presented in Fig. 4. Observation of calculated and measured plots in Fig. 4 indicates reasonable agreement between them.

The impedance of the turned-off power supply is also plotted in Fig. 4. Based on this plot, one can estimate the value of the output capacitance, its ESR and ESL. The low-frequency asymptote of the plot indicates output capacitance of 223 μF . The medium-frequency part of the plot suggests ESR of 20 m Ω . The estimated values of capacitance and ESR match the corresponding values of the physical output

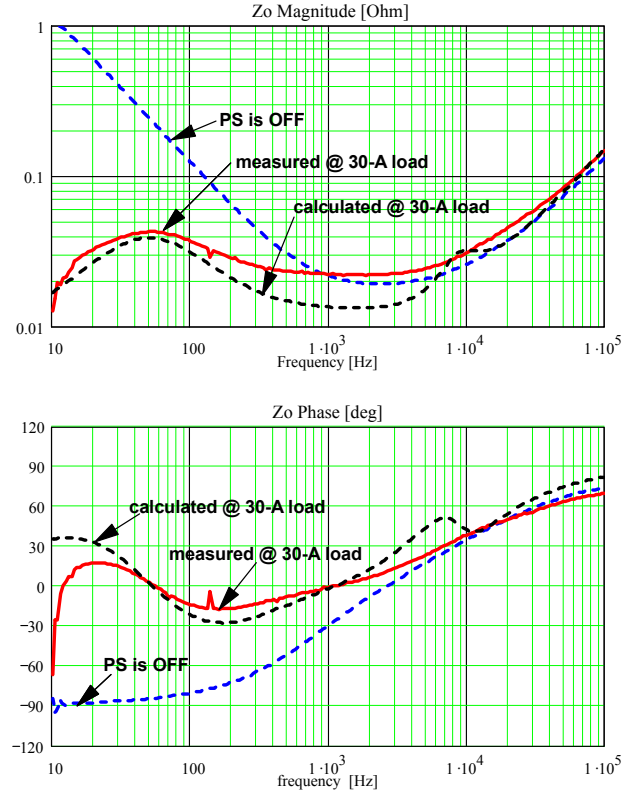


Fig. 4. Measured and calculated output impedance Z_o of 12-V, 450-W ac-dc power supply.

capacitor. However, the high frequency asymptote of the plot indicates ESL of 240 nH. The measured inductance value does not correspond to the actual ESL value of the output capacitor. This discrepancy is due to the additional parasitic inductances of wires and PCB traces, which connect the output capacitor to the measurement circuit. To minimize the effect of those parasitic inductances, the measurement circuit connections to the power supply output capacitor should be as short as possible.

Finally it should be noted that impedances of turned-off and turned-on power supply in Fig. 4 converge at high frequencies.

III. MEASUREMENT OF CONVERTER INPUT IMPEDANCE

Input impedance of the power supply is defined as

$$Z_{IN} = \hat{V}_{IN} / \hat{i}_{IN}, \quad (6)$$

where small-signal voltages and currents are shown in Fig. 1. Input impedance is useful for analysis of the system stability and source/load interactions. Two typical setups for measuring the converter input impedance, described in [2] and [3], are shown in Figs. 5(a) and 5(b). The major drawback of the circuit in Fig. 5(a) is that secondary winding N_s of injection transformer T_x carries considerable dc

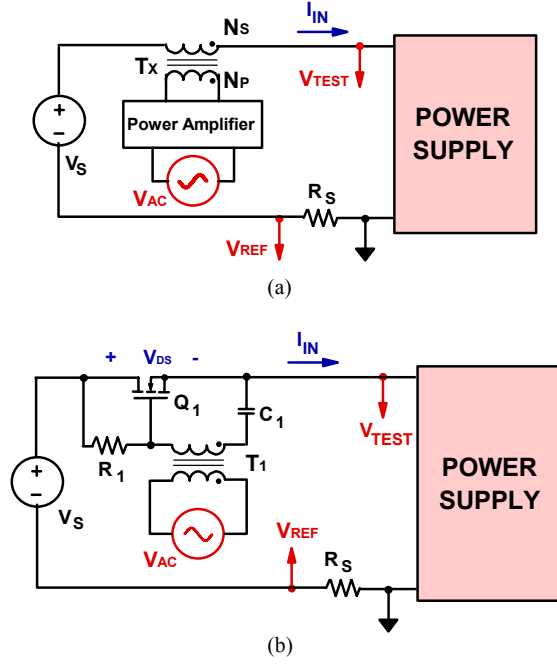


Fig. 5. Input impedance measurement circuits described in [2] and [3].

current, which magnetizes the core. Hence, to prevent inductor saturation, the core must be gapped. In the presence of the gap, the transformer magnetizing inductance dramatically decreases and, therefore, limits the lowest measurement frequency unless the size of the injection transformer is very large. The circuit in Fig. 5(b) has no additional magnetic components since transformer T1 is the accessory of the frequency-response analyzer. To inject the excitation signal into the power supply input voltage, measurement circuit uses MOSFET Q1 operating in the linear region. The voltage on capacitor C1 provides dc bias for Q1. The voltage drop across Q1 is governed by equation

$$V_{DS} = V_{TH} + I_{IN}/G_M. \quad (7)$$

Since parameters V_{TH} and G_M depend strongly on the device temperature, thermal stability of the measurement circuit operating point is poor.

The proposed circuit for input impedance measurement is shown in Fig. 6. The circuit represents a linear regulator whose reference is perturbed by a sweep generator signal V_{AC} through injection transformer T1. Due to negative feedback, a stable dc voltage across the power supply input terminals is maintained. Similarly to the output impedance computation, input impedance Z_{IN} is calculated based on V_{REF} and V_{TEST} signal measurements

$$Z_{IN} = -R_S \cdot \frac{V_{TEST}}{V_{REF}}. \quad (8)$$

Voltage divider resistors R1 and R2 determine the dc value of converter input voltage V_{IN} . Resistor R3 maintains the circuit operating point when transformer T1 is

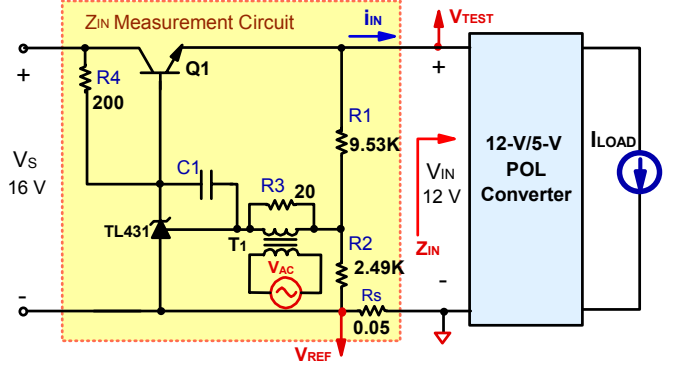


Fig. 6. Circuit for measuring input impedance of 12-V/5-V, 125-W POL converter.

disconnected from the circuit. R3 value is quite arbitrary and typically is selected in the range 20-100 Ω . The current through resistor R4 should supply the TL431 bias current I_{BIAS} and the Q1 base current, i.e.,

$$\frac{V_S - V_{IN} - V_{BE}}{R_4} \geq \frac{I_{IN}}{h_{FE}} + I_{BIAS}, \quad (9)$$

where V_S is the power source output voltage, V_{BE} and h_{FE} are the base-emitter voltage and current gain of transistor Q1, respectively. The TL431 bias current is typically selected in the range of 5-10 mA. For high-current supplies under test, it is recommended to select a Darlington transistor for Q1 to reduce the currents flowing through resistor R4 and TL431. Resistor R_S used for the current sensing should be of non-inductive type and be able to dissipate $I_{IN}^2 \cdot R_S$ power.

The value of capacitor C1 is determined by considering the trade-off between stability and high bandwidth of the linear regulator feedback loop. Since the value of capacitor C1 depends on the power supply under test, it is recommended to test the loop gain of the measurement circuit before starting the measurements.

The equivalent circuit and corresponding asymptotical Bode plots of a typical switching power supply are shown in Figs. 7(a) and 7(b), respectively. At low frequencies, power converter input impedance is a negative resistance, whose value is determined by the input voltage and the load. At higher frequencies, as can be seen in Fig. 7(b), the input impedance follows the impedance of the converter LC input filter.

The proposed measurement circuit was used to test the input impedance of a 12-V/5-V, 125-W POL converter. The measured and calculated Bode plots are shown in Fig. 8 and are in a good agreement. As predicted by the analytical model, at low frequencies the input impedance behaves like a negative resistance and at higher frequencies is shaped by the input filter impedance of the POL converter.

IV. APPLICATION OF MEASURED INPUT AND OUTPUT IMPEDANCES TO STABILITY ANALYSIS

The major application of measured input and output impedances is stability assessment of the integrated power system, which is based on interface stability criterion. Interface stability criterion was originally formulated in [5, 6] for the interface between the power converter and its input filter. Later this criterion was extended in [7] to include cascaded power systems. The interface stability criterion can be derived as follows. Suppose that the power system can be separated into independent source and load subsystems with corresponding terminal impedances Z_O and Z_{IN} , as shown in Fig. 9(a) along with small-signal perturbation source \hat{V}_S .

Then, voltage \hat{V}_B across load subsystem terminals is:

$$\hat{V}_B = \hat{V}_S \cdot \frac{Z_{IN}}{Z_O + Z_{IN}} = \hat{V}_S \cdot \frac{1}{1 + Z_O/Z_{IN}} = \hat{V}_S \cdot \frac{1}{1 + T_M} \quad (10)$$

where $T_M = Z_O / Z_{IN}$ is a minor loop gain. The corresponding block diagram in Fig. 9(b) clearly explains why T_M is considered a loop gain. For voltage \hat{V}_B to be stable, term $(1+T_M)$ in equation (6) must have no RHP poles. The absence of RHP poles in $(1+T_M)$ can be verified through the Nyquist analysis of open-loop gain T_M . Nyquist criterion calculates the number of RHP poles in term $(1+T_M)$ if the number of RHP poles in loop gain T_M is known. Practically it means that impedance Z_O and admittance $1/Z_{IN}$ should have no RHP poles, i.e., source and load subsystems must be stable in stand-alone operation. Namely, the source subsystem should be stable with the current-sink load and the load subsystem should be stable with the ideal voltage source input. Interface stability criterion is a powerful tool for stability analysis of a large class of power systems. However, it has a significant limitation of being applicable only to the independent source and load subsystems. One subsystem is independent of the other if it does not contain voltage or current sources dependent on the signals in the other subsystem. For example, Fig. 10 shows the buck converter with a two-stage output filter whose output voltage is sensed at the output of the filter second stage. In this case, the interface with corresponding impedances Z_O and Z_{IN} can be drawn between the first and second filter stages, as shown in Fig. 10. However, the resulting source and load subsystems are not independent, since the duty cycle d of the source subsystem depends on the signal in the load subsystem, namely, on output voltage V_O . Therefore, the interface stability criterion cannot be applied to the indicated interface.

It is also important to establish the frequency range in which the Nyquist plot should be constructed. Theoretically, the Nyquist plot should be constructed in the frequency range $0 < f < \infty$. This is not possible to accomplish because the frequency range of any practical measurement circuit is limited. In most cases, it is sufficient to construct the Nyquist plot up to the frequencies several times above the power

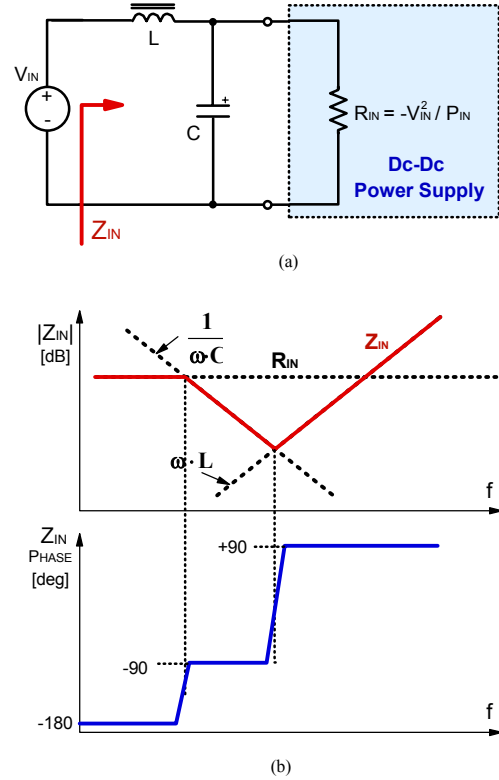


Fig. 7. Equivalent circuit and asymptotic input impedance of a switching power supply.

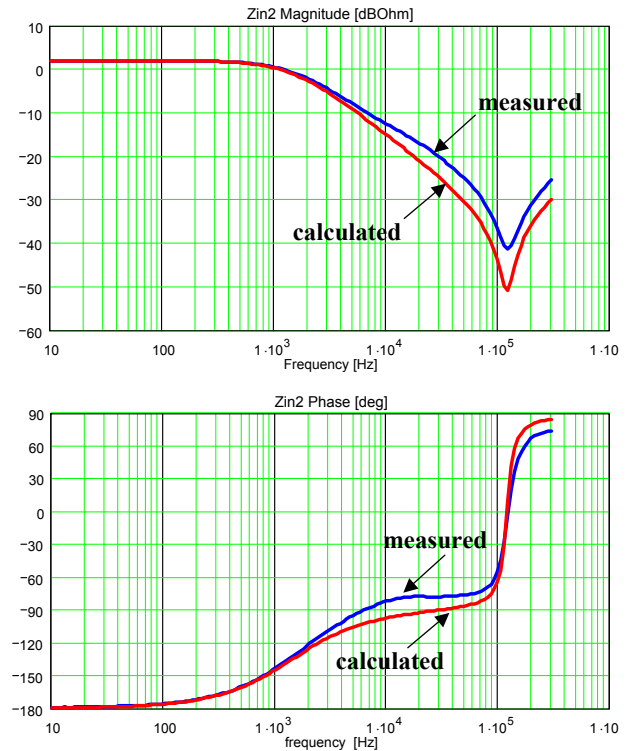


Fig. 8. Measured and calculated input impedance of 12-V/5-V, 125-W POL converter.

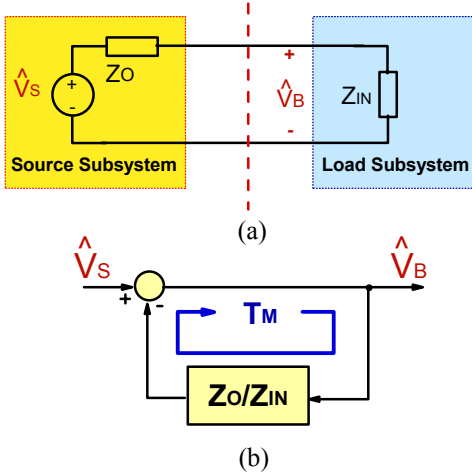


Fig. 9. Derivation of interface stability criterion.

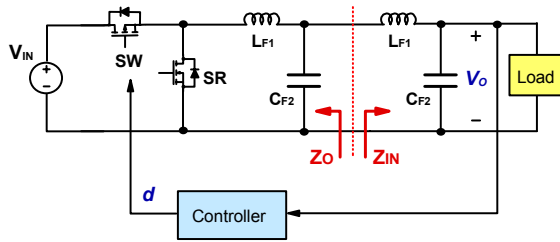


Fig. 10. Example of dependent source and load subsystems.

supply feedback loop gain crossover frequency. Beyond the loop bandwidth, the power supply becomes a passive circuit, which does not have a mechanism for sustained oscillations. In the case when the loop bandwidth is unknown, the impedance measurement should be conducted up to half of the power supply switching frequency.

The interface stability criterion was applied to stability analysis of a computer DPS that consists of an ac-dc converter with 12-V output and a 12V/5-V POL converter, separated by an EMI filter, as shown in Fig. 11. The parameters of the components on the system board in Fig. 11 are $C_B = 1000 \mu\text{F}$, $L_1 = 22 \mu\text{H}$, $C_1 = 33 \mu\text{H}$, $C_2 = 120 \mu\text{F}$, and $R_D = 0.5 \Omega$. Q factor of the EMI filter is $Q = R_D \cdot \sqrt{C_1/L_1} \approx 0.6$.

Prior to impedance measurement, stand-alone stability of both converters was tested in the time domain. Namely, ac-dc converter with the connected EMI filter was tested by applying a dynamic current-sink load to the EMI filter output. The POL converter was tested with the low-output-impedance laboratory power source and the dynamic current-sink load. The conducted tests demonstrated stand-alone stability of both ac-dc and POL converters.

Figure 12 shows measured impedances Z_o and Z_{IN} at the interface between the EMI filter and the POL converter. As can be seen in Fig. 12, the impedances overlap at frequencies

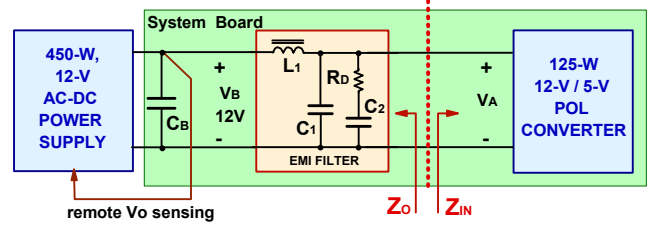


Fig. 11. Block diagram of computer distributed power system under consideration.

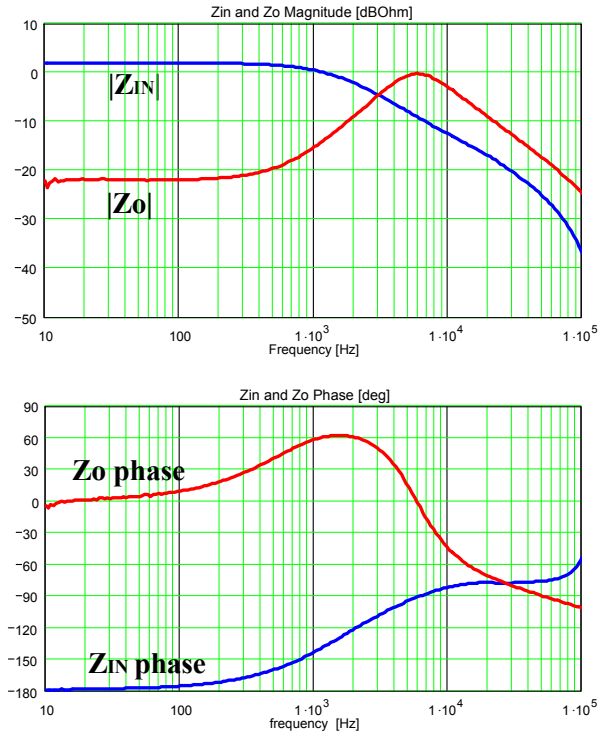


Fig. 12. Measured input and output impedances at the interface between the POL converter and EMI filter.

above 3 kHz. To determine the system stability, the construction of the T_M Nyquist plot is necessary. To select the frequency range of the Nyquist plot, it is important to know in advance switching frequencies and control bandwidths of the source and load converters. It was known from converter specifications, that the ac-dc power supply operates at 100-kHz switching frequency and has the control bandwidth of 3 kHz, whereas the POL converter operates at 600-kHz switching frequency and has the control bandwidth of 20 kHz. Based on this data, the highest frequency for the Nyquist plot construction was selected to be 100 kHz. The constructed T_M Nyquist plot is shown in Fig. 13. The arrow in Fig. 13 points in the direction of frequency increase. Examination of Fig. 13 reveals that, despite the overlap of impedances Z_o and Z_{IN} at high frequencies, the Nyquist plot does not encircle (-1,0) point. Therefore, the system is stable

V. SUMMARY

Input and output impedances carry important information about the power system dynamics. The most important application of the considered impedances is stability analysis of an integrated power system. The improved setups for measuring input and output impedances were proposed, which have thermally stable operating points and can be successfully applied to measurement of high-current power supplies. The example of stability assessment of the computer DPS in the frequency domain, based on measured impedances, was presented. The power system stability analysis was verified by testing the system in the time domain.

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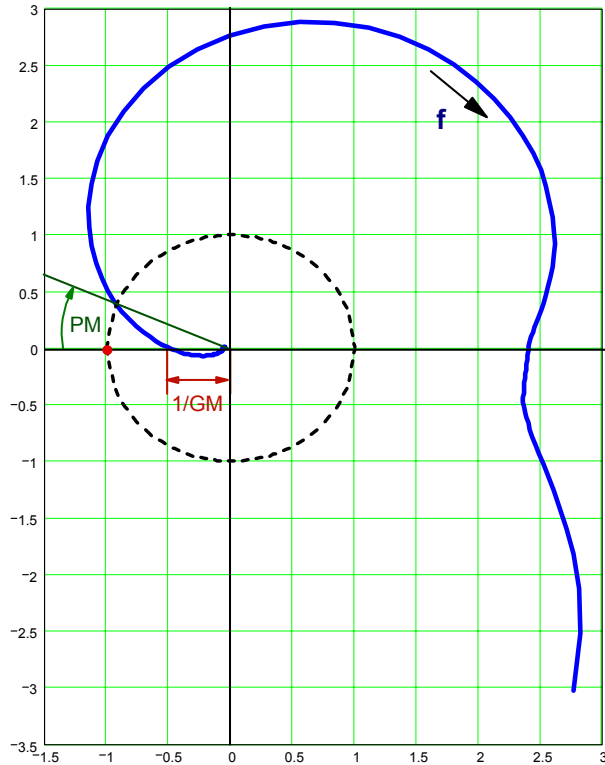


Fig. 13. Nyquist plot of loop gain T_M of computer distributed power system.

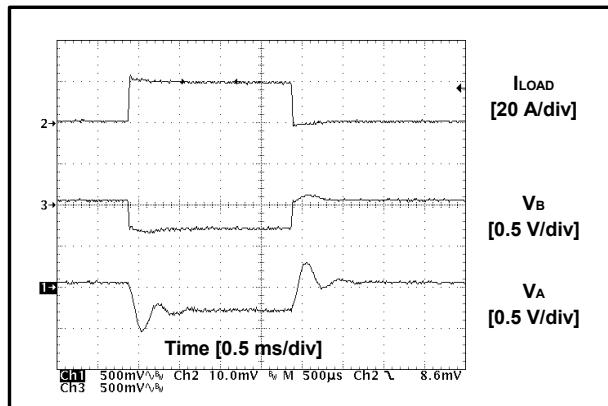


Fig. 14. Power system response to the load step at the output of the ac-dc converter.

with phase margin PM of 27° and gain margin GM of 6 dB, as shown in Fig.13.

Stability of the power system was tested in the time domain by applying the dynamic load across capacitor C_B in Fig. 11. The measured transient waveforms of load current I_{LOAD} , and of voltages V_B and V_A at the input and the output of the EMI filter are shown in Fig. 14. Convergence of voltages V_A and V_B with time to their steady-state values confirms the conclusion about system stability, based on the frequency-domain analysis.