

# Isolated Boost Converters

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**Abstract** — Two implementations of the isolated boost converter that exhibit no parasitic voltage ringing across all semiconductor devices on the primary and secondary sides of the transformer are introduced. Ringing-free operation is achieved by clamping the voltages of the primary switches and rectifiers to the voltage of the primary-side energy-storage capacitor and clamping the voltage across the secondary-side rectifiers to the output filter capacitor. The performance of the proposed topology was verified on a dual ac-input, 900-W experimental prototype operating at 100 kHz.

## I. INTRODUCTION

The conventional non-isolated boost converter topology has been extensively used in various ac/dc and dc/dc applications. In fact, the front end of today's ac/dc power supplies with power-factor correction (PFC) is almost exclusively implemented with the boost topology. The boost topology is also used in numerous battery-powered applications to generate a high output voltage from a relatively low battery voltage.

However in some applications, it may be advantageous to use a boost converter with a galvanically isolated input and output. For example, fault tolerant power systems that use a dual ac-input architecture can be implemented with isolated boost converters, [1], [2]. In fact, the isolated-boost-converter implementation offers a reduced number of components compared to the implementations with non-isolated boost converters in applications which require dual ac input [2]. Also, in applications where a power supply with both ac and dc inputs is required, the isolated boost converter can be applied to provide safety-required isolation between the inputs.

So far, a number of boost topologies utilizing an isolation transformer have been proposed, [3]-[8]. Generally, these circuits exhibit increased voltage stresses on the switches and/or diodes due to the parasitic ringing of the leakage inductance of the transformer with the output capacitances of the switching devices. To control the parasitic ringing voltage, these converters rely on various snubbers, which have detrimental effect on their efficiency and also limit their switching frequency.

In this paper, a two-switch implementation and a three-switch implementation of an isolated boost converter that exhibits voltage waveforms without parasitic voltage ringing across all semiconductor devices on the primary and secondary sides of the transformer are introduced. Ringing-free operation in the presence of the transformer's leakage

inductance is achieved by clamping the voltages of the primary switches and rectifiers to the voltage of the primary-side energy-storage capacitor and clamping the voltage across the secondary-side rectifiers to the output filter capacitor.

## II. ISOLATED BOOST CONVERTERS

The circuit diagram of the proposed two-switch isolated boost converter is shown in Fig. 1. The primary side consists of boost inductor  $L_B$ , switches  $S_1$  and  $S_2$ , primary-side energy-storage capacitor  $C_B$ , rectifiers  $D_1$  through  $D_4$ , and the primary winding of transformer TR. The output side of the circuit consists of the secondary winding of transformer TR connected to the full-bridge rectifier implemented with rectifiers  $D_{R1}$  through  $D_{R4}$ , and capacitive filter  $C_F$  connected across load  $R_L$ .

To facilitate the explanation of the circuit operation, Fig. 2 shows a simplified circuit diagram of the circuit in Fig. 1. In the simplified circuit, energy-storage capacitor  $C_B$  and filter capacitor  $C_F$  are modeled by voltage sources  $V_B$  and  $V_O$ , respectively, by assuming that the values of capacitors  $C_B$  and  $C_F$  are large enough so that the voltage ripple across the capacitors are small compared to their dc voltages. In addition, isolation transformer TR is modeled by leakage inductance  $L_{LK}$ , magnetizing inductance  $L_M$ , and an ideal transformer with turns ratio  $n=N_p/N_s$ , where  $N_p$  is the number of turns of the primary winding and  $N_s$  is the number of turns of the secondary winding. Finally, in this analysis it is also assumed that all semiconductor components represent zero impedances in the on state and infinite impedances in the off state.

To further facilitate the analysis of operation, Fig. 3 shows the topological stages of the circuit in Fig. 1 during a switching cycle, whereas Fig. 4 shows its key waveforms assuming that the inductance of boost inductor  $L_B$  is large enough to keep input current  $i_{IN}$  continuously flowing. The

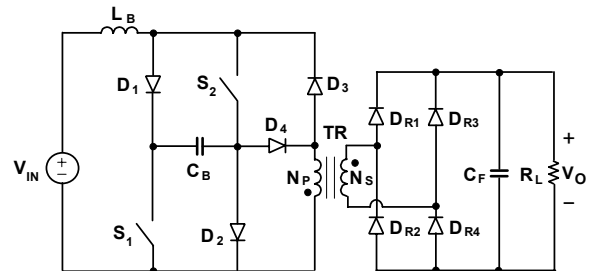


Fig. 1. Proposed two-switch implementation of isolated boost converter.

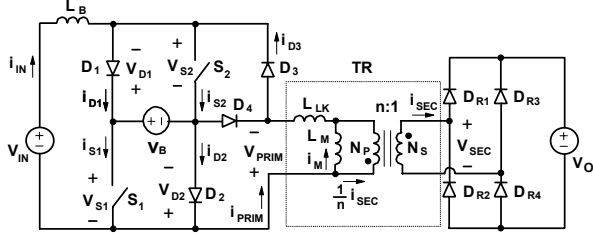


Fig. 2. Simplified circuit diagram of proposed converter with reference directions of voltage and currents.

reference directions of currents and voltages plotted in Fig. 4 are shown in Fig. 2.

As can be seen from the timing diagram of the control signals for switches  $S_1$  and  $S_2$  shown in Fig. 4, switches  $S_1$  and  $S_2$  of the proposed circuit are simultaneously turned on and off. The on time of the switches defines duty cycle  $D$  of the converter, as indicated in Fig. 4.

During the time interval when switches  $S_1$  and  $S_2$  are open, input current  $i_{IN}$  flows through diodes  $D_1$  and  $D_2$ , as shown in Fig. 3(a). Assuming that at  $t=T_0$ , transformer TR is completely reset, *i.e.*, magnetizing current  $i_M(t=T_0)=0$ , no other current is flowing in the circuit during the time interval from  $t=T_0$  until switches  $S_1$  and  $S_2$  are turned on at  $t=T_1$ . Since voltage  $V_B$  is always greater than input voltage  $V_{IN}$  (since it is the boost topology), input current  $i_{IN}$  is decreasing with a constant slope during the  $[T_0 - T_1]$  interval, as shown in Fig. 4. As a result, diode currents  $i_{D1}$  and  $i_{D2}$  are also decreasing, *i.e.*,

$$\frac{di_{D1}}{dt} = \frac{di_{D2}}{dt} = \frac{di_{IN}}{dt} = \frac{V_{IN} - V_B}{L_B} < 0 \quad (1)$$

After switches  $S_1$  and  $S_2$  are closed at  $t=T_1$ , input current  $i_{IN}$  is diverted from diodes  $D_1$  and  $D_2$  to switches  $S_1$  and  $S_2$ , as illustrated in Fig. 3(b). At the same time, primary current

$i_{PRIM}$  and secondary current  $i_{SEC}$  start to flow because voltage source  $V_B$  appears in parallel with the primary of the transformer when switches  $S_1$  and  $S_2$  are closed and diode  $D_3$  is forward biased, *i.e.*,  $V_{PRIM}=V_B$ . Since during the  $[T_1 - T_2]$  interval secondary voltage  $V_{SEC}$  is positive, secondary current  $i_{SEC}$  is carried by rectifiers  $DR_1$  and  $DR_4$ . From Fig. 3(b), secondary current  $i_{SEC}$  during the  $[T_1 - T_2]$  interval can be calculated as

$$i_{SEC} = n \cdot [i_{PRIM} - i_M], \quad (2)$$

where primary current  $i_{PRIM}$  and magnetizing current  $i_M$  are

$$i_{PRIM} = \frac{V_B - nV_O}{L_{LK}} \cdot t, \quad (3)$$

$$i_M = \frac{nV_O}{L_M} \cdot t, \quad (4)$$

*i.e.*,

$$i_{SEC} = n \cdot \left[ \frac{V_B - nV_O}{L_{LK}} - \frac{nV_O}{L_M} \right] \cdot t. \quad (5)$$

From Eqs. (2)-(4), it can be seen that during the  $[T_1 - T_2]$  interval, primary current  $i_{PRIM}$ , magnetizing current  $i_M$ , and secondary current  $i_{SEC}$  increase linearly beginning from zero at  $t=T_1$ , as illustrated in Fig. 4. In addition, during this interval, input current  $i_{IN}$  also increases with a slope of

$$\frac{di_{IN}}{dt} = \frac{V_{IN} + V_B}{L_B}. \quad (6)$$

At  $t=T_2$ , switches  $S_1$  and  $S_2$  are simultaneously open so that the current flowing through the switches starts charging output capacitances  $C_{OSS1}$  and  $C_{OSS2}$  of switches  $S_1$  and  $S_2$ , as shown in Fig. 3(c). During this stage, switch voltages  $V_{S1}$  and  $V_{S2}$  increase toward  $V_B$ , whereas diode voltages  $V_{D1}$  and  $V_{D2}$  decrease toward zero at the same rate, as illustrated in Fig. 4. Due to decreasing primary voltage  $V_{PRIM}$ , the rising rate of primary current  $i_{PRIM}$  also decreases causing a corresponding decrease in the rising rate of secondary current

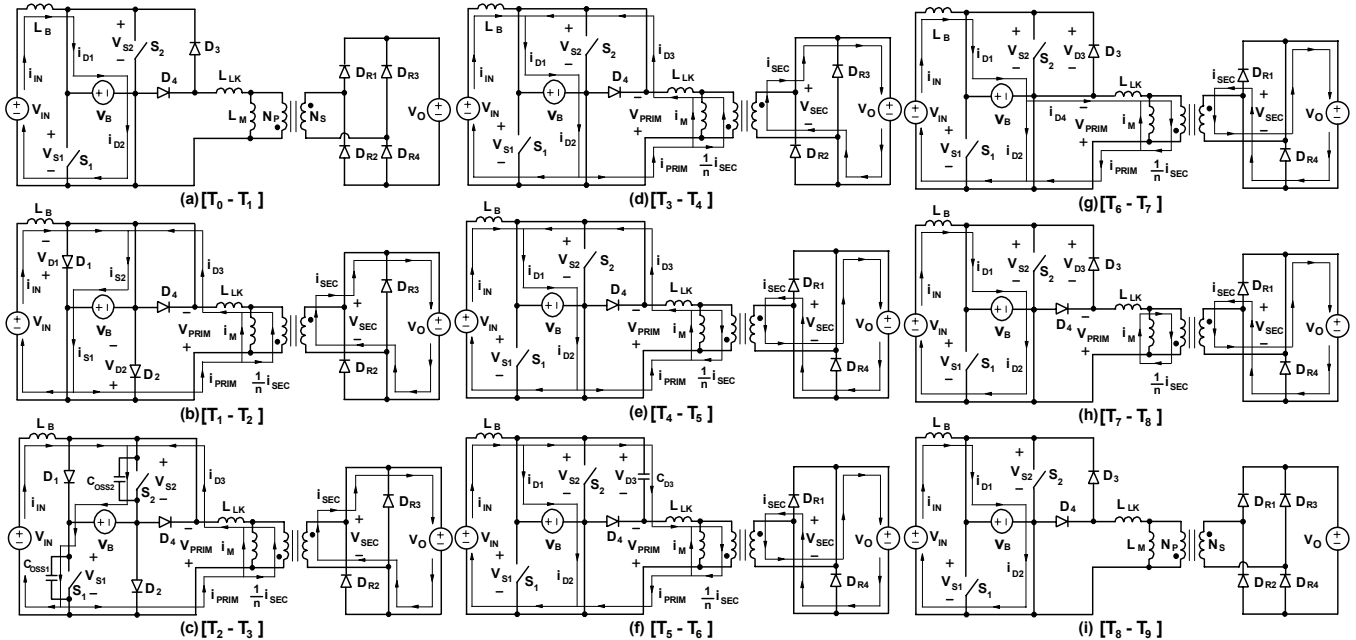


Fig. 3. Topological stages of proposed two-switch isolated boost converter.

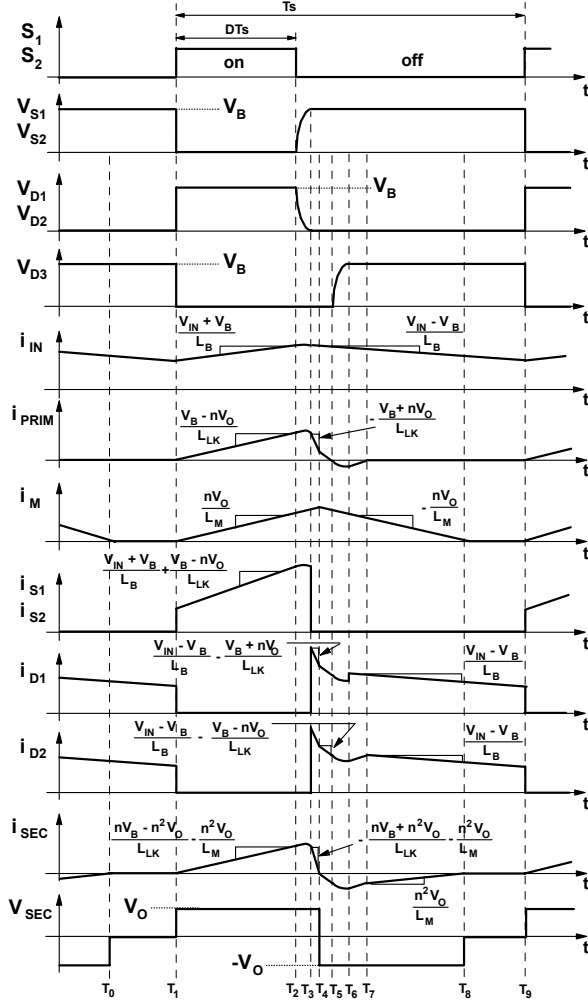


Fig. 4. Key waveforms of circuit in Fig. 1 operating in CCM.

$i_{SEC}$ . It should be noted that magnetizing current  $i_M$  continues to increase during this topological stage at the same rate as in the previous topological stage since the voltage across  $L_M$  is unchanged, *i.e.*, it is still  $nV_O$ . This stage ends at  $t=T_3$  when capacitances  $C_{OSS1}$  and  $C_{OSS2}$  are charged to  $V_B$  and diodes  $D_1$  and  $D_2$  start conducting, as shown in Fig. 3(d).

After  $t=T_3$ , the connection of voltage source  $V_B$  to input voltage source  $V_{IN}$  changes its polarity so that input current  $i_{IN}$  decreases linearly with the slope given by Eq. (1). In addition, since during this topological stage primary voltage is negative, *i.e.*,  $V_{PRIM}=-V_B$ , primary current  $i_{PRIM}$  also decreases linearly with a slope of

$$\frac{di_{PRIM}}{dt} = -\frac{V_B + nV_O}{L_{LK}}. \quad (7)$$

Because both  $i_{IN}$  and  $i_{PRIM}$  decrease linearly, diode currents  $i_{D1}$  and  $i_{D2}$  also decrease linearly, as illustrated in Fig. 4. The topological stage in Fig. 3(d) ends at  $t=T_4$  when primary current  $i_{PRIM}$  becomes equal to magnetizing current  $i_M$ , *i.e.*, secondary current  $i_{SEC}$  is decreased to zero.

As shown in Fig. 3(e), after  $t=T_4$ , secondary current  $i_{SEC}$  flows in the negative direction through rectifiers  $D_{R2}$  and  $D_{R3}$ ,

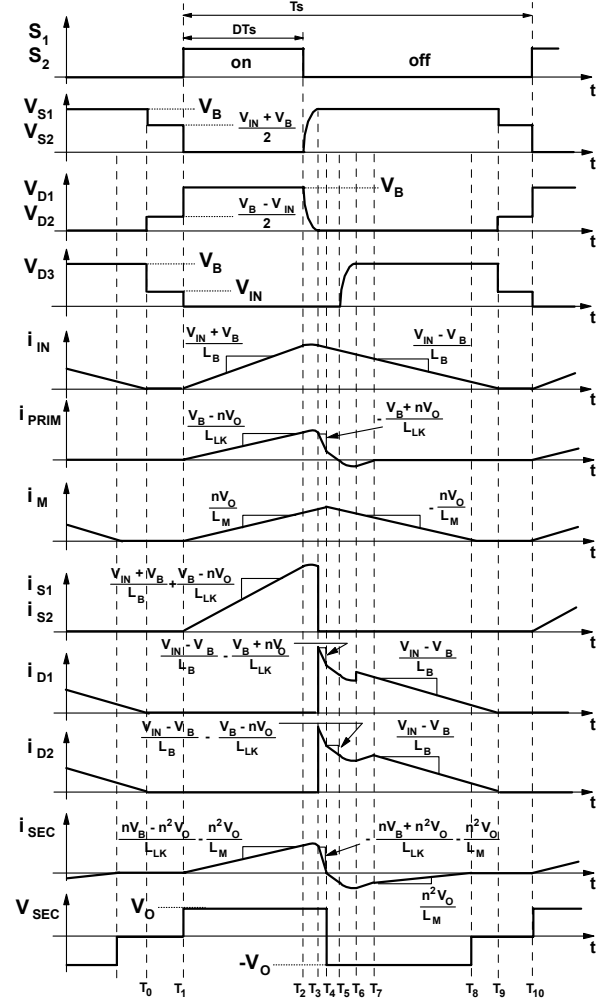


Fig. 5. Key waveforms of circuit in Fig. 1 operating in DCM.

while primary current  $i_{PRIM}$  continues to flow through diode  $D_3$ . Because of the reverse polarity of the voltage across the secondary winding during this topological stage, the rate at which the primary current decreases toward zero is reduced to

$$\frac{di_{PRIM}}{dt} = -\frac{V_B - nV_O}{L_{LK}} < 0. \quad (8)$$

At  $t=T_5$ , when primary current  $i_{PRIM}$  falls to zero, diode  $D_3$  ceases conducting so that diode's junction capacitance  $C_{D3}$  starts to resonate with leakage inductance  $L_{LK}$ , as shown in Fig. 3(f). During this resonance, primary current  $i_{PRIM}$  that is flowing in the negative direction charges junction capacitance  $C_{D3}$  toward  $V_B$ , as illustrated in Fig. 4. The negative peak of  $i_{PRIM}$  occurs at  $t=T_6$  when voltage  $V_{D3}$  reaches  $V_B$  and clamp diode  $D_4$  starts conducting, providing a path for primary current  $i_{PRIM}$ , as shown in Fig. 3(g). The magnitude of the negative peak of  $i_{PRIM}$  is given by

$$i_{PRIM}^{PK(NEG)} = \frac{V_B - nV_O}{\sqrt{L_{LK}/C_{D3}}}. \quad (9)$$

During the topological stage in Fig. 3(g), primary current  $i_{PRIM}$  increases linearly from the peak negative current given

in Eq. (9) toward zero. When  $i_{\text{PRIM}}$  becomes zero at  $t=T_7$ , diode  $D_4$  stops conducting and residual magnetizing current  $i_M$  continues to flow through the secondary, as shown in Fig. 3(h), until it is completely reset at  $t=T_8$ , as illustrated in Fig. 4. The next switching cycle is initiated at  $t=T_9$  when switches  $S_1$  and  $S_2$  are turned on again.

According to the presented analysis of operation, in the proposed circuit, the energy stored in primary energy-storage capacitor  $C_B$  is transferred to the load during the time interval switches  $S_1$  and  $S_2$  are closed, *i.e.*, during the  $[T_1 - T_2]$  interval in Fig. 4. In addition, during this interval, energy stored in boost inductor  $L_B$  is increasing. When switches  $S_1$  and  $S_2$  are open, the energy stored in the boost inductor  $L_B$  is transferred to primary-side energy-storage capacitor  $C_B$ , while the load current is supplied by output filter capacitor  $C_F$ .

Based on the volt-second balance on the boost inductor, energy-storage capacitor voltage  $V_B$  is related to input voltage  $V_{\text{IN}}$  as

$$V_B = \frac{1}{1-2D} \cdot V_{\text{IN}}, \quad (10)$$

where  $D$  is the duty cycle of switches  $S_1$  and  $S_2$  defined as  $D=T_{\text{ON}}/T_S$ , where  $T_{\text{ON}}$  is on time of the switches and  $T_S$  is the switching period, as indicated in Fig. 4. According to Eq. (10), duty cycle  $D$  of the proposed converter is limited to the maximum of  $D=0.5$ .

The relationship between output voltage  $V_O$  and  $V_B$  can be found by recognizing that load current  $I_O$  is equal to the average of rectified secondary current  $\langle i_{\text{SEC}} \rangle$ , *i.e.*,

$$V_O = R_L I_O = R_L \langle i_{\text{SEC}} \rangle, \quad (11)$$

where  $R_L$  is the load resistance.

Neglecting magnetizing current  $i_M$  by assuming that magnetizing inductance  $L_M$  is very (infinitely) large and by assuming that the time interval  $[T_2 - T_4]$  is much shorter than on time  $T_{\text{ON}}$  of switches  $S_1$  and  $S_2$ , the average secondary current is given by

$$I_O = \langle i_{\text{SEC}} \rangle = \frac{n^2 D^2}{2L_{\text{LK}} f_S} \left[ \frac{V_B}{n} - V_O \right], \quad (12)$$

where  $f_S=1/T_S$  is the switching frequency.

From Eqs. (10)-(12), the approximate voltage conversion ratio of the circuit in Fig. 1 can be calculated as

$$\frac{nV_O}{V_{\text{IN}}} \approx \frac{1}{1-2D} - \frac{2}{nD^2} \cdot \frac{I_O L_{\text{LK}} f_S}{nV_{\text{IN}}} = \frac{1}{1-2D} - \frac{2}{nD^2} I_{\text{ON}}, \quad (13)$$

where

$$I_{\text{ON}} = \frac{I_O L_{\text{LK}} f_S}{nV_{\text{IN}}} \quad (14)$$

is the normalized output current. The expression for the voltage conversion ratio in Eq. (13) is valid only for

$$0 < D < 0.5 \quad (15)$$

and

$$I_{\text{ON}} \leq \frac{nD^3}{1-2D}. \quad (16)$$

since  $nV_O/V_{\text{IN}} \leq 1$ .

As can be seen from Eq. (13), the voltage conversion ratio not only depends on duty cycle  $D$  and turns ratio  $n$  of the transformer, but it also depends on load current  $I_O$  as well as

switching frequency  $f_S$  and leakage inductance  $L_{\text{LK}}$ .

The proposed circuit can also be implemented so that input current  $i_{\text{IN}}$  flowing through boost inductor  $L_B$  is decreased all the way to zero during the off-time of switches  $S_1$  and  $S_2$ , as illustrated in Fig. 5. The operation of the circuit with discontinuous boost inductor current is the same as that of the circuit with continuous inductor current whose waveforms are shown in Fig. 4. The only difference is that after input current  $i_{\text{IN}}$  becomes zero at  $t=T_9$ , rectifiers  $D_1$  and  $D_2$  cease conducting and their reverse voltages for the remainder of the switching period are  $V_{D1}=V_{D2}=0.5(V_B-V_{\text{IN}})$ , as illustrated in Fig. 5. In addition, during the  $[T_9 - T_{10}]$  interval, the voltages across switches  $S_1$  and  $S_2$  and rectifier  $D_3$  are  $V_{S1}=V_{S2}=0.5(V_B+V_{\text{IN}})$  and  $V_{D3}=V_{\text{IN}}$ , respectively.

It should be noted that in the circuit in Fig. 1, substantial secondary current  $i_{\text{SEC}}$  flows only during the on-time of switches  $S_1$  and  $S_2$ . During the time the switches are off only a part of the relatively small magnetizing current flows through the secondary until the magnetizing inductance is reset. Due to the short duration (that is limited to less than  $T_S/2$ ) of the secondary current flow, as well as the triangular secondary current waveform, the peak current stress on the secondary side is relatively large.

The secondary-side current stress of the circuit in Fig. 1 can be significantly reduced by replacing rectifier  $D_3$  in Fig. 1 with switch  $S_3$ , as shown in Fig. 6. It should be noted that the body diode of switch  $S_3$  is labeled as  $D_3$  in Fig. 6. Switch  $S_3$  makes it possible for secondary current  $i_{\text{SEC}}$  to flow in both directions and to decrease the peak current through the secondary.

To facilitate the explanation of the circuit operation in Fig. 6, Fig. 7 shows the simplified circuit diagram, whereas Figs. 8 and 9 show its topological stages and key waveforms during a switching cycle, respectively. The reference

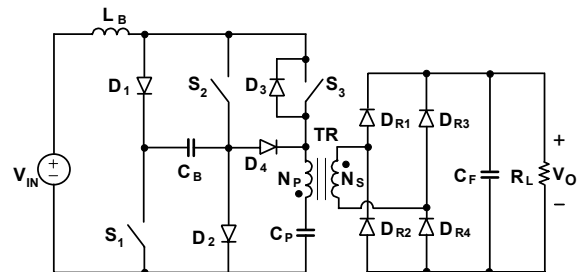


Fig. 6. Implementation of isolated boost converter with three switches.

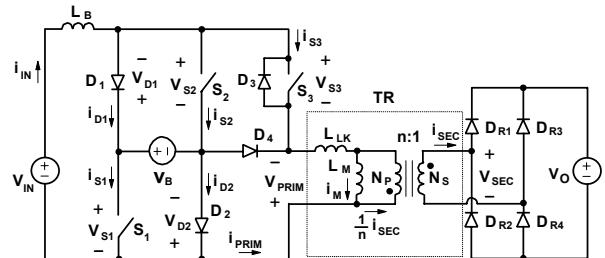


Fig. 7. Simplified circuit diagram of proposed isolated boost converter with three switches.

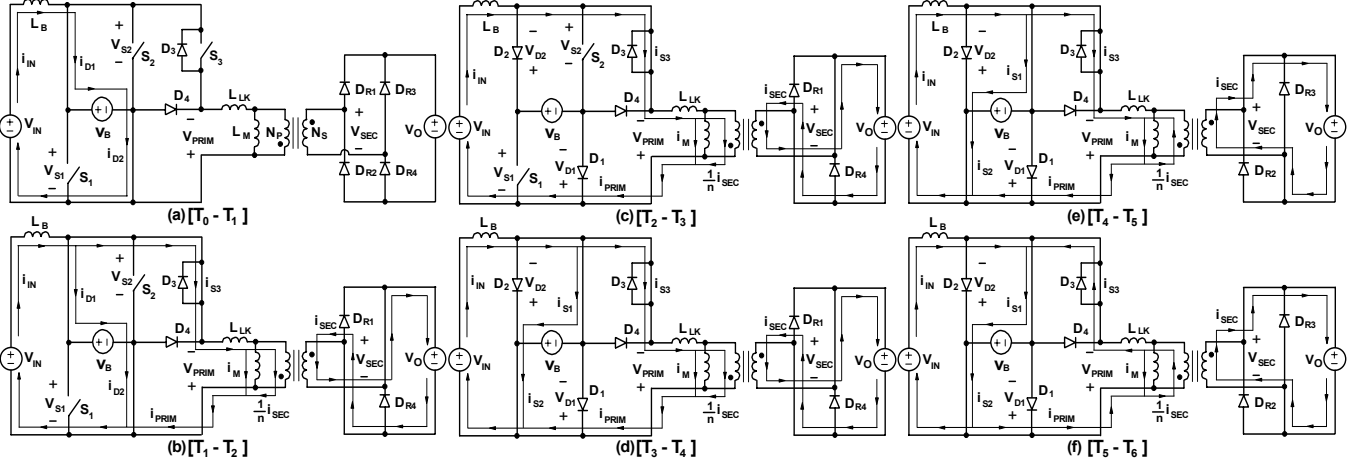


Fig. 8. Topological stages of isolated boost converter with three switches during time interval  $[T_0-T_6]$ . After switch  $S_3$  is turned off at  $t=T_6$ , topological stages of the circuit during remainder of switching period, *i.e.*, during time interval  $[T_6-T_{12}]$ , are identical to those of two-switch implementation in Fig. 1 during time interval  $[T_2-T_3]$ , shown in Fig. 3.

directions of currents and voltages plotted in Fig. 9 are shown in Fig. 7.

As can be seen from the timing diagrams of the drive signals for the switches, shown in Fig. 9, switch  $S_3$  is turned on substantially before switches  $S_1$  and  $S_2$  are simultaneously turned on and is turned off before switches  $S_1$  and  $S_2$  are turned off. For proper operation, *i.e.*, to avoid saturation of transformer TR, the duration of the time interval between the moment when switch  $S_3$  is closed and the moment when switches  $S_1$  and  $S_2$  are closed should be exactly equal to the on time of switches  $S_1$  and  $S_2$ . To prevent transformer saturation in the case of a drive-signal timing mismatch, blocking capacitor  $C_p$  is added in series with the primary winding of transformer TR, as shown in Fig. 6. Since the dc voltage across blocking capacitor  $C_p$  is zero for ideally matched drive signals, or very small for slightly mismatched drive signals, the voltage across  $C_p$  is neglected, *i.e.*, it is assumed to be zero in the following analysis.

As can be seen from Fig. 9, at  $t=T_0$  all three switches are off so input current  $i_{IN}$  flows through diodes  $D_1$  and  $D_2$ , as shown in Fig. 8(a). Assuming that at  $t=T_0$ , transformer TR is completely reset, *i.e.* magnetizing current  $i_M(t=T_0)=0$ , no other current flows in the circuit during the time interval from  $t=T_0$  until switch  $S_3$  is turned on at  $t=T_1$ . Since voltage  $V_B$  is greater than  $V_{IN}$ , during the  $[T_0 - T_1]$  interval input current  $i_{IN}$  is decreasing with a constant slope, as shown in Fig. 9. As a result, diode currents  $i_{D1}$  and  $i_{D2}$  are also decreasing with a slope given in Eq. (1).

After switch  $S_3$  is closed at  $t=T_1$ , primary current  $i_{PRIM}$  and secondary current  $i_{SEC}$  start to flow because voltage source  $V_B$  appears in parallel with the primary of the transformer, *i.e.*,  $V_{PRIM}=-V_B$ . Since during the  $[T_1 - T_2]$  interval secondary voltage  $V_{SEC}$  is negative, secondary current  $i_{SEC}$  is carried by rectifiers  $D_{R2}$  and  $D_{R3}$ . From Fig. 8(b), secondary current  $i_{SEC}$  during the  $[T_1 - T_2]$  interval can be calculated as

$$i_{SEC} = n \cdot [i_{PRIM} + i_M], \quad (17)$$

where primary current  $i_{PRIM}$  and magnetizing current  $i_M$  are

$$i_{PRIM} = -\frac{V_B - nV_O}{L_{LK}} \cdot t, \quad (18)$$

$$i_M = \frac{nV_O}{L_M} \cdot t, \quad (19)$$

$$i.e., \quad i_{SEC} = n \cdot \left[ -\frac{V_B - nV_O}{L_{LK}} + \frac{nV_O}{L_M} \right] \cdot t. \quad (20)$$

From Eqs. (18) and (20), it can be seen that during the  $[T_1 - T_2]$  interval, primary current  $i_{PRIM}$  and secondary current  $i_{SEC}$  increase linearly in the negative direction starting from zero at  $t=T_1$ , as illustrated in Fig. 9. Also, during this time interval, input current  $i_{IN}$  and diode currents  $i_{D1}$  and  $i_{D2}$  continuously decrease. The negative slope of  $i_{IN}$  is given in Eq. (1), whereas the negative slope of  $i_{D1}$  and  $i_{D2}$  is

$$\frac{di_{D1}}{dt} = \frac{di_{D2}}{dt} = \frac{V_{IN} - V_B}{L_B} - \frac{V_B - nV_O}{L_{LK}}. \quad (21)$$

When  $i_{D1}$  and  $i_{D2}$  become zero at  $t=T_2$ , the circuit enters the topological stage shown in Fig. 8(c). Since during this stage input current  $i_{IN}$  and primary current  $i_{PRIM}$  are equal, both currents continue to decrease with the same rate, which is given by Eq. (1), until switches  $S_1$  and  $S_2$  are simultaneously closed at  $t=T_3$ . From Fig. 8(c), it can be calculated that during the  $[T_2 - T_3]$  interval, the voltage across diodes  $D_1$  and  $D_2$  is

$$V_{D1} = V_{D2} = \frac{1}{2} \left( nV_O - V_B + L_{LK} \frac{di_{PRIM}}{dt} \right). \quad (22)$$

When switches  $S_1$  and  $S_2$  are turned on at  $t=T_3$ , primary voltage  $V_{PRIM}$  changes polarity, *i.e.*,  $V_{PRIM}=V_B$ . Consequently, primary current  $i_{PRIM}$  starts to increase, causing a corresponding increase in switch currents  $i_{S1}$  and  $i_{S2}$ , as well as in secondary current  $i_{SEC}$ , as illustrated in Fig. 9. The positive slope of the primary current is given by

$$\frac{di_{PRIM}}{dt} = \frac{V_B + nV_O}{L_{LK}}. \quad (23)$$

This stage, shown in Fig. 8(d), ends at  $t=T_4$  when secondary current  $i_{SEC}$  becomes zero. At that moment, rectifiers  $D_{R2}$  and  $D_{R3}$  stop conducting and secondary current  $i_{SEC}$  starts flowing through rectifiers  $D_{R1}$  and  $D_{R4}$ , as shown in

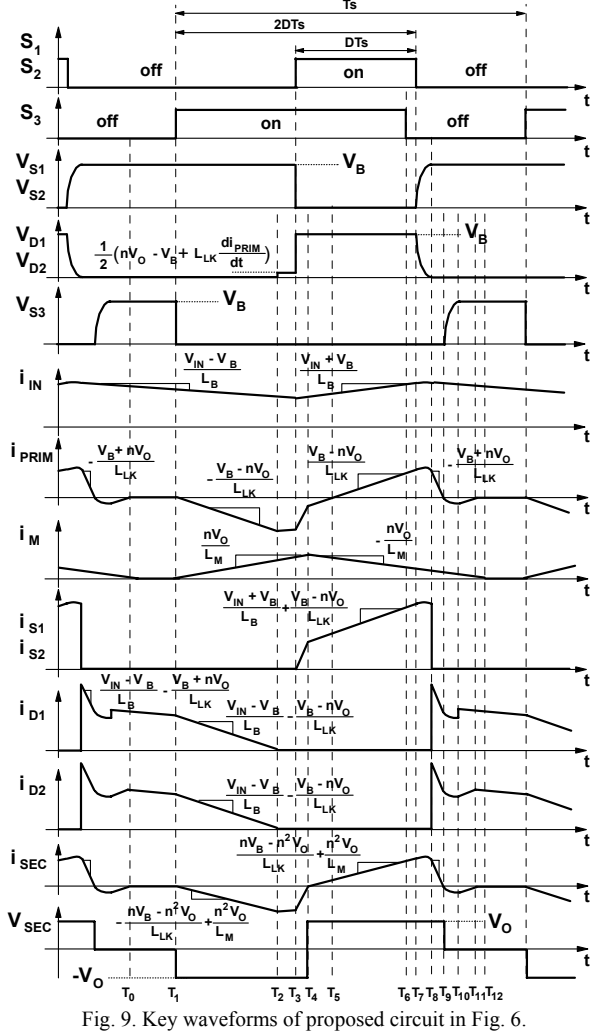


Fig. 9. Key waveforms of proposed circuit in Fig. 6.

Fig. 8(e). Because at  $t=T_4$  the secondary voltage changes polarity, as illustrated in Fig. 9, the positive slope of primary current  $i_{PRIM}$  changes to

$$\frac{di_{PRIM}}{dt} = \frac{V_B - nV_O}{L_{LK}} \quad (24)$$

Moreover, it causes corresponding changes in the positive slope of currents  $i_{S1}$ ,  $i_{S2}$ , and  $i_{SEC}$ , as shown in Fig. 9.

After primary current  $i_{PRIM}$  changes polarity at  $t=T_5$ , switch  $S_3$  can be turned off under ZVS condition. In Fig. 9,  $S_3$  is turned off at  $t=T_6$ , just before the turn off instance of switches  $S_1$  and  $S_2$ , to minimize the conduction time of the body diode of each switch. Once switch  $S_3$  is turned off and primary current  $i_{PRIM}$  is diverted to the body diode of switch  $S_3$ , the operation of the circuit for the rest of the switching cycle is identical to that of the circuit with two switches shown in Fig. 1. Specifically, the operation of the circuit in Fig. 6 from  $t=T_6$  through  $t=T_{12}$  is identical to the operation of the circuit in Fig. 1 from  $t=T_2$  through  $t=T_8$ .

Comparing the waveforms of secondary current  $i_{SEC}$  shown in Fig. 4 and Fig. 9, it can be seen that for the same output

current, which is the average of rectified secondary current  $i_{SEC}$ , the peak of secondary current  $i_{SEC}$  in the proposed circuit in Fig. 6 is approximately one-half of that in Fig. 1. In addition, the voltage conversion ratio of the proposed circuit in Fig. 6 is given by

$$\frac{nV_O}{V_{IN}} \approx \frac{1}{1-2D} - \frac{1}{nD^2} I_{ON}, \quad (25)$$

where  $I_{ON}$  is defined in Eq.(14) and the range of duty cycle  $D$  is  $0 < D < 0.5$ .

### III. EXPERIMENTAL RESULTS

The performance of the proposed isolated boost-converter topology was verified on a dual ac-input 900-W experimental prototype operating at 100-kHz switching frequency and providing 385-V dc output voltage. The dual ac-input prototype was built with two two-switch isolated boost rectifiers. Each rectifier employs an independent average-current PFC controller. Each isolated PFC boost rectifier was designed to deliver full maximum output power to meet the ac-line redundancy requirement. In addition, to provide input power sharing between the two ac-line inputs, an active output-current sharing circuit was employed.

Figure 10 shows the measured gate-to-source voltage, drain-to-source voltage, and drain current of switch  $S_1$ . The waveforms in Figs. 10(a) and 10(b) were measured when the boost rectifier operates in CCM and DCM, respectively. The switch voltage is well clamped to bulk voltage  $V_B$ . It should be noted that the voltage ringing in Fig. 10(b) occurs after the inductor current becomes zero in DCM operation. During that period, the output capacitance of each boost switch and boost inductor  $L_B$  oscillate. However, this voltage can never exceed voltage  $V_B$  since the switch is clamped by diodes  $D_1$  and  $D_2$ .

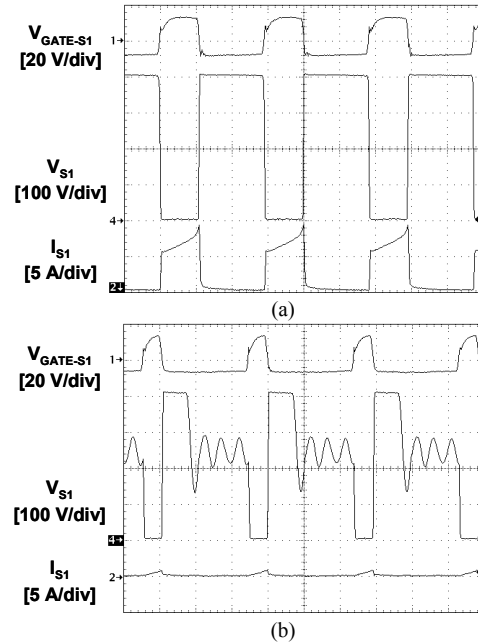


Fig. 10. Measured switch voltage and current waveforms of experimental isolated boost converter at  $V_{IN}=90$  V<sub>AC</sub>,  $V_O=385$  V<sub>DC</sub> at (a) CCM and (b) DCM operation. Time base: 5  $\mu$ s/div.

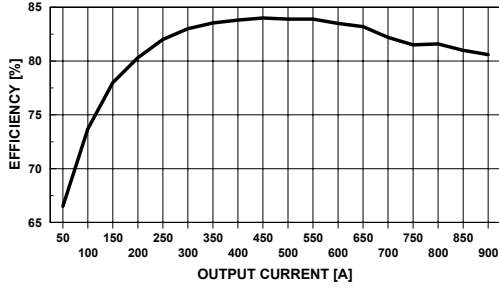


Fig. 11. Measured efficiency of experimental converter at  $V_{IN}=90$  V<sub>AC</sub> and  $V_{OUT}=385$  V<sub>DC</sub>.

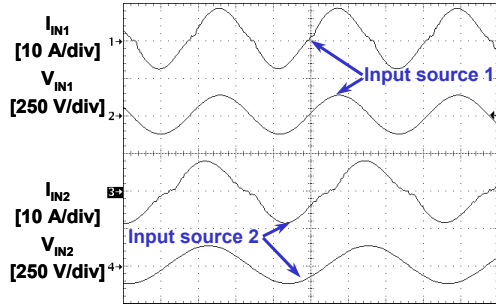


Fig. 12. Measured input voltage and current waveforms of experimental dual ac-input prototype connected to source 1 ( $V_{IN1}=90$  V<sub>AC</sub>,  $f_{L1}=63$  Hz,  $P_{IN1}=503$  W) and source 2 ( $V_{IN2}=90$  V<sub>AC</sub>,  $f_{L2}=47$  Hz,  $P_{IN2}=492$  W). Time base: 5 ms/div.

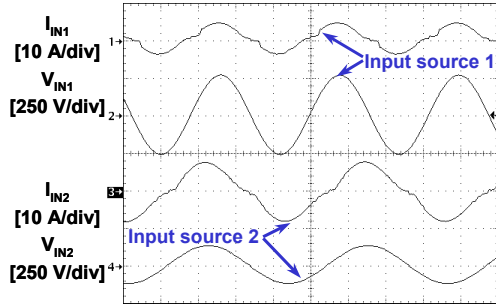


Fig. 13. Measured input voltage and current waveforms of experimental dual ac-input prototype connected to source 1 ( $V_{IN1}=90$  V<sub>AC</sub>,  $f_{L1}=63$  Hz,  $P_{IN1}=506$  W) and source 2 ( $V_{IN2}=185$  V<sub>AC</sub>,  $f_{L2}=47$  Hz,  $P_{IN2}=469$  W). Time base: 5 ms/div.

Figure 11 shows the measured efficiency of a single two-switch isolated-boost PFC converter as a function of output power at minimum line voltage of 90 V. As can be seen from Fig. 11, the full-load, minimum-line efficiency is approximately 81%.

Finally, Figs. 12 and 13 show the measured line voltage and current waveforms of the experimental prototype connected to two independent ac sources and delivering full output power. The waveforms in Fig. 12 were measured with one isolated PFC rectifier connected to a source with voltage  $V_{IN1}=90$  V and line frequency  $f_{L1}=63$  Hz and the other isolated PFC rectifier connected to another source with voltage  $V_{IN2}=90$  V and line frequency  $f_{L2}=47$  Hz. In this operating condition, the measured input power from the two ac sources were  $P_{IN1}=503$  W and  $P_{IN2}=492$  W, *i.e.*, an

excellent input-power sharing with a difference of less than 3% was achieved.

The waveforms in Fig. 13 were measured with one isolated PFC rectifier connected to a source with voltage  $V_{IN1}=90$  V and line frequency  $f_{L1}=63$  Hz and the other isolated PFC rectifier connected to another source with voltage  $V_{IN2}=185$  V and line frequency  $f_{L2}=47$  Hz. The measured input power of the individual ac sources for the operating condition in Fig. 13 were  $P_{IN1}=506$  W and  $P_{IN2}=469$  W, which still translates to an input-power sharing accuracy better than 10%.

#### IV. SUMMARY

A two-switch implementation and a three-switch implementation of the isolated boost converter that exhibit ringing-free voltage waveforms across all semiconductor devices on the primary and secondary sides of the transformer are introduced. In both implementations, ringing-free operation is achieved by clamping the voltages of the primary switches and rectifiers to the voltage of the primary-side energy-storage capacitor and clamping the voltage across the secondary-side rectifiers to the output filter capacitor. The three-switch implementation exhibits lower peak currents in the secondary-side components compared to those in the two-switch implementation.

The performance of the proposed isolated boost converter topology was verified on a dual ac-input 900-W experimental prototype. The prototype was built with two, two-switch isolated PFC boost rectifiers operating with an active output-current sharing circuit. The measured full-load, low-line efficiency and THD of the individual converters were approximately 81% and 7.5%, respectively.

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