# A New PWM ZVS Full-Bridge Converter

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***Abstract* — A soft-switched full-bridge (FB) converter that features zero-voltage-switching (ZVS) of the bridge switches over a wide range of input voltage and output load is introduced. The proposed converter achieves ZVS with substantially reduced duty-cycle loss and circulating current. The control of the proposed converter can be implemented either with the phase-shift (PS) or pulse-width-modulated (PWM) technique. The performance of the proposed topology was verified on a 2-kW (48-V/40-A) experimental PWM FB converter prototype operating at 120 kHz from a 380-V dc input.**

## I. Introduction

The full-bridge (FB) zero-voltage-switched (ZVS) converter shown in Fig. 1 is the most widely used soft-switched circuit in high-power applications, [1]-[3]. This constant-frequency converter employs phase-shift control and features ZVS of the primary switches with relatively small circulating energy. However, full ZVS operation can only be achieved with a limited load and input-voltage range, unless a relatively large inductance is provided in series with the primary winding of the transformer either by an increased leakage inductance of the transformer and/or by an additional external inductor. This increased inductance has a detrimental effect on the performance of the converter since it causes an increased loss of the duty cycle on the secondary side, as well as severe voltage ringing across the secondary-side output rectifiers due to the resonance between the inductance and the junction capacitance of the rectifier. The secondary-side ringing can be suppressed by either a passive RCD snubber, shown in Fig. 1, or an active snubber described in [1]. For implementations with an external primary inductor, the ringing can also be effectively controlled by employing primary-side clamp diodes $D_1$ and $D_2$ shown in Fig. 1, as proposed in [2]. While the snubber approaches in [1] and [2] offer practical and efficient solutions to the secondary-side ringing problem, they do not offer any improvement of the secondary-side duty-cycle loss.

Several techniques have been proposed to extend the ZVS range of FB ZVS converters without the loss of duty cycle and secondary-side ringing [4]-[7]. Generally, these circuits achieve ZVS for all primary switches in an extended load and input-voltage range by utilizing energy stored in the inductive components of an auxiliary circuit. Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load because the full-load current stores enough energy in the converter's inductive components to achieve complete ZVS for all switches. As the load current decreases, the energy provided by the auxiliary circuit must increase to maintain ZVS, with the maximum energy required at no load. In the approaches described and analyzed in [4] and [5], the energy stored for ZVS is independent of load, therefore these FB ZVS converters cannot optimally resolve the trade-off between power-loss savings brought about by a full-load-range ZVS and power losses of the auxiliary circuit. A number of FB ZVS converters that feature ZVS over the entire load range with adaptive energy storage in the auxiliary circuit have been introduced in [6] and [7]. However, a major deficiency of these converters is a relatively high circulating energy that is needed to achieve no-load ZVS and that is due to a relatively large inductor employed to assist ZVS.

In this paper, a FB ZVS converter with adaptive energy storage that offers ZVS of the primary switches over a wide input voltage and load ranges with greatly reduced no-load circulating energy and with significantly reduced secondary-side duty cycle loss is introduced. The proposed converter can be controlled by either constant-frequency phase-shift control or conventional PWM control.

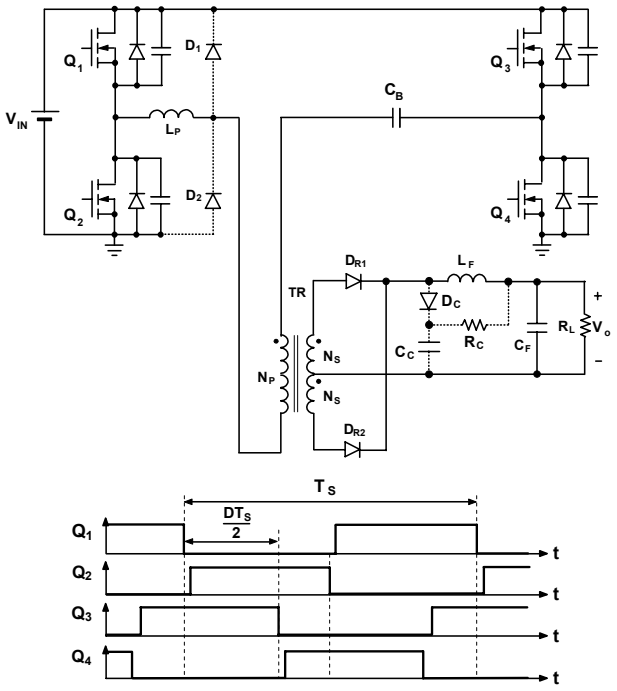


Fig. 1. Conventional phase-shifted full-bridge ZVS converter and its switch timing waveforms.

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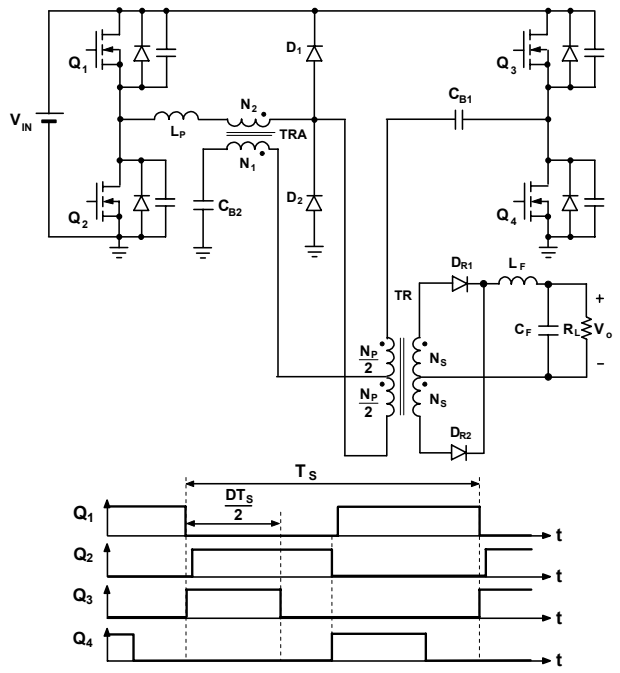


Fig. 2. Proposed full-bridge ZVS converter: (a) circuit diagram; (b) timing diagram for variable duty-cycle PWM control.

## II. PWM ZVS FULL-BRIDGE CONVERTER

Figure 2 shows the proposed FB ZVS converter that provides ZVS for the bridge switches over a wide range of input voltage and load current. As shown in Fig. 2, the proposed converter employs low-power auxiliary transformer TRA to extend the ZVS range. The primary of auxiliary transformer TRA is connected to the center tap of power transformer TR and the ground through blocking capacitor $C_{B2}$, whereas its secondary is connected in series with the primary winding of power transformer TR and inductor $L_P$. Auxiliary transformer TRA is only used to adaptively store a relatively small amount of energy into primary inductor $L_P$ that is required for ZVS. Finally, two diodes are connected from the node connecting the primary of the power transformer and the secondary of the auxiliary transformer to the positive and negative (ground) rails of the bridge to provide a path for the current through primary inductor $L_P$, which is used to store ZVS energy.

When the load voltage is regulated, as the load current and/or input voltage decreases, the duty cycle of each PWM switch, *i.e.*, switches $Q_3$ and $Q_4$, decreases so that the volt-second product on the windings of power transformer TR also decreases. At the same time, the volt-second product on the windings of auxiliary transformer TRA increases, which proportionally increases the energy stored in the primary inductor. Due to the adaptive nature of the energy available for ZVS stored in the primary inductor, which increases as the load current and/or input voltage decreases, the proposed circuit can achieve ZVS in a very wide range of input voltage and load current, including no load, with minimal circulating energy.

In the proposed circuit, since the ZVS energy stored in the primary inductor is dependent on its inductance value and the volt-second product of the secondary of auxiliary transformer TRA, the size of the primary inductor can be minimized by properly selecting the turns ratio of auxiliary transformer TRA. As a result, the size of the primary inductor is very much reduced compared to that of the conventional phase-shift FB converter shown in Fig. 1. In addition, since the auxiliary transformer does not need to store energy, its size can be small. Finally, because the energy used to create the ZVS condition at light loads is not stored in the leakage inductances of transformer TR, the transformer's leakage inductances can also be minimized. As a result of the reduced total primary inductance, *i.e.*, the inductance of the primary inductor used for ZVS energy storage and the leakage inductance of the power transformer, the proposed converter exhibits a relatively small duty-cycle loss, which minimizes both the conduction loss of the primary switches and the voltage stress on the components on the secondary side of the transformer, which improves the conversion efficiency. Moreover, because of the reduced total primary inductance, the secondary-side parasitic ringing is also reduced and is effectively controlled by primary side diodes $D_1$ and $D_2$.

As shown in the timing diagram in Fig. 2, for constant-frequency, variable duty cycle control of the proposed converter, switches $Q_1$ and $Q_2$ always operate with approximately 50% duty cycle, whereas switches $Q_3$ and $Q_4$ have a duty cycle in the range from 0% to 50%.

### A. Operation

To facilitate the explanation of the operation of the circuit in Fig. 2, Fig. 3 shows a simplified circuit diagram. In the simplified circuit it is assumed that the inductance of output filter $L_F$ is large enough so that during a switching cycle the output filter can be modeled as a constant current source with a magnitude equal to output current $I_O$. Also, it is assumed that the capacitance of capacitor $C_{B2}$ is large enough so that

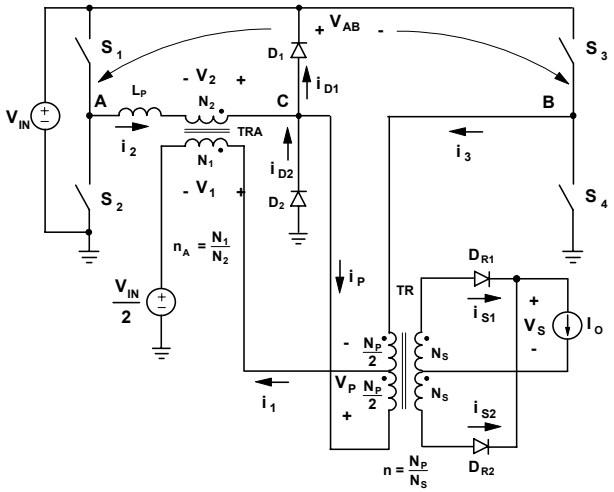


Fig. 3. Simplified circuit diagram of proposed converter showing reference directions of currents and voltages.

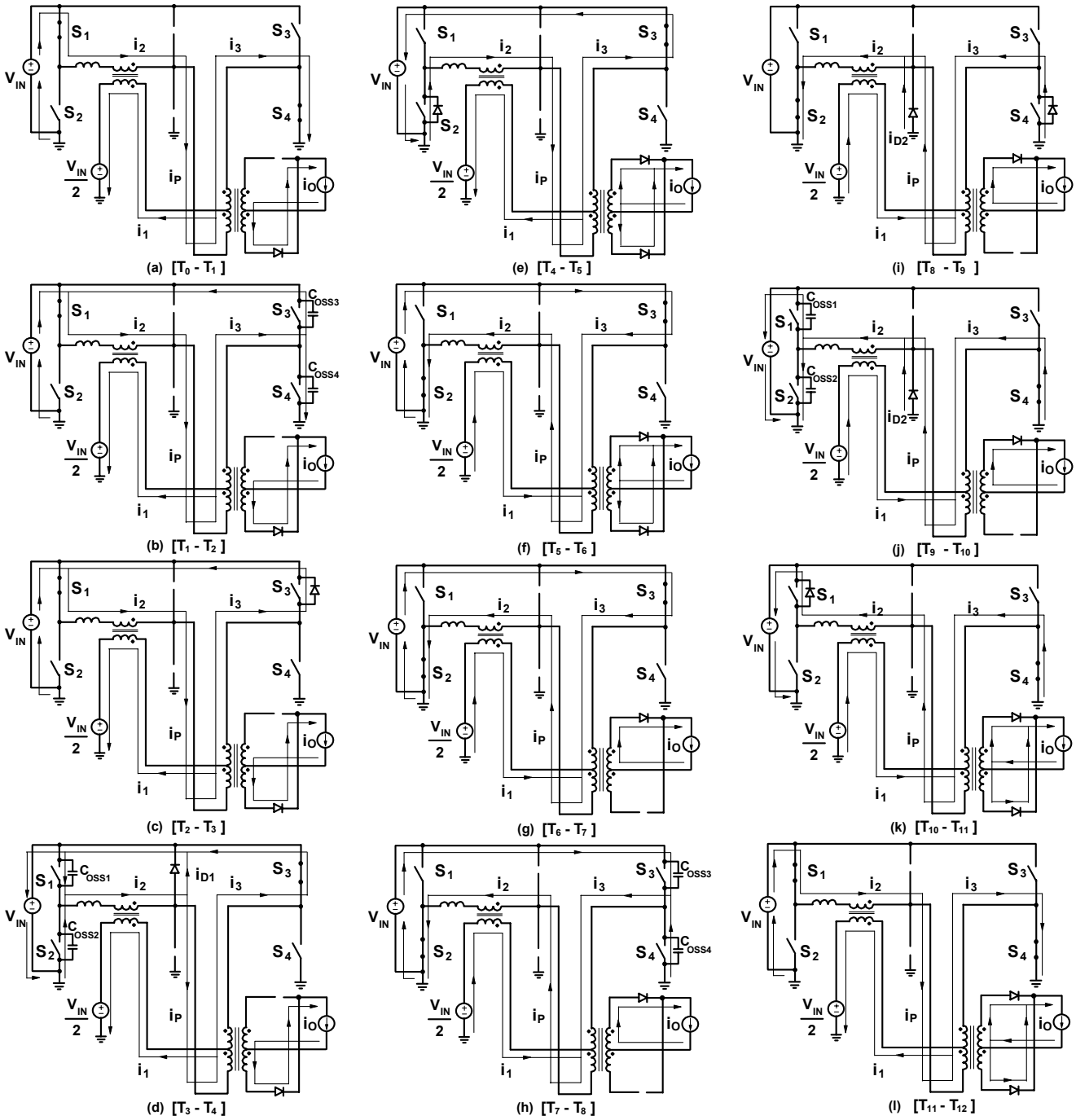


Fig. 4. Topological stages of proposed converter power stage.

the capacitor can be modeled as a constant voltage source. Because the average voltages of the windings of both transformers are zero and because switches $Q_1$ and $Q_2$ operate with approximately 50% duty cycle, the magnitude of the voltage source that models $C_{B2}$ is approximately $V_{IN}/2$. Blocking capacitor $C_{B1}$, which is used to prevent transformer core saturation due to various bridge component mismatching, can be neglected since it has no significant effect on the operation of the circuit.

To further simplify the analysis, it is assumed that the resistance of each conducting semiconductor switch is zero, whereas the resistance of each non-conducting switch is infinite. In addition, the leakage inductance of auxiliary transformer TRA and the magnetizing inductances of both transformers are neglected since their effect on the operation of the circuit is not significant. However, the output capacitance of each primary switch is not neglected in this analysis since it is important for understanding the operation

of the proposed circuit. Finally, since turns ratio $n_A$ of auxiliary transformer TRA, which equals $N_1/N_2$, is much greater than unity, current $i_1$ through winding $N_1$ of TRA is very small compared to primary current $i_P$ and is neglected, *i.e.*, in the following analysis it is assumed that $i_1=0$.

Figure 4 shows topological stages of the proposed converter during a switching period, whereas Fig. 5 shows its key waveforms. As shown in Fig. 4(a), when diagonal switches $S_1$ and $S_4$ are conducting, primary voltage $V_P$ is positive so that load current $I_O$ flows through rectifier $D_{R2}$ and the lower secondary of power transformer TR. Since during this topological stage diodes $D_1$ and $D_2$ are reverse biased, the reflected primary current $i_P=I_O/n$, where $n=N_P/N_S$, is flowing through closed switch $S_1$, primary inductor $L_P$, winding $N_2$ of auxiliary transformer TRA, primary winding $N_P$ of transformer TR, and closed switch $S_4$. During this topological stage, almost all the input voltage is induced across primary winding $N_P$ of transformer TR because the impedances of primary inductor $L_P$ and winding $N_2$ of auxiliary transformer TRA are very small compared to the reflected output impedance across primary winding $N_P$ of transformer TR. As a result, the potential of the center tap of primary winding $N_P$ is $V_P/2\cong V_{IN}/2$, and hence, the voltage across each winding of auxiliary transformer TRA is near zero, *i.e.*, $V_1=V_2\cong 0$, as shown in Fig. 5.

After switch $S_4$ is turned off at $t=T_1$, primary current $i_P=I_O/n$ starts charging output capacitance $C_{OSS4}$ of switch $S_4$ and discharges output capacitance $C_{OSS3}$ of switch $S_3$, as shown in Fig. 4(b). As a result, voltage $V_{S4}$ across switch $S_4$ starts increasing toward $V_{IN}$, whereas voltage $V_{S3}$ across switch $S_3$ starts decreasing toward zero. At the same time, auxiliary transformer winding voltages $V_1$ and $V_2$ start increasing from zero to $V_{IN}/2$ and $V_{IN}/(2n_A)$, respectively. Because of the increasing voltage $V_2$, diode $D_1$ becomes forward biased and clamps the potential of node C to $V_{IN}$.

Since the energy for charging $C_{OSS4}$ and discharging $C_{OSS3}$ is supplied from filter inductor $L_F$, which generally has a large inductance, this energy is large enough to completely discharge $C_{OSS3}$ even at low currents, as illustrated in Fig. 5. After $C_{OSS3}$ is completely discharged, *i.e.*, after the voltage across switch $S_3$ reaches zero at $t=T_2$, primary current $i_P$ continues to flow through the antiparallel diode of switch $S_3$.

When the voltage across switch $S_3$ becomes zero, voltage across the power transformer also becomes zero since the primary of the transformer is shorted by the simultaneous conduction of the body diode of $S_3$ and diode $D_1$. As a result, the secondary windings are also shorted so that rectifiers $D_{R1}$ and $D_{R2}$ can conduct the load current simultaneously. However, because of the leakage inductance of transformer TR, load current $I_O$ is still carried by the lower secondary through rectifier $D_{R2}$ since no voltage is available to commutate the current from the lower secondary and $D_{R2}$ to the upper secondary and $D_{R1}$ if ideal components are assumed. With real components this commutation voltage exists, but is too small to commutate a significant amount of current from the lower to the upper secondary so that even

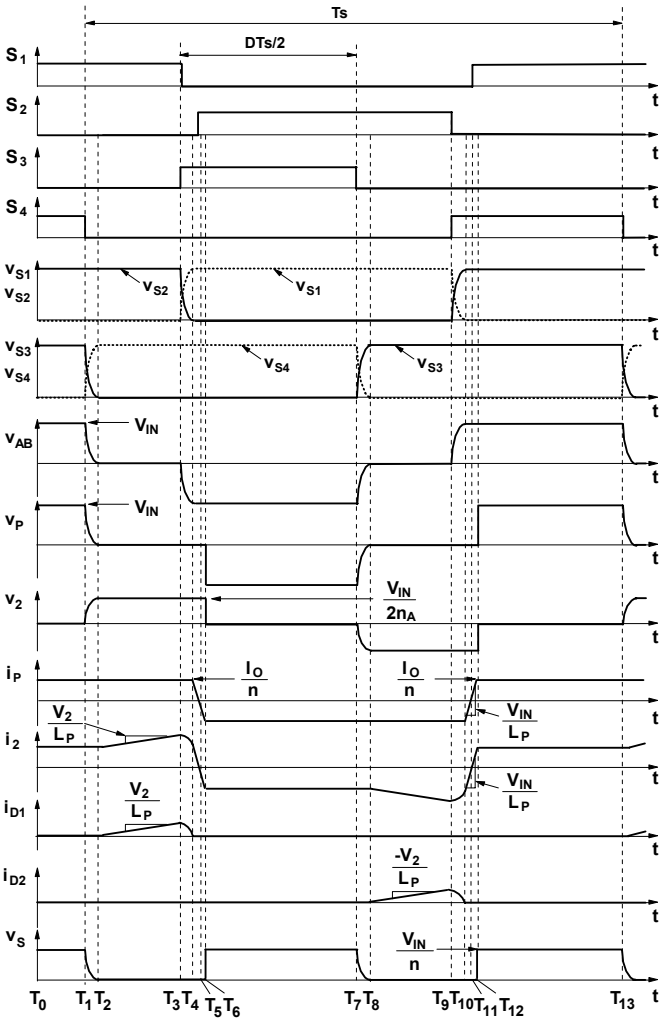


Fig. 5. Key waveforms of proposed converter power stage for variable duty cycle PWM control.

with real components the majority of the current is still found in the lower secondary and its corresponding rectifier $D_{R2}$. As a result, during the topological stage when switches $S_1$ and $S_3$ are conducting, shown in Fig. 4(c), primary current $i_P$ stays virtually unchanged, *i.e.*, $i_P=I_O/n$.

Since during the topological stage in Fig. 4(c) diode $D_1$ is conducting, voltage $V_2=V_{IN}/(2n_A)$ is applied directly across primary inductor $L_P$, which linearly increases current $i_2$ until switch $S_1$ is turned off at $t=T_3$, as illustrated in Fig. 5. During time interval $T_2$-$T_3$, the linearly increasing current through diode $D_1$, $i_{D1}$, is given by

$$i_{D1}(t)=\frac{V_2}{L_P}(t-T_2)=\frac{V_{IN}}{2n_A L_P}(t-T_2),\quad T_2\le t\le T_3, \quad (1)$$

so that current $i_2$ is

$$i_2(t)=i_P+i_{D1}(t)=\frac{I_O}{n}+\frac{V_{IN}}{2n_A L_P}(t-T_2),\quad T_2\le t\le T_3. \quad (2)$$

During this interval, the voltage across switch $S_3$ is kept zero because diode $D_1$ clamps the potential of node C to $V_{IN}$. As a result, switch $S_3$ is turned on with ZVS at $t=T_3$. After switch $S_1$ is turned off at $t=T_3$, current $i_2$ begins charging output

capacitance $C_{OSS1}$ of switch $S_1$ and discharging capacitance $C_{OSS2}$ of switch $S_2$, as shown in Fig. 4(d). By properly selecting turns ratio $n_A$ of auxiliary transformer TRA and the inductance value of $L_P$, the energy stored in $L_P$ will be enough to charge capacitance $C_{OSS1}$ of switch $S_1$ and discharge capacitance $C_{OSS2}$ of switch $S_2$ even at no load. After capacitance $C_{OSS2}$ is discharged, primary current $i_P=i_2$ continues to flow through the antiparallel diode of switch $S_2$ so that switch $S_2$ can be turned on with ZVS after $t=T_4$, as shown in Fig. 5.

Because in this topological stage voltage $V_{S1}$ across switch $S_1$ that is in opposition to voltage $V_2$ is increasing, current $i_{D1}$ starts decreasing. When current $i_{D1}$ becomes zero at $t=T_4$, diode $D_1$ stops conducting so that primary current $i_P=i_2$ starts decreasing because a negative voltage appears across primary inductor $L_P$ and leakage inductance $L_{LK}$ of transformer TR. At the same time, load current $I_O$ begins commutating from the lower secondary and rectifier $D_{R2}$ into the upper secondary and corresponding rectifier $D_{R1}$. The rate of change of the primary current is given by

$$\frac{di_P}{dt} = -\frac{V_{IN}}{L_P + L_{LK}} \approx -\frac{V_{IN}}{L_P}, \tag{3}$$

since $L_P >> L_{LK}$.

When the commutation of the load current from the lower to the upper secondary is completed at $t=T_6$, the primary current commutation from the positive to negative direction is also finished so that the primary current is $i_P=-I_O/n$. After the primary current is commutated in the negative direction, voltages $V_1$ and $V_2$ of the windings of auxiliary transformer TRA quickly collapse to zero, as illustrated in Fig. 5.

The circuit stays in the topological mode shown in Fig. 4(g) with diagonal switches $S_2$ and $S_3$ turned on until switch $S_3$ is turned off at $t=T_7$, which marks the end of the first half of the switching period and the beginning of the second half of the switching period. In the second half of the switching period, the operation of the circuit is exactly the same as the operation in the first half of the switching period as illustrated in Figs. 4(h)-4(l) and Fig. 5.

The operation of the circuit in Fig. 2 with phase-shift control is similar to that of the described variable duty cycle control.

*B. Design Considerations*

As already explained, in the proposed circuit shown in Fig. 2, lagging-leg switches $S_3$ and $S_4$ can achieve complete ZVS turn on even at very light loads because the ZVS conditions are maintained by voltage $V_2$ and diodes $D_1$ and $D_2$. However, to achieve ZVS of leading-leg switches $S_1$ and $S_2$ in a wide load range, it is necessary to store enough energy in primary inductor $L_P$ by properly selecting turns ratio $n_A$ of auxiliary transformer TRA and the inductance value of $L_P$. The total energy stored in inductor $L_P$ prior to the turn off of a leading-leg switch and subsequent turn on of the other leading-leg switch is given by

$$E_{LP} = \frac{1}{2} L_P i_2^2, \tag{4}$$

where $i_2$ is the current of inductor $L_P$ at the moment when a leading leg switch turns off, *i.e.*, at moments $t=T_3$ and $t=T_9$ in Fig. 5. Since

$$i_2(t=T_3) = \frac{I_O}{n} + i_{D1}(t=T_3) \tag{5}$$

and

$$i_2(t=T_9) = -\left(\frac{I_O}{n} + i_{D2}(t=T_9)\right), \tag{6}$$

substituting expression (1) for $i_{D1}$ and $i_{D2}$ into (4) and recognizing that $i_{D1}$ and $i_{D2}$ flow only during the off time $(1-D)T_S/2$, as shown in Fig. 5, the stored energy in $L_P$ available for ZVS of the leading-leg switches can be expressed as

$$E_{LP} = \frac{1}{2} L_P \left(\frac{I_O}{n} + \frac{V_{IN}(1-D)}{4n_A L_P f_S}\right)^2, \tag{7}$$

where $f_S=1/T_S$ is the switching frequency.

Neglecting the transformer winding capacitances and any other parasitic capacitance, to achieve ZVS of leading-leg switches, stored energy $E_{LP}$ must be at least equal to the energy required to charge output capacitance $C_{OSS}$ (of the leading-leg switch that is turning off) to $V_{IN}$ and discharge output capacitance $C_{OSS}$ (of the other leading-leg switch that is about to be turned on) to zero, *i.e.*,

$$E_{LP} \geq C_{OSS} V_{IN}^2. \tag{8}$$

From (7) and (8), it follows that the ZVS condition is

$$L_P \left(\frac{I_O}{n} + \frac{V_{IN}(1-D)}{4n_A L_P f_S}\right)^2 \geq 2C_{OSS} V_{IN}^2. \tag{9}$$

For a properly designed converter, duty cycle D is very close to 1 at full load. Therefore, the ZVS condition can be expressed as

$$L_P \left(\frac{I_{O(MAX)}}{n}\right)^2 \geq 2C_{OSS} V_{IN}^2 \tag{10}$$

at full load, where $I_{O(MAX)}$ is the full load current. As it can be seen from (10), almost all the energy stored in $L_P$ is from the output current reflected into the primary.

However, according to (9), at no load ($I_O=0$) or light loads all energy stored in $L_P$ is due to currents $i_{D1}$ or $i_{D2}$. Since at no load $D<<1$, the ZVS condition can be rewritten as

$$L_P \left(\frac{V_{IN}}{4n_A L_P f_S}\right)^2 \geq 2C_{OSS} V_{IN}^2. \tag{11}$$

Expressions (10) and (11) can be used to estimate the required value of primary inductance $L_P$ and turns ratio of auxiliary transformer $n_A$. From (10), $L_P$ can be calculated as

$$L_P \geq \frac{2C_{OSS} V_{IN(MAX)}^2}{\left(I_{O(MAX)}/n\right)^2}, \tag{12}$$

where $V_{IN(MAX)}$ is the high line input voltage since it represents the worst-case input voltage. To minimize full-load circulating energy and the size of inductor $L_P$, the smallest value of $L_P$ that satisfies (12) should be selected, *i.e.*,

$$L_P \approx \frac{2C_{OSS} V_{IN(MAX)}^2}{\left(I_{O(MAX)}/n\right)^2}. \tag{13}$$

Once $L_P$ is determined according to (13), desired range of $n_A$ can be calculated from (11) as

$$n_A \le \frac{1}{4f_S\sqrt{2C_{OSS}L_P}}. \quad (14)$$

To minimize no-load circulating energy and the size of the auxiliary transformer, the turns ratio of the auxiliary transformer should be maximized, *i.e.*, $n_A$ should be selected so that

$$n_A \approx \frac{1}{4f_S\sqrt{2C_{OSS}L_P}}. \quad (15)$$

With $L_P$ and $n_A$ selected according to (13) and (15), the proposed circuit achieves complete ZVS over the entire load range.

It should be noted that the value of $L_P$ in the proposed circuit is many times smaller than the value of primary inductance $L_P$ required to achieve ZVS for the primary switches in the conventional phase-shifted FB ZVS-PWM converter shown in Fig. 1. In fact, the value of $L_P$ in the conventional converter $L_{P(CONV)}$ is determined by the condition that $L_{P(CONV)}$ has enough energy to achieve ZVS at the minimum desirable current, *i.e.*,

$$L_{P(CONV)} \ge \frac{2C_{OSS}V_{IN(MAX)}^2}{\left(I_{O(MIN)}/n\right)^2}, \quad (16)$$

where $I_{O(MIN)}$ is the minimum current at which complete ZVS can be achieved.

From Eqs. (13) and (16), the ratio of the values of the primary inductor in the proposed circuit and that of the conventional circuit is

$$\frac{L_P}{L_{P(CONV)}} = \left(\frac{I_{O(MIN)}}{I_{O(MAX)}}\right)^2. \quad (17)$$

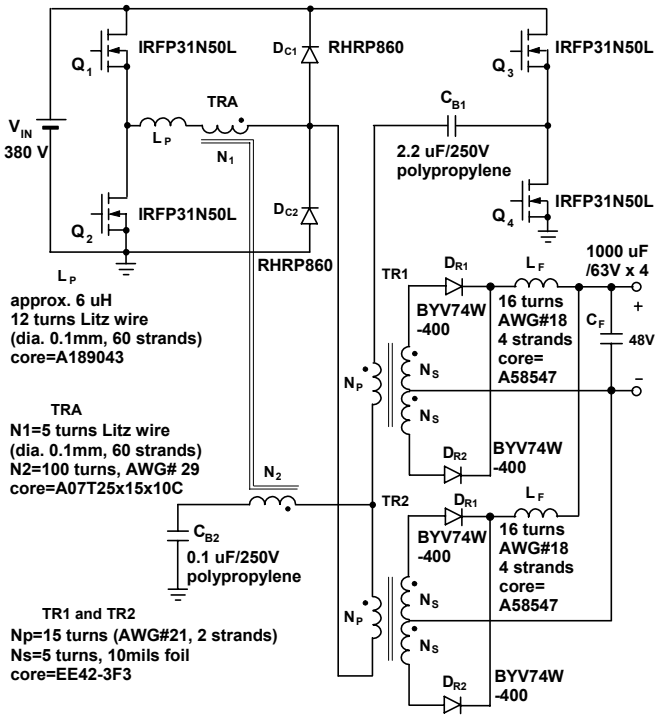


Fig. 6. Experimental 2-kW FB ZVS converter power-stage components.

Therefore, to achieve ZVS in the conventional circuit from full load $I_{O(MAX)}$ to only 50% of full load, $L_{P(CONV)}$ must be four times larger than $L_P$ in the proposed circuit. To extend the ZVS range to 25% of full load, $L_{P(CONV)}$ must be sixteen times larger than $L_P$. Because of a substantially reduced value of primary inductance $L_P$ compared to the required value of $L_{P(CONV)}$ in the conventional phase-shifted full-bridge ZVS converter, the secondary-side duty-cycle loss of the proposed circuit is also substantially reduced compared to that of the conventional phase-shifted full-bridge ZVS converter. At the same time, the reduced value of $L_P$ reduces the energy in the parasitic ringing on the secondary side. In fact, this parasitic ringing is very much suppressed in the circuit in Fig. 2 because diodes $D_1$ and $D_2$ clamp the primary voltage of the power transformer to the input voltage. Since the leakage inductance of the power transformer in the proposed circuit can be minimized because it is not used to store ZVS energy, the primary winding clamp also effectively clamps the secondary winding voltage. Any parasitic ringing due to the residual leakage inductance of the transformer can be controlled with a small (low-power) snubber circuit.

## III. Experimental Results

The performance of the proposed converter was verified on a 2-kW prototype circuit designed to operate from a 380 V-dc input voltage and provide 48-V dc output voltage. The component values of the experimental circuit are shown in Fig. 6. To distribute losses, the experimental circuit was designed with two transformers with their primary windings connected in series to ensure current sharing between their secondaries. The control circuit was implemented with a constant-frequency PWM FB controller ISL6753 from Intersil. For performance comparison purposes, an experimental prototype of the conventional FB ZVS converter was also built. The conventional FB ZVS converter was designed with an external inductance of 18 μH in series with the primary windings of the two transformers (13T:5T:5T) to achieve ZVS over the load range from 50% to 100%.

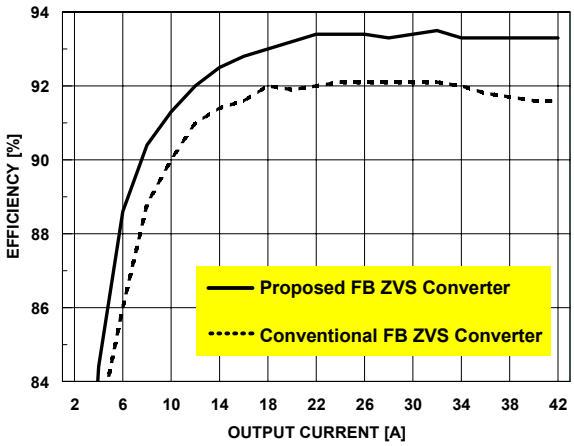


Fig. 7. Measured efficiencies of conventional phase-shifted FB ZVS converter (dashed line) and proposed converter (solid line) as functions of output current.

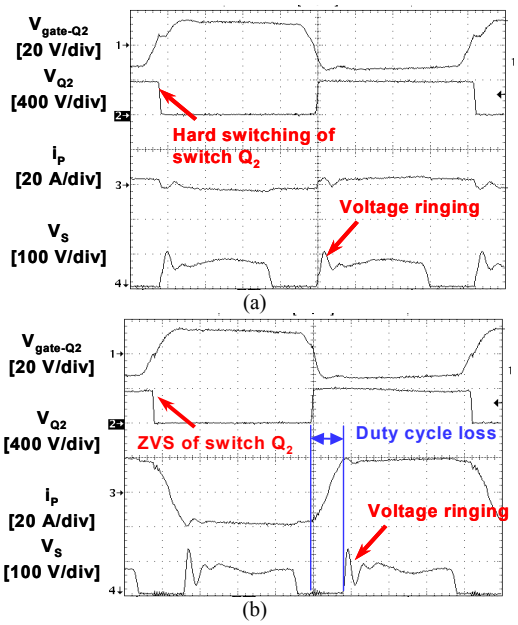


Fig. 8. Measured waveforms of the conventional phase-shifted FB converter at (a) $I_O$=2 A and (b) $I_O$=40 A. Time base: 1 µs/div.

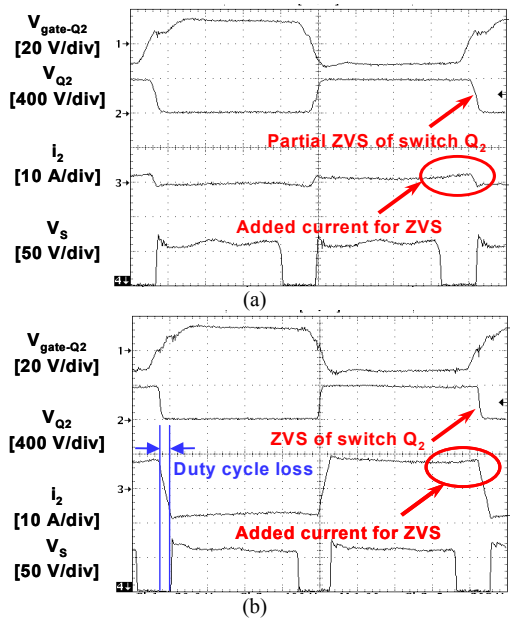


Fig. 9. Measured waveforms of the proposed converter at (a) $I_O$=2 A and (b) $I_O$=40 A. Time base: 1 µs/div.

The efficiency measurements for both the conventional phase-shifted FB ZVS converter and the proposed FB ZVS converter are summarized in Fig. 7. As can be seen in Fig. 7, the proposed converter shows a much higher efficiency than the conventional converter through the entire power (load-current) range. At full power the efficiency improvement is around 1.6%, which translates into a conduction loss reduction of more than 20%. In addition, by comparing secondary-winding voltage $V_S$ waveforms in Figs. 8 and 9, it can be seen that the conventional FB ZVS converter exhibits severe ringing, whereas the corresponding waveforms of the proposed FB ZVS converter show no ringing. Also, at full load ($I_O$=40 A), the conventional FB ZVS converter exhibits a much larger secondary-side duty cycle loss (Fig. 8(b)) compared to that of the proposed FB ZVS converter (Fig. 9(b)). For the proposed converter, the current through diodes $D_1$ and $D_2$ used to store energy for ZVS can be inferred from the current waveform of $i_2$, as indicated in Figs. 9(a) and (b). Finally, Fig. 10 shows the gate signals of PWM switches $Q_3$ and $Q_4$ along with their drain-to-source voltage waveforms confirming that these switches are turned on at zero voltage.

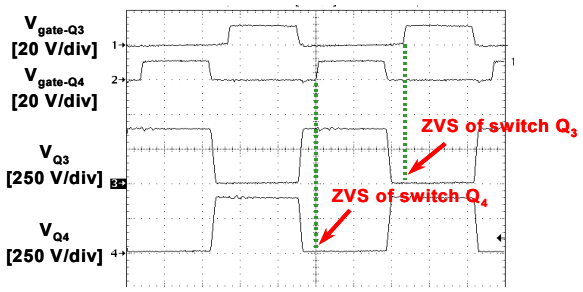


Fig. 10. Measured PWM switch waveforms of the proposed circuit at $I_O$=2A. Time base: 2 µs/div.

## IV. Summary

A new soft-switched FB converter that offers ZVS over a wide range of input voltage and output load has been described. The proposed constant-frequency converter that can be controlled by either phase-shift or variable duty-cycle PWM control achieves ZVS with substantially reduced duty cycle loss and no-load circulating energy.

The operation and performance of the proposed topology was verified on a 2-kW (48 V/40 A) experimental converter operating at 120 kHz from a 380-V dc input. The measured full-load efficiency improvement with respect to the conventional FB ZVS converter was around 1.6%.

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