Closed-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters

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***Abstract* - In this paper, a systematic overview of PLL-based closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters is presented. It is shown that the PLL-based closed-loop methods always provide stable operation, unlike the open-loop control methods, where the only method which results in stable operation is the slave synchronization to the turn-on instant of the master with current-mode control. It is also shown that the dynamic response of the PLL-based closed-loop methods with master-slave approach and democratic approach is almost identical. Experimental results obtained on a 300-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic, PLL-based closed-loop method is also provided.**

I. INTRODUCTION

In off-line power supplies that require active power factor correction (PFC), a boost converter operating at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) is a widely employed topology at low power levels (up to 200-300 W) [1]-[4]. The major benefit of the DCM/CCM boundary boost PFC converter, compared to the CCM boost PFC converter, is that the reverse-recovery losses of the boost diode are eliminated [5]. In addition, turn-on with zero-voltage switching (ZVS) of the boost switch or near ZVS (also called valley switching) can be easily achieved. Other benefits of the DCM/CCM boundary boost PFC converter compared to the constant-switching-frequency DCM boost PFC converter are a lower total-harmonic distortion (THD) of the line current, and a smaller peak inductor current resulting in lower turn-off switching losses and lower conduction losses [6]. Although the DCM/CCM boundary boost PFC converter exhibits a smaller peak inductor current than the DCM boost PFC converter, its peak inductor current is still twice its average current, which often necessitates a large differential mode (DM) electromagnetic interference (EMI) filter [9]. Another drawback is that its switching frequency, which changes with the instantaneous line voltage and the output power, varies over a wide range

Generally, the input current ripple and, consequently, the input DM-EMI filter can be significantly reduced by interleaving two or more boost PFC converters as shown in Fig. 1 [7]-[21]. In addition, the output current ripple can also be significantly reduced, resulting in a reduced equivalent-series-resistance (esr) loss of the output capacitor, and possibly a reduction in capacitor volume. Another benefit of interleaving is that the efficiency at lighter loads can be increased by employing phase shedding, i.e., by progressively turning off converters as the load is decreased.

By interleaving two or more DCM/CCM boundary boost converters, the benefits of DCM/CCM boundary boost PFC converters mentioned above can be extended to higher power levels. However, since the switching frequency is variable, the synchronization of interleaved DCM/CCM boundary boost PFC converters presents a challenging task.

Very few implementations of the interleaved DCM/CCM boundary boost PFC converters have been published in the literature [9]-[21]. All of the previously published implementations except one [20] are based on a master-slave relationship, where the master converter operates as a stand-alone converter, whereas, the slave converter is partially controlled by the master in order to achieve proper interleaving, i.e., a proper phase shift with respect to the master. It has been shown that the slave converter can be synchronized to the master converter with an open-loop method [9]-[14], i.e., by generating a time delay equal to half the switching period of the master determined from its previous switching cycle, or with a closed-loop method [15]-[17], [21], i.e., by measuring the phase difference between the converters and adjusting the phase of the slave based on the phase error. The slave converter with open-loop synchronization can be synchronized to the turn-on instant of the master converter [10]-[13] or to the turn-off instant of the master converter [9], [14]. In both cases, the converters can operate either with current-mode control or with voltage-mode

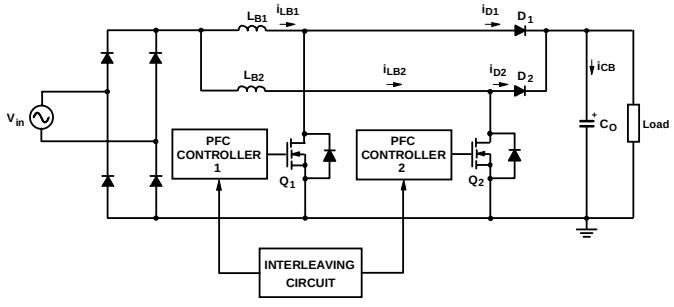

Fig. 1 Basic topology of two interleaved PFC boost converters.

control. A detailed analysis of the open-loop synchronization methods of the slave converter to the master converter is presented in [18]. It is shown in [18] that among the open-loop synchronization methods, only the method when the slave is synchronized to the turn-on instant of the master with current-mode control can provide a stable operation. The slave converter with closed-loop synchronization has been synchronized to the master converter by using a phase-locked-loop (PLL) approach. The PLL approach has been implemented by using a low-pass filter [15]-[17] or a cycle-by-cycle instant averaging filter [21], and then adjusting the turn-off instant of the slave converter. Although PLL-based closed-loop methods where the turn-on instant of the converter(s) is adjusted can be implemented, they are, generally, not attractive because of the additional complexity needed to achieve valley switching. In [20], instead of the master-slave PLL interleaving, a democratic PLL interleaving is employed, where the turn-off instant of both converters is adjusted proportionally to the phase error. In fact, in [20], the phase shift between the two converters is measured the same way as in the master-slave PLL method. However, unlike the master-slave method, where only the slave's turn-off instant is adjusted, in the democratic method, the turn-off instant of both converters is adjusted in equal but opposite directions.

In this paper, a systematic overview of the PLL-based closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters is presented. It is shown that the PLL-based closed-loop methods where the turn-off instant of the converter(s) is adjusted always provide stable operation. The dynamic response of the PLL-based closed-loop methods with master-slave approach and democratic approach is compared using simulations and it is shown that their dynamic response is almost identical. Experimental results obtained on a 300-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic PLL-based closed-loop method are also provided.

II. Overview of PLL-Based Closed-Loop Interleaving Methods

The block diagram and key waveforms of the PLL-based control circuit with master-slave approach of two interleaved DCM/CCM boundary boost PFC converters are presented in Figs. 2 and 3, respectively. The phase difference between the gate-drive signals of the master and slave converters is sensed by a positive-edge triggered SR flip-flop. The output voltage of the SR flip-flop, $v_{\Delta\phi}$, is averaged by a low-pass filter, which can be implemented by using either a simple RC filter or a cycle-by-cycle instant averaging filter. For simplicity, cycle-by-cycle instant averaging of voltage $v_{\Delta\phi}$ is shown in Fig. 3, where the averaged voltage $v_{\Delta\phi av}$ is constant over a switching cycle. The averaged voltage $v_{\Delta\phi av}$ is compared to a reference voltage (V_{CC}/2) that corresponds to the desired phase

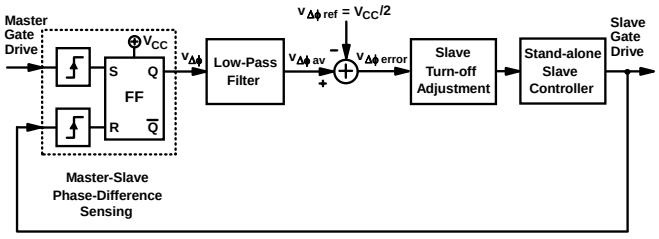

Fig. 2 Block diagram of PLL-based control circuit with master-slave interleaving method of two DCM/CCM boundary boost PFC converters.

difference of 180° between the gate-drive signals of the master and slave converters. The phase-error voltage $v_{\Delta\phi error}$ is used to adjust the turn-off instant of the slave converter.

When the phase shift of the slave's gate signal with respect to the master's gate signal is 180°, i.e., $T_{\Delta\phi} = T_{sw}/2$, the phase error voltage $v_{\Delta\phi error} = 0$ (solid lines in Fig. 3). When $T_{\Delta\phi} > T_{sw}/2$, $v_{\Delta\phi error} > 0$ (dashed lines in Fig. 3).

Both the master and slave converters can operate either with voltage-mode or current-mode control. In both control methods, the turn-off instant of the slave converter can be adjusted either by modifying the level of the slave's feedback error voltage or by modifying the slope of the slave's ramp signal as illustrated in Fig. 4. It should be noted that both the master and slave converters turn on with valley switching after zero-current detection (ZCD) of their respective inductor currents.

An implementation of the PLL-based control circuit with master-slave approach of two interleaved DCM/CCM boundary boost PFC converters when the turn-off instant of the slave converter is adjusted by modifying the level of the slave's feedback error voltage is shown in Fig. 5, and by modifying the slope of the slave's voltage ramp is shown in Fig. 6.

In Fig. 5, the slave's feedback error voltage is obtained as

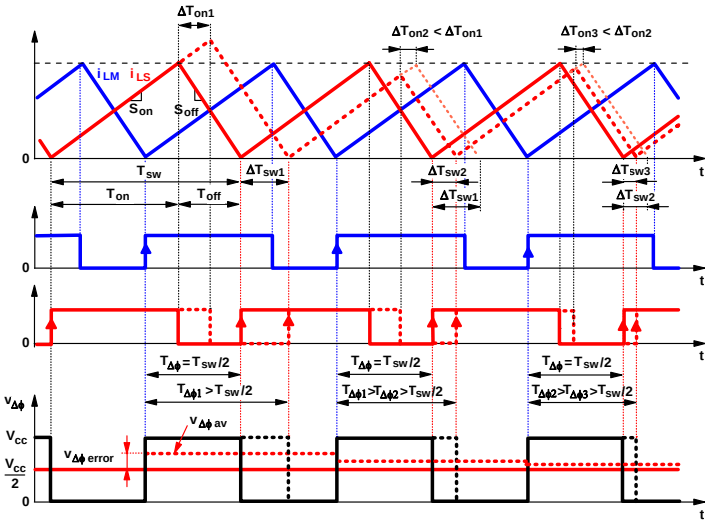

Fig. 3 Key waveforms of PLL-based control circuit with master-slave interleaving method of two DCM/CCM boundary boost PFC converters.

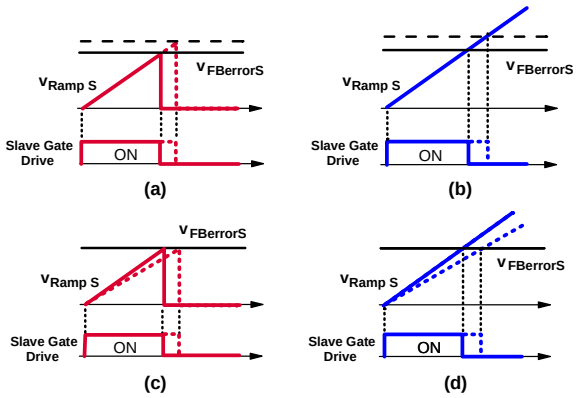

Fig. 4 Adjustment of turn-off instant of slave converter by modifying the level of slave's feedback error voltage when operating with (a) current-mode (b) voltage-mode control, or by modifying the slope of slave's ramp signal when operating with (c) current-mode, (d) voltage-mode control.

$$v_{FBerrorS} = v_{FBerror} + \Delta v_{FBerrorS} \quad , \tag{1}$$

where the adjustment voltage is

$$\Delta v_{FBerrorS} = R_2 \cdot i_{\Delta\phi error} \quad . \tag{2}$$

The phase-error current $i_{\Delta\phi error}$ is proportional to the phase-error voltage $v_{\Delta\phi error}$, i.e.,

$$i_{\Delta\phi error} = -\frac{2}{R_1} \cdot v_{\Delta\phi error} \quad . \tag{3}$$

Substituting (3) in (2), the adjustment of the slave's feedback error voltage is obtained as

$$\Delta v_{FBerrorS} = -\frac{2R_2}{R_1} \cdot v_{\Delta\phi error} \quad . \tag{4}$$

When $T_{\Delta\phi} > T_{sw}/2$, $v_{\Delta\phi error} > 0$, and $i_{\Delta\phi error} < 0$, resulting in a reduced level of the slave's feedback error voltage and, consequently, in a reduced on time of the slave converter and in a reduced phase shift of the slave's gate signal with respect to the master's gate signal, as shown in Fig. 3.

In Fig. 6, the slope of the slave's voltage ramp is obtained as

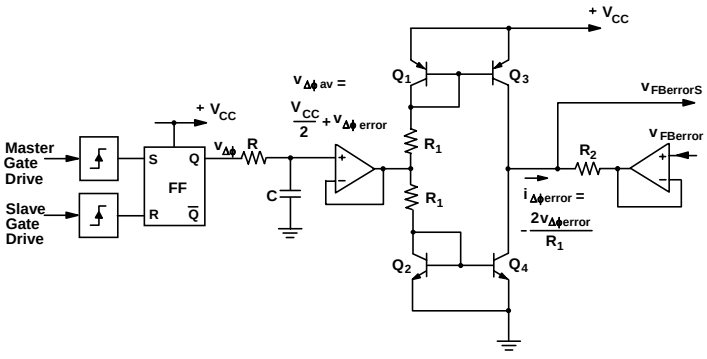

Fig. 5 Implementation of PLL-based control circuit with master-slave interleaving method of two DCM/CCM boundary boost PFC converters that operate with either voltage-mode or current-mode control, when the turn-off instant of the slave converter is adjusted by modifying the level of the slave's feedback error voltage.

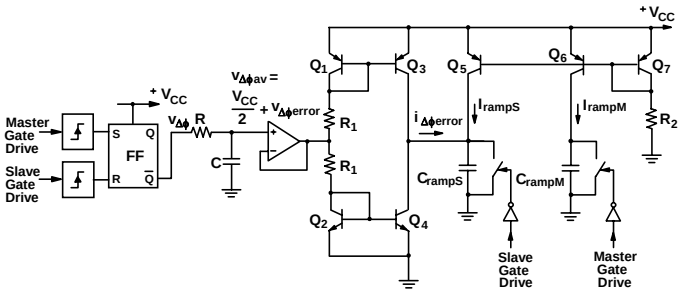

Fig. 6 Implementation of PLL-based control circuit with master-slave interleaving method of two DCM/CCM boundary boost PFC converters that operate with voltage-mode control, when the turn-off instant of the slave converter is adjusted by modifying the slope of the slave's voltage ramp.

$$\frac{dv_{rampS}}{dt} = \frac{I_{rampS} + i_{\Delta\phi error}}{C_{rampS}} \quad , \tag{5}$$

where the phase error current $i_{\Delta\phi error}$ is defined again by (3). However, the phase-error voltage $v_{\Delta\phi error}$ in Fig. 6 has an opposite sign compared to that in Fig. 5 because in Fig. 6 the input of the low-pass filter is connected to the $\overline{Q}$ output of the SR flip-flop. Therefore, when $T_{\Delta\phi} > T_{sw}/2$, $v_{\Delta\phi error} < 0$, and $i_{\Delta\phi error} > 0$, resulting in an increased slope of the slave's voltage ramp and, consequently, again in a reduced on time of the slave converter and in a reduced phase shift of the slave's gate signal with respect to the master's gate signal.

It should be noted that the implementation of the PLL-based control circuit in Fig. 5 is applicable for both voltage-mode and current-mode control, whereas, Fig. 6 illustrates a voltage-mode implementation. A simplified current-mode implementation corresponding to Fig. 6 is presented in Fig. 13.

The block diagram of the PLL-based control circuit with democratic approach of two interleaved DCM/CCM boundary boost PFC converters is presented in Fig. 7. The key difference between the master-slave and democratic approaches is that the phase-error voltage $v_{\Delta\phi error}$ is applied to each converter with an equal but opposite sign, to adjust the turn-off instant of the corresponding converters. It follows from Fig. 7 that the control circuit with democratic approach is a natural extension of the control circuit with master-slave

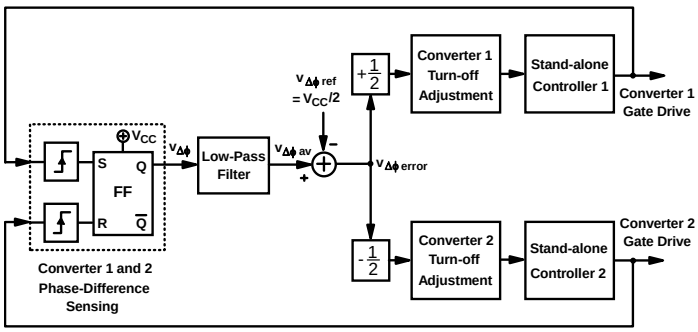

Fig. 7 Block diagram of PLL-based control circuit with democratic interleaving method of two interleaved DCM/CCM boundary boost PFC converters.

approach and, therefore, all the implementations presented in Figs. 5, 6, and 13 are applicable with minor modifications.

III. Analysis of PLL Loop Stability

The stability of PLL loops can be analyzed by deriving a small-signal model based on the perturbed waveforms such as those in Fig. 3 and by verifying through simulation. To illustrate this method, the master-slave type PLL loop with cycle-by-cycle instant averaging filter was selected, where the turn-off instant of the slave converter is adjusted by modifying the level of the slave's feedback error voltage, and where the converters operate with voltage-mode control. The stability of more complex PLL loops was analyzed only through simulation.

Considering the perturbed waveforms in Fig. 3 and referring to (4), the following relationships can be obtained.

$$\Delta T_{sw1} = \left(1+\frac{S_{on}}{S_{off}}\right)\cdot\Delta T_{on1} = \frac{1}{1-\frac{v_{in}}{V_o}}\cdot\Delta T_{on1} \quad , \tag{6}$$

$$\Delta T_{sw1} \rightarrow v_{\Delta\phi error1} \rightarrow \Delta v_{FBerrorS1} \rightarrow \Delta T_{on2} \quad , \tag{7}$$

$$\Delta T_{sw2} = \Delta T_{sw1} + \frac{1}{1-\frac{v_{in}}{V_o}}\cdot\Delta T_{on2} \quad . \tag{8}$$

It should be noted in Fig. 3 that $\Delta T_{on2} < 0$ and, therefore, $\Delta T_{sw2} < \Delta T_{sw1}$. For the k-th perturbed switching cycle,

$$\Delta T_{sw(k)} = \Delta T_{sw(k-1)} + \frac{1}{1-\frac{v_{in}}{V_o}}\cdot\Delta T_{on(k)} \quad , \tag{9}$$

$$\Delta T_{sw(k)} \rightarrow v_{\Delta\phi error(k)} \rightarrow \Delta v_{FBerrorS(k)} \rightarrow \Delta T_{on(k+1)} \quad . \tag{10}$$

Based on (6)-(10), the corresponding PLL loop can be represented in the s-domain as shown in Fig. 8, where $S_{\Delta\phi error}$ is the slope of the voltage ramp for converting ΔT_{sw} to phase-error voltage $v_{\Delta\phi error}$, S_{PWM} is the slope of the PWM voltage ramp, and G_{adj} is the gain of the slave's turn-off adjustment circuit defined by (4). The delay block $e^{-sT_{off}}$ represents the delay of the ΔT_{sw} perturbation with respect to the ΔT_{on} perturbation, whereas, $H_{SH}(s)$ is the sample and hold block,

$$H_{SH}(s) = \frac{1-e^{-sT_{sw}}}{sT_{sw}} \quad , \tag{11}$$

which represents the stair shape of phase-error voltage $v_{\Delta\phi error}$ in Fig. 3.

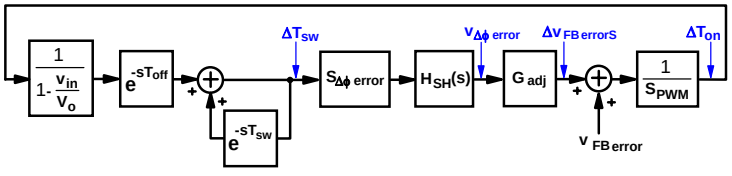

Fig. 8 Small-signal model of master-slave type PLL loop with cycle-by-cycle instant averaging filter, where the turn-off instant of slave is adjusted by modifying the slave's feedback error voltage, and where the converters operate with voltage-mode control.

If the PLL loop is much faster than the voltage loop, feedback error voltage $v_{FBerror}$ in Fig. 8 can be considered as constant and the loop gain is obtained as

$$LG_{PLL}(s) = \frac{K_{PLL}}{T_{sw}}\cdot\frac{1}{s}\cdot e^{-sT_{off}} \quad , \tag{12}$$

where

$$K_{PLL} = \frac{1}{1-\frac{v_{in}}{V_o}}\cdot\frac{S_{\Delta\phi error}}{S_{PWM}}\cdot G_{adj} \quad . \tag{13}$$

It follows from (13) that the PLL loop basically behaves as an integrator. The magnitude and phase of the loop gain (12) are shown in Fig. 9 (line with "o" symbol).

To verify the small-signal model in Fig. 8, SIMPLIS™ simulations were performed of a 400-V/280-W, 127-V_{dc} input, interleaved DCM/CCM boundary boost converter with a PLL-based voltage-mode control, where the slave's turn-off instant is adjusted by modifying the slave's feedback error voltage. The schematic of the simulation circuit is shown in Fig. 10, where the power stage and voltage loop error amplifier are not shown for simplicity. Figure 10 includes both an implementation of a cycle-by-cycle instant averaging filter, and an implementation of an RC filter, as well as a means of implementing either the master-slave or democratic interleaving method. The PLL loop gain was simulated by inserting ac voltage source v_{inj}.

The instant averaging filter was implemented by using a sawtooth oscillator and two sample and hold (S&H) circuits.

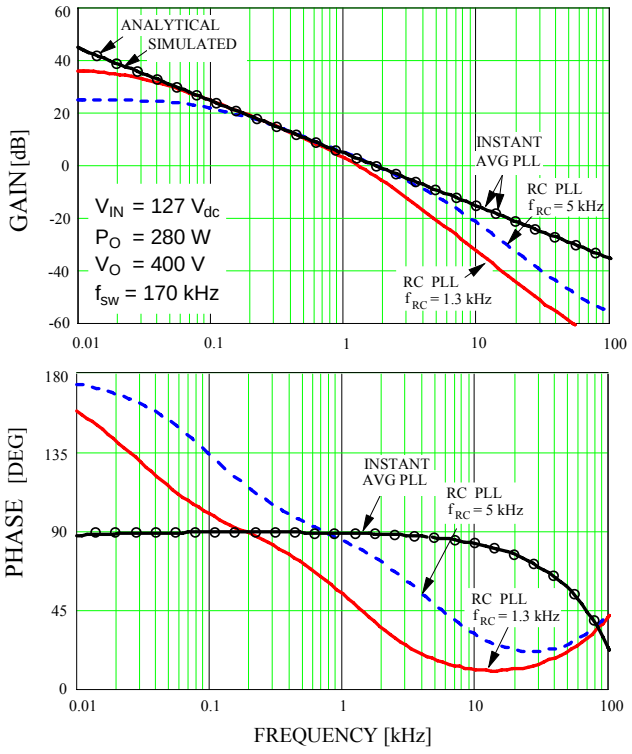

Fig. 9 Analytical and simulated PLL loop gain of master-slave interleaving method with voltage-mode control where the turn-off instant of slave is adjusted by modifying the slave's feedback error voltage.

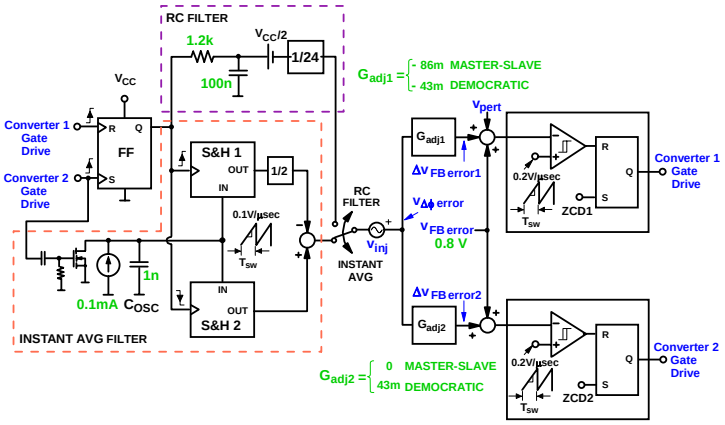

Fig. 10 Simulation subcircuit of a 400-V/280-W, 127 V_{dc} input, interleaved DCM/CCM boundary boost converter with PLL-based closed-loop control for both master-slave and democratic interleaving methods, where the turn-off instant is adjusted by modifying the feedback error voltage, and where the converters operate with voltage-mode control.

The sawtooth oscillator consists of a 100-μA current source and a 1-nF capacitor (C_{OSC}) which results in a constant slope, with synchronization to converter 2 through a MOSFET which discharges capacitor C_{OSC} at the rising edge of its gate drive signal after a short delay. Prior to discharging capacitor C_{OSC}, the peak of the sawtooth oscillator is sampled by S&H 1, which is triggered by the rising edge of the Q output of SR flip flop FF, and the value is divided by two. When converter 1 turns on, output Q goes low, and a sample of the sawtooth ramp is taken. Phase-error voltage $v_{\Delta\phi error}$ is obtained by subtracting the output of S&H 2 from half of the output of S&H 1, and therefore, it is proportional to the cycle-by-cycle instant average of output Q minus $V_{CC}/2$, and remains constant over half a switching cycle. Alternatively, the average can also be obtained using an RC filter, and voltage $v_{\Delta\phi error}$ can be obtained by subtracting $V_{CC}/2$. Voltage $\Delta v_{FBerror1}$ is obtained through gain G_{adj1}, which is set to -0.086 for the master-slave, and -0.043 for the democratic control method. Similarly, voltage $\Delta v_{FBerror2}$ is obtained through gain G_{adj2}, which is set to zero for the master-slave, and 0.043 for the democratic control method. Finally, voltages $\Delta v_{FBerror1,2}$ are summed with the output of the voltage error amplifier ($v_{FBerror}$), and compared to a PWM ramp with a 0.2-V/μsec slope in order to determine the on-time of each converter.

Simulation results for the master-slave interleaving methods are shown in Fig. 9. For the implementation with the cycle-by-cycle instant-averaging filter, the simulation results are in excellent agreement with the analytical results, as shown in Fig. 9, which verifies the proposed model. Figure 9 also includes simulations of the PLL loop gain using an RC filter with two reasonable filter bandwidths. It is shown that the loop gain with the RC filter, in addition to the integrator, also contains a pole at the RC-filter bandwidth as well as a limited low frequency gain. Since for the implementation with the cycle-by-cycle instant-averaging filter only one pole exists

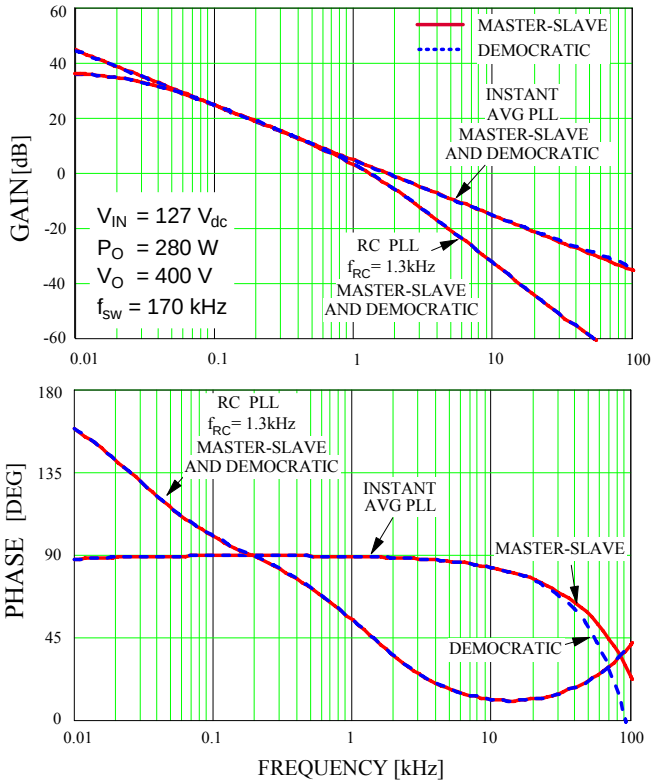

Fig. 11 Comparison of simulated PLL loop gains of master-slave and democratic interleaving methods with voltage-mode control where the turn-off instant is adjusted by modifying the feedback error voltage.

and for the implementation with the RC filter only two poles are apparent, it can be concluded that the PLL-based master-slave interleaving methods are always stable. Although the results in Fig. 9 were obtained for voltage-mode control where the turn-off instant of the slave is adjusted by modifying the slave's feedback error voltage, similar results can be obtained for current-mode control as well as for both voltage-mode and

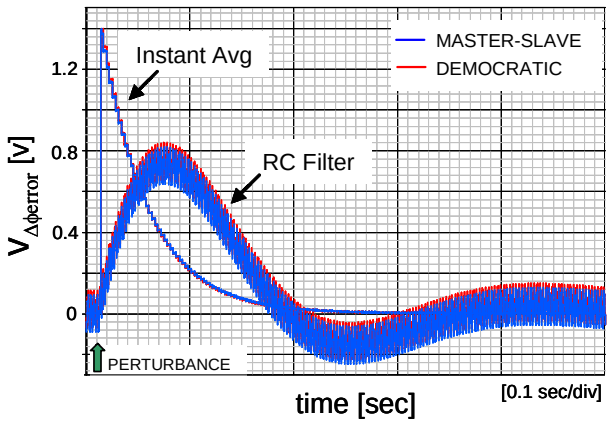

Fig. 12 Simulation of a perturbance of a 400-V/280-W, 127-V_{dc} input, interleaved DCM/CCM boundary boost converter with PLL-based closed-loop control for both master-slave and democratic interleaving methods, where the turn-off instant is adjusted by modifying the feedback error voltage, and where the converters operate with voltage-mode control. It should be noted that the waveforms of the master-slave and democratic methods are almost overlapping.

current-mode control methods with the adjustment of the slope of the slave's PWM ramp.

Simulation results comparing the stability of PLL loops of master-slave and democratic interleaving methods are shown in Fig. 11. It is shown in Fig. 11 that the PLL loop gain of the democratic interleaving method is nearly identical to that of the master-slave interleaving method except for a minor phase mismatching at high frequencies for the implementation with instant-averaging filter.

IV. Dynamic Response of PLL Loop

To compare the dynamic response of the implementations with instant-averaging filter and RC filter, time domain simulations were performed using the simulation circuit in Fig. 10. The results are presented in Fig. 12. A perturbation was injected using an 80-mV voltage pulse through voltage source v_{pert} in Fig. 10 to increase the feedback error voltage during a single switching cycle. It can be seen in Fig. 12 that the implementation with the instant-averaging filter recovers from the perturbation at least twice as fast as the implementation with the RC filter. It should be noted in Fig. 12 that the shape of the perturbed phase-error voltage is consistent with the order of the corresponding implementation. Fig. 12 also illustrates that the dynamic response of the master-slave and democratic interleaving methods is nearly identical.

Simulation results presented in Fig. 13 illustrate that the dynamic response of the master-slave and democratic interleaving methods remains nearly identical when an ac input voltage is applied. The SIMPLIS™ simulation circuit, shown in Fig. 14, modeled a 385-V/250-W, universal input, interleaved DCM/CCM boundary boost PFC converter that operates with a PLL-based current-mode control circuit, where the turn-off instant is adjusted by modifying the slope of the current sense ramp. The PLL low-pass filter is an RC filter. The power stage and voltage loop error amplifier are not shown in Fig. 14 for simplicity.

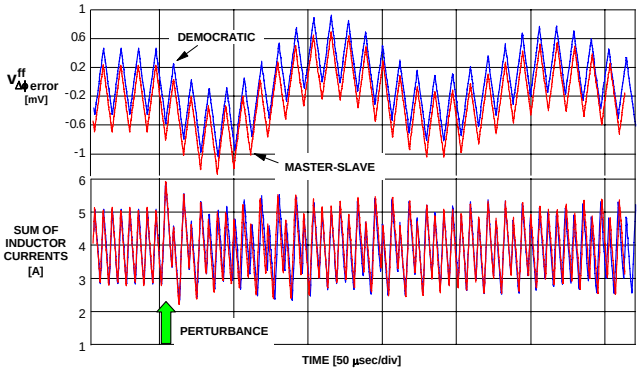

Fig. 13 Simulation of a perturbance of a 385-V/250-W, universal input, interleaved DCM/CCM boundary boost PFC converter with PLL-based closed-loop control for both master-slave and democratic interleaving methods where the turn-off instant is adjusted by modifying the slope of the current-sense voltage ramp, and where the converters operate with current-mode control.

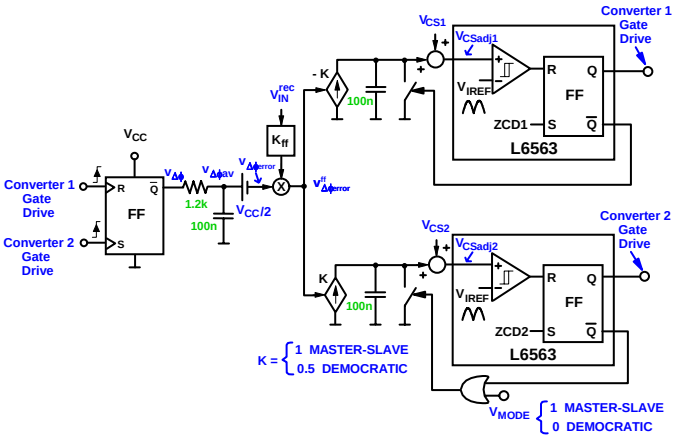

Fig. 14 Simulation circuit of a 385-V/250-W, universal input, interleaved DCM/CCM boundary boost PFC converter with PLL-based closed-loop control for both master-slave and democratic interleaving methods, where the turn-off instant is adjusted by modifying the slope of the current-sense voltage ramp, and where the converters operate with current-mode control.

The simulation circuit in Fig. 14 is based on the L6563 controller from ST Microelectronics, which operates with a master-slave relationship when mode selection voltage V_{MODE} = 1, and which operates with a democratic relationship when V_{MODE} = *0*. It should be noted that transconductance gain *K* is set to 1 when operated with a master-slave relationship, and 0.5 when operated with a democratic relationship. The slope adjustment is accomplished by making the added voltage ramp proportional to rectified input voltage v_{IN}^{rec} so that adjusted current sense ramp v_{CSadj} is proportional to rectified input voltage v_{IN}^{rec} .

The dynamic response was tested by perturbing the reference current of converter 1, i.e., by increasing the level of feedback voltage of converter 1 by 100 mV for a single switching cycle at the peak of the input voltage, at full load and V_{IN} = 90 V_{RMS}. As illustrated in Fig. 13, the sum of inductor currents i_{LB1} and i_{LB2}, and, voltage $v_{\Delta\phi error}^{ff}$ both show that the perturbation damps with a settling time related to the PLL RC filter time constant. It should be noted that this control method, namely, synchronization to the turn-off instant with current-mode control, is unstable when implemented with open-loop control, as shown in [18].

Finally, experimental results shown in Fig. 15 verify the stability of the interleaved DCM/CCM boundary boost PFC converters with PLL-based closed-loop control by observing the inductor current waveforms during a line cycle. The experimental results were obtained on a 385-V/300-W, universal input range, interleaved prototype converter implemented with the UCC28061 interleaving IC controller [22]. The prototype operates with voltage mode control using a democratic approach with turn-off synchronization. It is shown in Fig. 15 that interleaving is lost around the zero crossing of the line voltage, which can be considered as a natural perturbation, and that interleaving is restored around the peak of the line voltage.

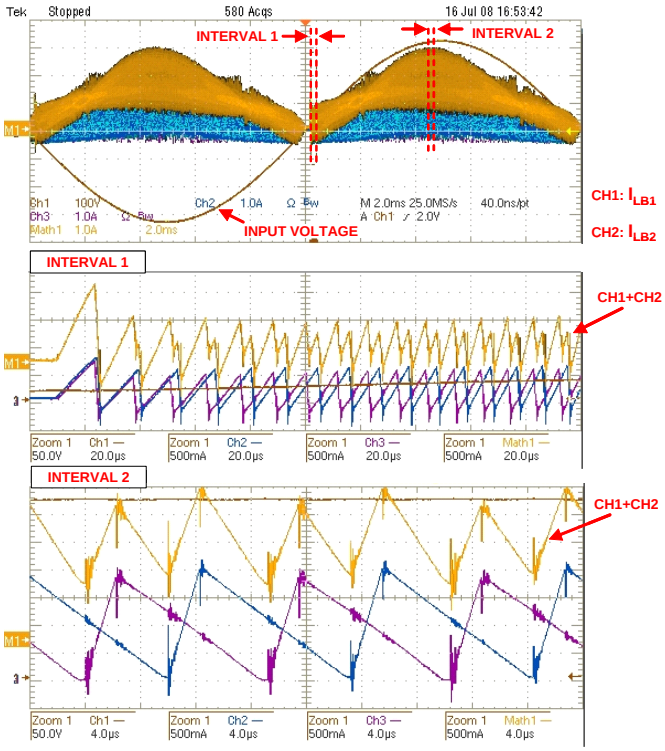

Fig. 15 Measurements of a 385-V/300-W, universal input, interleaved DCM/CCM boundary boost PFC converter with PLL-based closed-loop control circuit using democratic interleaving method, where the converters operate with voltage-mode control.

V. Summary

An overview of PLL-based closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters is presented. It is shown in both the frequency and time domain that the PLL-based closed-loop methods, implemented with either voltage-mode or current-mode control, always provide stable operation. It is also shown that the dynamic response of the PLL-based closed-loop methods with master-slave approach and democratic approach is almost identical. Experimental results obtained on a 300-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit with a dedicated controller IC utilizing a democratic, PLL-based closed-loop method is also provided.

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