Design-Oriented Analysis and Performance Evaluation of Buck PFC Front-End

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Abstract - In universal-line ac/dc converters that require PFC, maintaining a high efficiency across the entire load range poses a major challenge. Typically, a boost PFC front-end exhibits 1-3% lower efficiency at 100-V line compared to that at 230-V line. It is shown in this paper that a buck PFC front end with an output voltage in the 80-V range can maintain a high-efficiency across the entire line range. A thorough analysis of the buck PFC converter operation and performance along with design optimization guidelines are presented. Experimental results obtained on a 90-W notebook adapter are provided.

I. Introduction

Until recently, efficiency increases of power conversion circuits were primarily driven by increased power density requirements since power density increases are only possible if appropriate incremental improvements in full-load efficiency are achieved so that the thermal and acoustic performance are not adversely affected. Today, the power supply industry is at the beginning of a major focus shift that puts efficiency improvements across the entire load range in the forefront of customers' performance requirements. This focus on efficiency has been prompted by economic reasons and environmental concerns caused by the continuous, aggressive growth of the Internet infrastructure and a relatively low energy efficiency of power delivery systems of large Internet-equipment hosting facilities.

Currently, minimum efficiencies of power supplies for computer, telecom, and networking equipment at different load levels have been defined in a number of voluntary specifications. Specifically, the minimum efficiencies of external power supplies (adapters) have been defined in U.S. Environmental Protection Agency's (EPA) Energy Star specifications [1], as well as in the European Code of Conduct (CoC) document [2]. Across-the-load efficiencies of desktop, workstation, and desktop-derived server power supplies were originally defined in the 80Plus specifications [3], which since July 20, 2007 have been incorporated into a corresponding Energy Star document [4]. However, with a recent launch of the Climate Saver Computing Initiative (CSCI) [5] led by Intel and Google, the very challenging CSCI efficiency specifications have been emerging as the major efficiency standard for multiple-output and single-output desktop, workstation, and server power supplies. For the time being, the CSCI spec defines minimum efficiencies at 80%, 50%, and 20% of full load with a peak efficiency at 50% load measured at both 115-V and 230-V line [5]. However, it is very likely that the current spec will be amended in the near future to include a 10%-load efficiency requirement, as well as minimum power factor at the defined load levels.

Generally, the optimization of efficiency in the entire load and line ranges boils down to finding a right balance between switching and conduction losses because the full load efficiency is predominantly determined by conduction loses of semiconductor and magnetic components, whereas light load efficiencies are in the most part determined by switching losses of semiconductors and core losses of magnetic components. As a result, the key steps in achieving high efficiencies in the entire load range are the selection of appropriate power supply architectures and topologies, selection of most suitable semiconductor devices, optimization of magnetic devices, packaging, and power management.

In universal-line (90-264-V) ac/dc converters that require PFC, maintaining a high efficiency across the entire load range poses a major challenge. Typically, a boost PFC front-end exhibits 1-3% lower efficiency at 100-V line compared to that at 230-V line. This drop of efficiency at low line can be attributed to the increased input current that produces higher losses in semiconductors and input EMI filter components.

Another drawback of the universal-line boost PFC front end is related to its relatively high output voltage, typically in the 380-400-V range. This high voltage not only has a detrimental effect on the switching losses of the boost converter, but also on the switching losses of the primary switches of the downstream dc/dc output stage and the size and efficiency of its isolation transformer.

At lower power levels, i.e., below 300-350 W, the drawbacks of the universal-line boost PFC front-end may be overcome by implementing the PFC front-end with the buck topology. As it is shown in this paper, the universal-line buck PFC front end with an output voltage in the 80-V range maintains a high-efficiency across the entire line range. In addition, a lower input voltage to the dc/dc output stage has beneficial effect on its performance because the dc/dc stage can be implemented with lower-voltage-rated semiconductor devices and optimized loss and size of the transformer.

The buck PFC converter operation in both DCM and CCM mode were described first in [6]. Additional analysis and circuit refinements were described in [7]-[14]. Because the buck PFC converter does not shape the line current around the zero crossings of the line voltage, i.e., during the time intervals when the line voltage is lower than the output voltage, as shown in Fig. 1, it exhibits increased THD and lower power factor compared to its

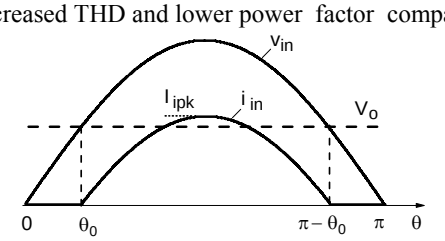

Fig. 1 Ideal input voltage and input current waveforms of CCB PFC

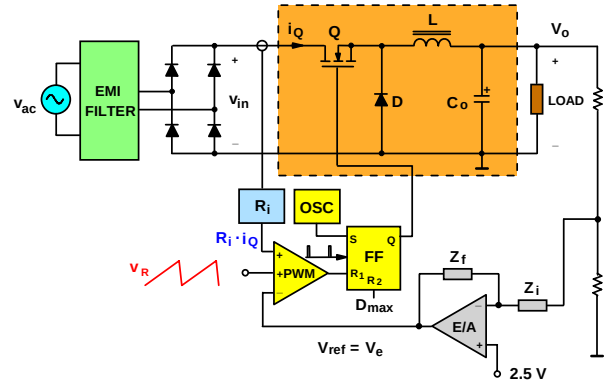

Fig. 2 Circuit diagram of CCB PFC

boost counterpart. As a result, in applications where IEC61000-3-2 and corresponding Japanese specifications need to be met, the buck converter PFC employment is limited to lower power levels. A simple control circuit for the buck PFC converter, suitable for cost-sensitive applications, is the clamped-current-mode control circuit [15]. The basic concept of the clamped-current buck PFC, shown in Fig. 2, is similar to that of the clamped-current boost PFC [16].

In this paper, a thorough analysis of the clamped-current buck PFC converter operation and performance along with design optimization guidelines are presented. Experimental results obtained on a 90-W notebook adapter with buck PFC are provided.

II. Analysis of Clamped-Current Buck PFC

The analysis of the clamped-current buck (CCB) PFC shown in Fig. 2 is performed assuming the following.

1) The input voltage is a full-wave rectified sine wave, i.e., $v_{in} = V_{im}\left|\sin(\omega_L t)\right| = V_{im}\left|\sin(\theta)\right|$, where V_{im} is the amplitude and $\omega_L = 2\pi f_L$ is the line frequency.
2) The output voltage V_o is constant, i.e., it has a negligible ac ripple.
3) The switching frequency f_{sw} is constant and much greater than the line frequency f_L, so that the input voltage can be considered constant during a switching cycle (quasi-static approach).
4) The reference voltage V_{ref} to the PWM modulator is constant during each half of a line cycle, because the bandwidth of the output-voltage loop is much smaller than the rectified line frequency ($2f_L$).
5) The phase-shift of the line current caused by the input filter can be neglected.

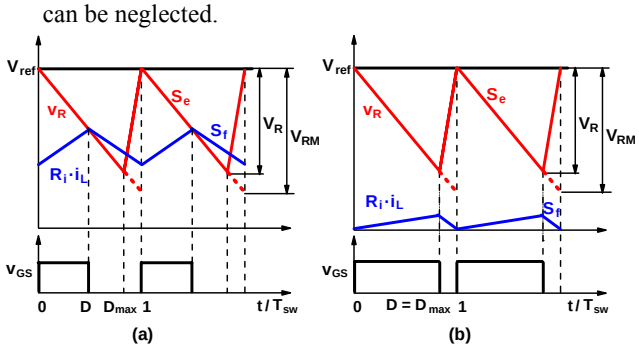

Fig. 3 Reference voltage V_{ref}, slope-compensation-ramp v_R, sensed voltage $R_i \cdot i_L$, and duty cycle of CCB PFC: switch turns off when (a) $R_i \cdot i_L$ reaches $V_{ref} - v_R$; (b) when duty cycle D reaches D_{max}

Within a half line cycle, the input current can flow only when the input voltage is greater than the output voltage. The conduction angle of the input current is equal to $\pi - 2\theta_0$, where $\theta_0 = \text{asin}(V_o/V_{im})$.

The conduction of switch Q in Fig. 2, is initiated by the oscillator of the control circuit. The switch is turned off either when sensed voltage $R_i \cdot i_L$ reaches the difference between reference voltage $V_{ref} = V_e$ and slope-compensation-ramp voltage v_R, i.e.,

$$R_i \cdot i_L = V_{ref} - v_R \tag{1}$$

as shown in Fig. 3(a), or when the duty cycle of switch Q reaches its preset maximum value D_{max}, as illustrated in Fig. 3(b). Note that in practical circuits, sensing of inductor current i_L is implemented by sensing the switch current i_Q since during on-time $i_L = i_Q$.

The buck inductor can operate in both the discontinuous-conduction mode (DCM) and continuous-conduction mode (CCM). Depending on which event terminates the conduction of Q in a switching cycle, two discontinuous and two continuous conduction modes of operation are possible. In this paper, the DCM and CCM where Q turns off when the switch duty ratio reaches D_{max}, Fig. 3(b), are denoted as DCM1 and CCM1, respectively. Similarly, the DCM and CCM in which sensed voltage $R_i \cdot i_L$ reaches the difference voltage $V_{ref} - v_R$, Fig. 3(a), are denoted as DCM2 and CCM2, respectively. From the two CCM's, only CCM2 will be considered since CCM1 usually encompasses only a few switching cycles with fast rising or falling edges of the inductor current, which can be approximated with vertical segments, as shown in Fig. 4 (input current waveforms at $k_S = 0.5$ and $k_S = 1$). Depending on the line and load conditions, five different sequences of the operation modes, called Mode Sequences (MS's), can be distinguished. The five MS's are summarized in Table I.

Expressions for the input current waveforms in the five operation modes as well as expressions for the boundary angles between the operation modes are derived next. Since it is more convenient to perform these derivations by using current signals instead of voltage signals, reference current I_{ref} and slope-compensation-ramp current i_R are defined from (1) as

$$i_L = \frac{V_{ref}}{R_i} - \frac{v_R}{R_i} = I_{ref} - i_R \quad . \tag{2}$$

The input current is equal to the switch current averaged over a switching cycle, i.e., $i_{in}(t) = \left\langle i_Q(t) \right\rangle_{Tsw}$.

To obtain the expressions for the input current and boundary angles, the slope of the compensation ramp should be determined first.

A. Slope Compensation Ramp

To ensure the stability of the current loop, the slope of the compensation (external) ramp, S_e^i, should be at least 50% of the maximum down slope of the inductor current in CCM2, $S_{f,\max}^i$, i.e.,

$$S_e^i = k_S \cdot S_{f,\max}^i, \quad k_S \geq 0.5 \quad . \tag{3}$$

From Fig. 3(a) the slope of the compensation ramp is

$$S_e^i = \frac{I_R}{D_{\max} T_s} = \frac{I_{RM}}{T_s} \quad . \tag{4}$$

TABLE I
MODE SEQUENCES OF CCB PFC

MODE SEQUENCE	OPERATION MODE			MS CONDITION [See Eqs. (35) and (37)]			BOUNDARY ANGLE [See Eq. (28)]	
	DCM1	DCM2	CCM2				Θ_{DD}	Θ_{DC}
MS1		+		$I_{ref} < I_R$	$I_{ref} < I_{refCCM2}$		Θ_0	$\pi/2$
MS2		+	+		$I_{ref} > I_{refCCM2}$		Θ_0	Θ_{D2C2}
MS3	+	+		$I_{ref} \geq I_R$	$I_{ref} < I_{refCCM2}$		Θ_{D1D2}	$\pi/2$
MS4	+		+		$I_{ref} > I_{refCCM2}$	$I_{ref} > I_{refD1C2}$	Θ_{D1C2}	Θ_{D1C2}
MS5	+	+	+			$I_{ref} < I_{refD1C2}$	Θ_{D1D2}	Θ_{D2C2}

The down-slope of the ind. current in CCM2 is constant, i.e.,

$$S^i_{f,\max} = S^i_f = \frac{V_o}{L} \quad . \tag{5}$$

Substituting (4) and (5) into (3), the amplitude of the compensation ramp is obtained as

$$I_{RM} = \frac{k_S V_o}{L f_{sw}} \quad . \tag{6}$$

B. Discontinuous Conduction Mode

In DCM, the input current is obtained as

$$i_{in,DCM} = D_{DCM} \cdot \frac{i_{L,pk,DCM}}{2} \quad , \tag{7}$$

where, $i_{L,pk,DCM}$ is the peak of the inductor current defined as

$$i_{L,pk,DCM} = D_{DCM} \cdot \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{L f_{sw}} \quad . \tag{8}$$

Substituting (8) into (7), the input current in DCM is determined as

$$i_{in,DCM} = D^2_{DCM} \cdot \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{2 L f_{sw}} \quad . \tag{9}$$

Specifically, in DCM1,

$$D_{DCM1} = D_{\max} \quad , \tag{10}$$

and by substituting (10) into (9), the final expression for the input current in DCM1 is

$$i_{in,DCM1} = D^2_{\max} \cdot \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{2 L f_{sw}} \quad . \tag{11}$$

It should be noted in (11) that in DCM1, the input current is proportional to the input-output voltage difference.

In DCM2, the peak of the inductor current is defined as

$$i_{L,pk,DCM2} = I_{ref} - I_{RM} D_{DCM2} \quad . \tag{12}$$

Combining (18) and (12), the duty cycle in DCM2 is obtained as

$$D_{DCM2} = \frac{I_{ref} L f_{sw}}{V_{im}\left|\sin(\omega_L t)\right| - V_o + I_{RM} L f_{sw}} \quad . \tag{13}$$

By substituting (13) into (9),), the final expression for the input current in DCM2 is

$$i_{in,DCM2} = \frac{I^2_{ref} L f_{sw}}{2} \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{\left[V_{im}\left|\sin(\omega_L t)\right| - V_o + I_{RM} L f_{sw}\right]^2} \quad . \tag{14}$$

It should be noted in (14) that in DCM2, the input current is proportional to the input-output voltage difference if

$$V_{im}\left|\sin(\omega_L t)\right| - V_o << I_{RM} L f_{sw} \quad . \tag{15}$$

Condition (15) can be rewritten by using (6) as

$$V_{im}\left|\sin(\omega_L t)\right| << (1 + k_S) V_o \quad . \tag{16}$$

In the opposite case when

$$V_{im}\left|\sin(\omega_L t)\right| >> (1 + k_S) V_o \quad , \tag{17}$$

the input current in DCM2 is approximately constant.

C. Continuous Conduction Mode

In CCM2, the input current is obtained as

$$i_{in,CCM2} = D_{CCM2}\left(i_{L,pk,CCM2} - \frac{\Delta i_{L,CCM2}}{2}\right) \quad , \tag{18}$$

where

$$i_{L,pk,CCM2} = I_{ref} - I_{RM} D_{CCM2} \quad , \tag{19}$$

$$\Delta i_{L,CCM2} = D_{CCM2} \cdot \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{L f_{sw}} \quad , \tag{20}$$

and

$$D_{CCM2} = \frac{V_o}{V_{im}\left|\sin(\omega_L t)\right|} \quad . \tag{21}$$

By substituting (19)-(21) into (18), the input current in CCM2 can be expressed as

$$i_{in,CCM2} = i_{in,CCM21} + i_{in,CCM22} \quad , \tag{22}$$

where

$$i_{in,CCM21} = I_{ref} \cdot \frac{V_o}{V_{im}\left|\sin(\omega_L t)\right|} \quad , \tag{23}$$

and

$$i_{in,CCM22} = -\left(I_{RM} + \frac{V_{im}\left|\sin(\omega_L t)\right| - V_o}{2 L f_{sw}}\right) \cdot \frac{V_o^2}{\left(V_{im}\left|\sin(\omega_L t)\right|\right)^2} \quad . \tag{24}$$

It should be noted in (22)-(24) that in CCM2, the input current has one positive and two negative components. Although the individual components of the input current in CCM2 are inversely proportional to the line voltage, or to the square of the line voltage, in a proper design, the total input current in CCM2 monotonically follows the input voltage as shown in Fig. 4 (input current waveforms at $k_S > 1$).

D. Boundary Angle Between Operation Modes

The DCM1-DCM2 boundary angle is obtained directly from (13) when $D_{DCM2} = D_{max}$,

$$\theta_{D1D2} = a\sin\left(\frac{L f_{sw}(I_{ref} - I_R)}{D_{\max} V_{im}} + \frac{V_o}{V_{im}}\right) , \quad (25)$$

whereas, the DCM1-CCM2 boundary angle is obtained directly from (21) when $D_{CCM2} = D_{max}$,

$$\theta_{D1C2} = a\sin\left(\frac{V_o}{D_{\max} V_{im}}\right) . \quad (26)$$

Finally, the DCM2-CCM2 boundary angle is obtained from (19)-(21) by equating the peak inductor current from (19) with the peak-to-peak inductor-current ripple from (20),

$$\theta_{D2C2} = a\sin\left(\frac{L f_{sw} I_{RM} - V_o}{L f_{sw} I_{ref} - V_o} \cdot \frac{V_o}{V_{im}}\right) . \quad (27)$$

E. Reference Current

The reference current I_{ref} can be determined from the input-output power balance,

$$P_{in} = \frac{2}{\pi} \cdot V_{im} \cdot \left(\int_{\theta_0}^{\theta_{DD}} i_{in,DCM1}(\theta) \cdot \sin\theta \cdot d\theta + \right.$$

$$\left. + \int_{\theta_{DD}}^{\theta_{DC}} i_{in,DCM2}(\theta) \cdot \sin\theta \cdot d\theta + \int_{\theta_{DC}}^{\pi/2} i_{in,CCM2}(\theta) \cdot \sin\theta \cdot d\theta \right) = \frac{P_o}{\eta} . \quad (28)$$

It should be noted that (28) encompasses all five MS's from Table I. The boundary angles θ_{DD} and θ_{DC} in different MS's are defined in Table I.

In MS1 and MS4, reference current I_{ref} can be expressed in a closed form. Specifically, in MS1, I_{ref} is obtained after substituting (14) and the boundary angles θ_{DD} and θ_{DC} form Table I into (28) as,

$$I_{ref1} = \sqrt{\frac{\pi P_{in}}{V_{im} L f_{sw} \int_{\theta_0}^{\pi/2} \frac{(V_{im}\sin(\theta) - V_o)\cdot\sin(\theta)}{[V_{im}\sin(\theta) - V_o + I_{RM} L f_{sw}]^2} d\theta}} . \quad (29)$$

whereas, in MS4, I_{ref} is obtained by substituting (11) and (22)-(24) as well as the boundary angles θ_{DD} and θ_{DC} form Table I into (28) as

$$I_{ref4} = \frac{P_{in} - \frac{2}{\pi} V_{im} \cdot \left(\int_{\theta_0}^{\theta_{D1C2}} i_{in,DCM1}(\theta)\sin\theta d\theta + \int_{\theta_{D1C2}}^{\pi/2} i_{in,DCM1}(\theta)\sin\theta d\theta \right)}{\left(1 - \frac{2}{\pi}\theta_{D1C2}\right) \cdot V_o} \quad (30)$$

In MS2, MS3, and MS5, boundary angles θ_{D1D2} and θ_{D2C2}, respectively defined in (25) and (27), are functions of I_{ref} and, therefore, I_{ref} cannot be expressed in a closed form. To determine I_{ref}, first, the corresponding boundary angles should be determined from the input-output power balance (28) after expressing I_{ref} as a function of the corresponding boundary angle.

Specifically, in MS2, by rewriting (27), I_{ref} can be expressed as

$$I_{ref}(\theta_{D2C2}) = I_{RM} \frac{V_o}{V_{im}\sin\theta_{D2C2}} + \frac{V_o}{L f_{sw}}\left(1 - \frac{V_o}{V_{im}\sin\theta_{D2C2}}\right) . \quad (31)$$

After substituting $I_{ref}(\theta_{D2C2})$ from (31) into (14) and (22)-(24), boundary angle θ_{D2C2} can be determined from the input-output power balance (28) by using an iterative procedure. Once boundary angle θ_{D2C2} is determined, I_{ref2} directly follows from (31).

In MS3, I_{ref} can be expressed by rewriting (25) as

$$I_{ref}(\theta_{D1D2}) = I_R + \frac{D_{\max}}{L f_{sw}}\left(V_{im}\sin\theta_{D1D2} - V_o\right) , \quad (32)$$

and after substituting $I_{ref}(\theta_{D1D2})$ from (30) into (14), boundary angle θ_{D1D2} can be determined from the input-output power balance (28) by using an iterative procedure, similarly to that in MS2. Once boundary angle θ_{D1D2} is determined, I_{ref3} directly follows from (32).

In MS5, both boundary angles θ_{D1D2} and θ_{D2C2} exist as shown in Table I. Therefore, both expressions (31) and (32) for I_{ref} hold. In addition,

$$I_{ref}(\theta_{D1D2}) = I_{ref}(\theta_{C2D2}) . \quad (33)$$

One of the boundary angles should be expressed as a function of the other boundary angle. For example,

$$\theta_{D1D2} = a\sin\left(\frac{L f_{sw}}{V_{im} D_{\max}} \cdot \left(I_{ref}(\theta_{D2C2}) - I_R\right) + \frac{V_o}{V_{im}}\right) . \quad (34)$$

Then, after substituting $I_{ref}(\theta_{D2C2})$ from (31) into (14) and (22)-(24), and using (34), boundary angle θ_{D2C2} can be determined iteratively from the input-output power balance (28). Again, once boundary angle θ_{D2C2} is determined, I_{ref5} directly follows from (31).

The whole procedure described above can be easily implemented by using any standard mathematical software (e.g., Mathcad). In a particular design, I_{ref} is calculated for all five MS's. The actual value of I_{ref}, i.e., the actual MS, is the one that satisfies the MS conditions which are also defined in Table I.

In fact, the MS conditions in Table I include three tests of the reference current. The first test is I_{ref} compared to I_R. If $I_{ref} < I_R$, the duty cycle is always smaller than $D_{\max}$, as follows from Fig. 3(b), and the first operation mode of the buck inductor is DCM2. In the opposite case, when $I_{ref} \geq I_R$, the duty cycle can reach $D_{\max}$, as shown in Fig. 3(b), and the first operation mode of the buck inductor is DCM1.

The second test is I_{ref} compared to $I_{refCCM2}$ defined as

$$I_{refCCM2} = \left(I_{RM} + \frac{V_{im} - V_o}{L f_{sw}}\right) \cdot \frac{V_o}{V_{im}} , \quad (35)$$

which tests if the buck inductor can reach operation in CCM2 at the peak of the input voltage, i.e. at phase angle $\theta = \pi/2$. Specifically, for operation in CCM2 at $\theta = \pi/2$, the peak of the inductor current in (19) should be greater than the peak-to-peak ripple of the inductor current in (20), i.e.,

$$I_{ref} - I_{RM} \cdot \frac{V_o}{V_{im}} > \frac{V_o}{V_{im}} \cdot \frac{V_{im} - V_o}{L f_{sw}} . \quad (36)$$

It should be noted above that (35) directly follows from (36).

The third test is I_{ref} compared to $I_{refD1C2}$ defined as

$$I_{refD1C2} = I_R + \frac{V_o}{L f_{sw}} \cdot \left(1 - D_{\max}\right) , \quad (37)$$

which is used in mode sequences MS4 and MS5 to test if the buck inductor can reach operation in CCM2 directly from DCM1, i.e., at maximum duty cycle $D_{\max}$. Specifically, for operation in CCM at $D_{\max}$, the peak of the inductor current in (19) should be greater than the peak-to-peak ripple of the inductor current in (20), i.e.,

$$I_{ref} - I_{RM} \cdot D_{\max} > (1 - D_{\max}) \cdot \frac{V_o}{L f_{sw}} \quad . \tag{38}$$

Again, it should be noted that (37) directly follows from (38).

F. Input Current Harmonics and Power Factor

The input current contains only odd harmonics whose rms value can be determined by using the Fourier analysis,

$$I_{in,k} = \frac{2\sqrt{2}}{\pi} \cdot \left(\int_{\theta_0}^{\theta_{DD}} i_{in,DCM1}(\theta) \cdot \sin(k\theta) \cdot d(\theta) + \int_{\theta_{DD}}^{\theta_{DC}} i_{in,DCM2}(\theta) \cdot \sin(k\theta) \cdot d(\theta) + \int_{\theta_{DC}}^{\pi/2} i_{in,CCM2}(\theta) \cdot \sin(k\theta) \cdot d(\theta) \right) . \tag{39}$$

The rms value of the input current is defined as

$$I_{in,rms} = \sqrt{\frac{2}{\pi} \cdot \left(\int_{\theta_0}^{\theta_{DD}} i_{in,DCM1}^2(\theta) d(\theta) + \int_{\theta_{DD}}^{\theta_{DC}} i_{in,DCM2}^2(\theta) d(\theta) + \int_{\theta_{DC}}^{\pi/2} i_{in,CCM2}^2(\theta) d(\theta) \right)} . \tag{40}$$

Finally, the input power factor and the total harmonic distortion are obtained as

$$PF = \frac{P_{in}}{V_{in,rms} \cdot I_{in,rms}} \quad , \tag{41}$$

and

$$THD = \sqrt{\frac{\cos^2(\phi)}{PF^2} - 1} \text{ , where } \phi = 0 . \tag{42}$$

III. Design of Clamped-Current Buck PFC

The mathematical model derived in the previous section is used for the design of a 94-W, 80-V output, universal-input ($V_{in,rms}$ = 90-264 V) CCB PFC converter, which is used as the front-end in a 90-W notebook adapter. The efficiency of the second stage of the adapter is around 95.8%.

It follows from (11), (14), and (22)-(24), where the components of the input current are defined, that the design variables are the buck inductance L, the switching frequency f_{sw}, the maximum duty cycle D_{max}, and the height of the ramp current I_{RM}.

A. Buck Inductor Design

For the buck inductor design, it can be assumed in the first iteration that the input current is proportional to the input-output voltage difference, as shown in Fig. 1,

$$i_{in}(\theta) = I_{im} \cdot \left(\sin(\theta) - \sin(\theta_0)\right), \ \theta_0 < \theta < \pi - \theta_0 \tag{43}$$

where, I_{im} is determined from the input power as

$$I_{im} = \frac{\pi}{2} \cdot \frac{P_{in}}{V_{im} \cdot \int_{\theta_0}^{\pi/2} \left(\sin^2(\theta) - \sin(\theta) \cdot \sin(\theta_0)\right) \cdot d\theta} \quad . \tag{44}$$

The peak value of the input current is obtained from (43) as

$$I_{ipk} = I_{im} \cdot \left(1 - \sin(\theta_0)\right) \quad . \tag{45}$$

The buck inductance should be designed so that at minimum rms input voltage and full load, the buck inductor can reach operation in CCM around the peak of the input voltage. Specifically, at the peak of the input voltage, in CCM operation, the average inductor current and the peak-to-peak ripple of the inductor current are determined as

$$i_{L,ave} = \langle i_L(t) \rangle_{T_{sw}} = \frac{I_{ipk}}{D_{CCM,pk}} \quad , \tag{46}$$

and

$$\Delta i_L = \frac{V_o}{L f_{sw}} \cdot \left(1 - D_{CCM,pk}\right) \quad , \tag{47}$$

respectively, where

$$D_{CCM,pk} = \frac{V_o}{V_{im}} \quad , \tag{48}$$

and they should satisfy the following condition

$$i_{L,ave} > \frac{\Delta i_L}{2} \quad . \tag{49}$$

By substituting (46)-(48) into (49), it is obtained that

$$L > \frac{1}{2 f_{sw} I_{ipk}} \cdot \left(\frac{V_o}{V_{im}}\right)^2 \cdot \left(V_{im} - V_o\right) .. \tag{50}$$

If the switching frequency is selected as f_{sw} = 100 kHz, it follows from (50) that the buck inductance should be greater than 44 μH. In this design, the buck inductance is selected as L = 95 μH, which results in $\Delta i_L \approx i_{L,ave}$ at the peak of the minimum rms input voltage and full load.

B. Ramp Current Design

In this design, the maximum duty cycle is selected as $D_{\max}$ = 0.8, which is a typical value in conventional PWM controllers.

After selecting the values of the switching frequency, buck inductance, and maximum duty cycle, the key design parameter is the normalized slope of the ramp current, k_S, defined in (3)-(6).

The normalized slope of the ramp current k_S should be designed so that the input current at nominal low-line (100 V_{rms}) and high-line (230 V_{rms}) can meet the standards for the line current harmonics such as the IEC-61000-3-2 Class D standard.

Input current waveforms obtained in Mathcad at nominal low-line (100 V_{rms}) and full load for different values of k_S are presented in Fig. 4. Corresponding values of PF and THD are given in Table II. The mode sequences for different values of k_S are also included in Table II. It Is shown in Table II that with

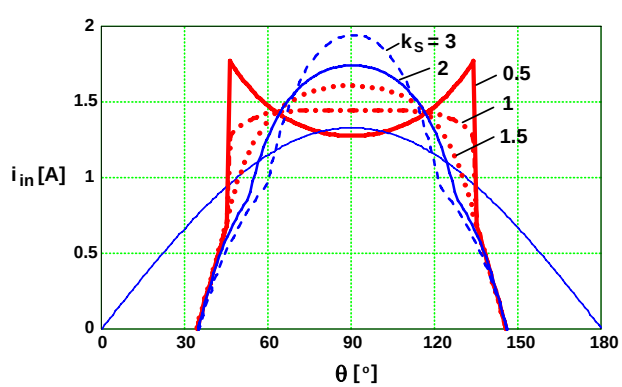

Fig. 4 Input current waveforms versus k_S at V_{in} = 100 V_{rms}

TABLE II
MS, PF AND THD VS k_S AT V_{in} = 100 V_{rms}

k_S	MS	PF	THD [%]	Meet IEC61000-3-2
0.5	4	0.915	44.1	No
1	4	0.932	38.9	Yes
1.5	4	0.931	39.2	Yes
2	5	0.922	42.0	Yes
3	2	0.904	47.3	Yes
5	2	0.880	54.0	Yes
10	2	0.843	63.8	No

TABLE III
MS, PF AND THD VS k_S AT V_{in} = 230 V_{rms}

k_S	MS	PF	THD [%]	Meet IEC61000-3-2
0.5	3	0.860	59.3	No
1	1	0.933	38.6	No
1.5	1	0.961	28.8	Yes
2	1	0.975	22.8	Yes
3	1	0.987	16.3	Yes
5	1	0.993	11.9	Yes
10	1	0.993	11.9	Yes

increasing k_S, the mode sequence changes as MS4 → MS5 → MS2. It can be concluded from Fig. 4 and Table II that k_S has an optimum value between 1 and 1.5, which results in a minimum THD and maximum PF. The minimum and maximum values of k_S to meet the Japanese standard corresponding to the IEC61000-3-2 Class D standard are $k_{S\min}$ = 0.95 and $k_{S\max}$ = 9.5, respectively.

Input current waveforms obtained in Mathcad at nominal high-line (230 V_{rms}) and full load for different values of k_S are presented in Fig. 5, whereas, the corresponding values of PF and THD are given in Table III. The mode sequences for different values of k_S are also included in Table III. It is shown in Table III that with increasing k_S, the mode sequence changes from MS3 to MS1. In fact, except for small values of k_S below 1, the mode sequence is MS1, where the converter operates only in mode DCM2. It should be noted that it was shown in Subsection II.B that in DCM2, in order the input current to be proportional to the difference of the input-output voltage, k_S should be as large as possible, which follows from (16). It can be concluded from Fig. 5 and Table III that with an increasing k_S, the quality of the input current improves, PF increases, and THD decreases. The minimum value of k_S to meet the IEC61000-3-2 Class D standard is $k_{S\min}$ = 1.25. By observing the input current waveforms in Fig. 4, it can be concluded that a practical value of k_S should be between 3 and 5.

It follows from the analysis above that with a single value of k_S in the whole input voltage range, an optimum design cannot be achieved. The value of k_S should be variable to increase with increasing input voltage. In this paper, k_S = 1.5 is selected at nominal low-line and k_S = 5 is selected at nominal high line.

The implementation of the external current ramp can be achieved in two ways. First, the slope of the external current ramp can be directly controlled by the input voltage as defined above. Second, the slope of the external current ramp can be indirectly controlled by the input voltage when the current ramp is implemented as an exponential ramp. In fact, at nominal high-line, the duty cycle is reduced and, therefore, at the end of the duty cycle the slope of the exponential ramp is close to its maximum value. At nominal low line, the duty cycle is increased and, consequently, at the end of the duty cycle the slope of the exponential ramp is decreased. In this paper, the external current ramp is implemented as an exponential ramp.

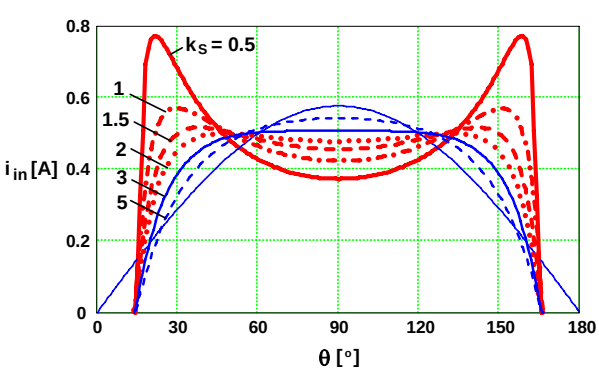

Fig. 5 Input current waveforms versus k_S at V_{in} = 230 V_{rms}

IV. EXPERIMENTAL RESULTS

Measured input voltage and input current waveforms at nominal low-line and nominal high-line, at full load, obtained on a 94-W, 80-V output, universal-input ($V_{in,rms}$ = 90-264 V) CCB PFC converter, which is used as the front-end in a 90-W notebook adapter, are shown in Figs. 6 and 7, respectively. The measured waveforms are in a good agreement with the corresponding calculated waveforms, except for the additional phase shift in the measured input-current waveforms, which is due to the effect of the input filter.

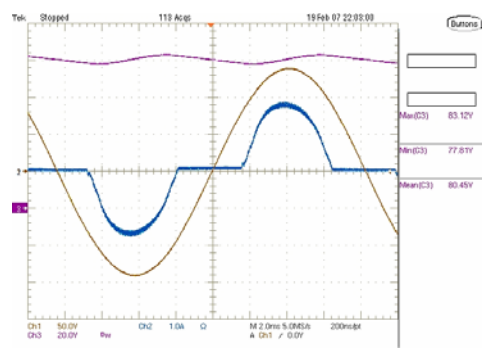
Fig. 6 Measured input voltage, input current, and bulk-capacitor voltage waveforms at nominal low-line (V_{in} = 100 V_{rms})

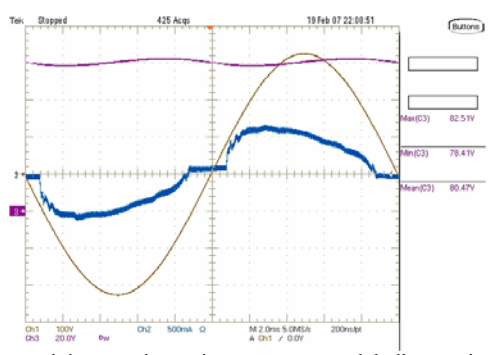
Fig. 7 Measured input voltage, input current, and bulk-capacitor voltage waveforms at nominal high-line (V_{in} = 230 V_{rms})

TABLE IV
MEASURED EFFICIENCY AND PF OF BUCK PFC FRONT END OF 90-W ADAPTER

V_{in} [V]	PF	η [%]
90	0.8910	95.74
100	0.9085	95.85
115	0.9356	96.02
132	0.9630	96.20
180	0.9627	96.35
200	0.9540	96.25
230	0.9278	96.22
264	0.8846	96.00

Efficiency and PF measurements at full load in the whole input-voltage range are presented in Table IV. It can be seen in Table IV that the buck PFC maintains a high efficiency of around 96% across the entire input-voltage range.

V. BUCK PFC VS BOOST PFC

Generally, the efficiency of the buck PFC at nominal low-line voltage compared to the efficiency of a conventional DCM/CCM boundary boost PFC is greater by approximately 1%. This improvement is brought about by several major factors.

First, the boost PFC requires a larger common-mode EMI filter because of the elevated common-mode current, which is the result of the larger voltage swing of the boost switch and the increased parasitic capacitance between the primary and secondary windings of the high-voltage transformer in the dc-dc output stage.

Second, the boost PFC has higher bridge-diode losses because of its average input current is greater than the average input current of the buck PFC. This is nicely illustrated with a simple example in Fig. 8. The rms value of the sinusoidal input current of a typical boost PFC in Fig. 8(a) is equal to the rms value of the rectangular input current of a simplified buck PFC in Fig. 8(b), i.e. $I_{i1,rms} = I_{i2,rms} = I_m/\sqrt{2}$. The corresponding average currents are $I_{i1,ave} = (2/\pi)I_{im} = 0.637I_{im}$ and $I_{i2,ave} = I_{im}/2 = 0.5I_{im}$, respectively. It follows that $I_{i1,ave} = 1.27I_{i2,ave}$, i.e., the average input current of a boost PFC is greater than the average input current of a buck PFC by more than 25%.

Finally, the boost PFC has a larger PFC inductance because the minimum switching frequency of a DCM/CCM boundary boost PFC is typically lower than a constant switching frequency of a buck PFC. This results in an increased number of turns and, consequently in an increased conduction loss.

V. SUMMARY

A detailed design-oriented analysis of the clamped-current buck (CCB) PFC converter is presented. The design is focused on the slope of the external current ramp. It is shown that with a constant slope of the external current ramp in the whole input voltage range, an optimum design cannot be achieved. The slope of the external ramp should be variable and increase with increasing input voltage. The whole design procedure can be easily implemented by using any standard mathematical software (e.g. Mathcad).

Experimental results obtained on a 94-W, 80-V output, universal-input ($V_{in,rms}$ = 90-264 V) CCB PFC converter, which is used as the front-end in a 90-W notebook adapter are given. It is shown that the buck PFC maintains a high efficiency of around 96% across the entire input-voltage range.

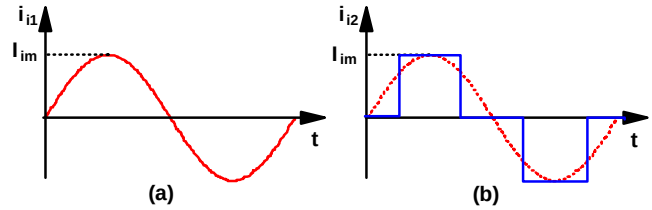

Fig. 8 Simple example to illustrate that the buck PFC has lower average input current than the boost PFC

The major factors that contribute to the improved efficiency of the buck PFC versus the boost PFC at low line voltages are briefly explained.

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