Light-Load Efficiency Optimization Method

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***Abstract* — A method of maintaining high power-conversion efficiency across the entire load range and its circuit implementations are described. The proposed method substantially increases the conversion efficiency at light loads by minimizing switching and driving losses of semiconductor switches, as well as core losses of magnetic components. These losses are minimized by periodically turning off and on the power converter and by controlling the converter so that when the converter is on it operates at the power level that exhibits the maximum efficiency. The performance of the proposed method was evaluated on a 500-W, 400-V/12-V dc/dc converter and a 1-kW ac/dc boost PFC front end.**

I. Introduction

Ever since the start of the miniaturization era spurred on by the microelectronics revolution of the late fifties and early sixties, power conversion equipment has been facing continuously increasing power density and efficiency challenges. Until recently, efficiency increases of power conversion circuits were primarily driven by increased power density requirements since power density increases are only possible if appropriate incremental improvements in full-load efficiency are achieved so that the thermal performance is not adversely affected. As a result, maximization of the full-load efficiency has been a design focus all along. However, in the late nineties, the explosive growth of consumer electronics and data-processing equipment has prompted the introduction of various, mostly voluntary, requirements aimed at minimizing the idle-mode, i.e., light-load, power consumption. Meeting these increasingly-stringent requirements, most notably those defined in the U.S. Energy Star, Japan Top Runner, and ECoC (European Code of Conduct) specifications [1], still poses a major design challenge.

Today, the power supply industry is at the beginning of another major focus shift that puts efficiency improvements across the entire load range in the forefront of customers' performance requirements. This focus on efficiency has been prompted by economic reasons and environmental concerns caused by the continuous, aggressive growth of the Internet infrastructure and a relatively low energy efficiency of its power delivery system. In fact, the environmental concerns have already prompted introduction of programs and initiatives aimed at reducing the energy waste in power supplies for data-processing applications by challenging power-supply manufacturers to improve efficiencies of their products. For example, the 80Plus incentive program [2] and Climate Saver Computing Initiative (CSCI) [3], the two programs that are already in place, require that power supplies for computer applications maintain efficiency above 80% in the entire load range from full load down to 20% of full load. These efficiency targets have recently been incorporated into the latest U.S. Environmental Protection Agency's (EPA) Energy Star specifications [4]. However, many of the largest computer, telecom, and network-equipment manufacturers already require light-load efficiencies that exceed the latest Energy Star specifications and also are extending these requirements down to 10% and, even 5% loads.

Generally, the efficiency of power conversion circuits at heavy loads is determined by the conduction losses of semiconductor and magnetic components, whereas their light-load efficiency is primarily determined by switching losses of semiconductors, core losses of magnetics, and drive losses of semiconductor switches [5],[6]. Because switching and drive losses of semiconductor switches and core losses of magnetic components are almost independent of the load, a typical efficiency curve as a function of the load power shows a steep fall off as the load decreases below 10-20% of the full load, as illustrated in Fig. 1. Furthermore, as the rated output power of the converter increases, larger semiconductor devices (or more devices in parallel) and larger magnetic cores are needed, which leads to increased switching and core

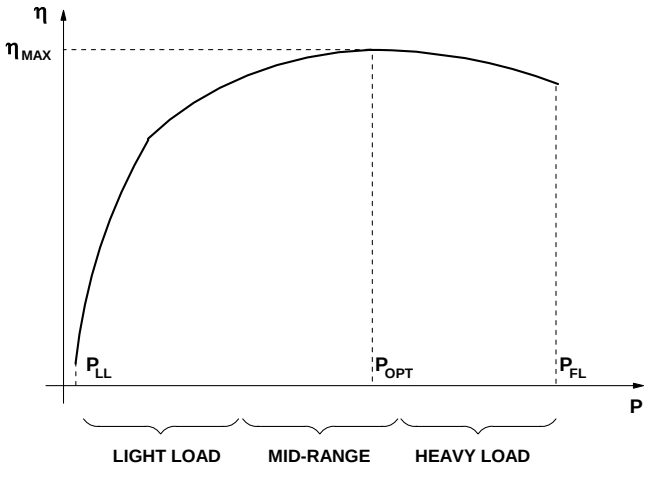

Fig. 1. Typical efficiency profile of power converter with respect to delivered power.

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losses and an even steeper fall-off of efficiency at light loads.

To make the power supply exhibit a flatter efficiency curve that meets customer's expectations, power management techniques such as variable switching frequency control, bulk-voltage reduction, phase-shedding, and "burst"-mode operation have been introduced [7]-[10]. Although the described techniques have been shown to improve the partial-load efficiency, they suffer from some major drawbacks that limit their area of application. For example, a major problem of reducing the switching frequency at light loads is an increased current ripple caused by the increased volt-second product in the core of the output filter inductor. This increase in the ripple current has an adverse effect on the efficiency because it increases the conduction loss. A major concern with bulk-voltage reduction and stage-shedding techniques is the dynamic performance. Specifically, their ability to restore full-power capability without output disturbance or other performance deterioration when the load suddenly changes from light load to full load. Finally, "burst"-mode operation is limited to very low power levels primarily due to acoustic noise.

In this paper, a method of maintaining high power-conversion efficiency across the entire load range and its circuit implementations are described. Specifically, the proposed method substantially increases the conversion efficiency at light load by minimizing switching and driving losses of semiconductor switches, as well as core losses of magnetic components. These losses are minimized by periodically turning off and on the power converter with a duty cycle set so that when the converter is on it operates at the power level that exhibits the maximum efficiency. The required output power during the periods that the converter is turned off is supplied from an energy-storage device. The operation and light-load efficiency performance of the proposed method was verified on a 500-W, 400-V/12-V dc/dc converter and a 1-kW ac/dc boost PFC front end.

II. METHOD DESCRIPTION

The proposed method of light-load efficiency optimization is based on a simple observation that the minimization of power loss requires that the power converter is either always operated at the load power with the maximum efficiency or be completely turned off. Namely, by restricting the operation of a converter to only these two operating points the best possible efficiency can be achieved because when the converter is turned off no loss is incurred, whereas when the converter is turned on it operates with the maximum efficiency.

A conceptual block diagram of the proposed light-load efficiency optimization method is shown in Fig. 2. The temporary energy storage and power conditioning block in Fig. 2 serves to maintain a continuous supply of load power during the periods the power converter is turned off. At power levels that the power converter is continuously on, this temporary energy storage and power conditioning block is idle since the entire required load power is supplied by the power converter.

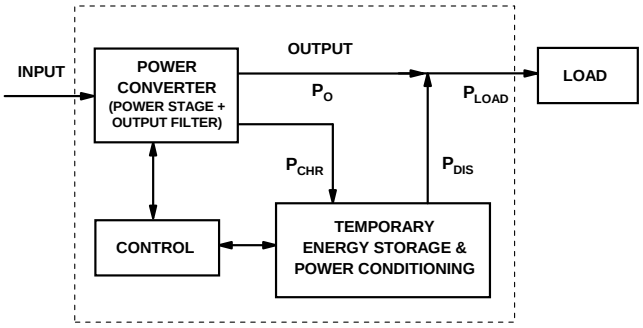

Fig. 2. Conceptual block diagram of proposed light-load efficiency optimization method.

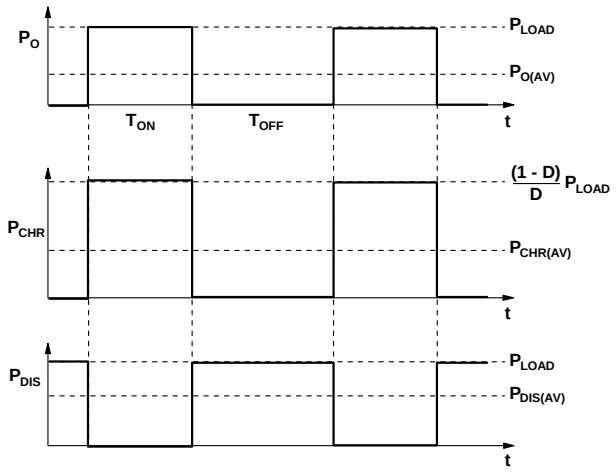

Fig. 3. Timing diagram of output power P_O, charging power P_{CHR}, and discharging power P_{DIS}.

As illustrated in the timing diagrams in Fig. 3, during time periods T_{ON} when the power converter is on, the power converter simultaneously supplies load power P_{LOAD} and charge power P_{CHR} to the energy-storage device. During time periods T_{OFF} when the power converter is turned off, the load power is entirely supported by the discharging of the energy-storage device, i.e., $P_{DIS}=P_{LOAD}$. According to Fig. 3, average power $P_{O(AV)}$ delivered by the power converter to the load is

$$P_{O(AV)} = D \cdot P_{LOAD} \tag{1}$$

and average power $P_{DIS(AV)}$ delivered by the energy-storage device to the load is

$$P_{DIS(AV)} = (1-D) \cdot P_{LOAD}, \tag{2}$$

where $D=T_{ON}/(T_{ON}+T_{OFF})$.

Since average charging power $P_{CHR(AV)}$ must be equal to average discharging power $P_{DIS(AV)}$, the instantaneous charging power P_{CHR} during T_{ON} is

$$P_{CHR} = \frac{(1-D)}{D} \cdot P_{LOAD}, \quad (3)$$

as illustrated in Fig. 3.

Therefore, total instantaneous power P delivered by the power converter during T_{ON} is

$$P = P_O + P_{CHR} = P_{LOAD} + \frac{1-D}{D} P_{LOAD} = \frac{P_{LOAD}}{D}. \quad (4)$$

From Eq. (4), to improve the light-load efficiency of a power converter with the efficiency dependence on delivered power as in Fig. 1, optimal duty cycle D_{OPT} should be selected from Eq. (4) as

$$D_{OPT} = \frac{P_{LOAD}}{P_{OPT}}, \quad (5)$$

i.e., the power converter during T_{ON} should deliver power P_{OPT} that corresponds to the maximum efficiency.

Theoretically, the power level that this method of efficiency optimization can be applied is limited to the power level below P_{OPT}. Typically, the boundary load power between continuous and pulse modes of operation of the power converter P_{BOUND} (<P_{OPT}) is set at light load levels where efficiency fall-off becomes pronounced, as illustrated in Fig. 4.

In the derivation of D_{OPT} in Eq. (5), it was assumed that no loss is incurred during the charging and discharging of the energy-storage device. If charging and discharging losses are included by assuming that the energy-storage device charging and discharging efficiencies are η_{CHR} and η_{DIS}, respectively, optimal duty cycle D^*_{OPT} is

$$D^*_{OPT} = \frac{1}{\frac{P_{OPT}}{P_{LOAD}} \cdot \eta_{ES} + (1-\eta_{ES})}, \quad (6)$$

where $\eta_{ES} = \eta_{CHR}\,\eta_{DIS}$ is the efficiency of the energy storage and power conditioning block.

With charging and discharging losses included, the conversion efficiency at power levels below P_{BOUND} is given by

$$\eta = \eta_{MAX} \frac{\eta_{ES}}{1 - D^*_{OPT}(1-\eta_{ES})}. \quad (7)$$

In the ideal case when no energy is lost during the charging and discharging of the energy-storage device, i.e., when $\eta_{ES} = 1$ is assumed, light-load efficiency is equal to η_{MAX} all the way to a minimum load, as illustrated in Fig. 4. However, in practice, because $\eta_{ES} < 1$ the light-load efficiency is lower than η_{MAX} and exhibits a fall-off as power is reduced, as shown in Fig. 4. Generally, to achieve light-load efficiency improvement, it is necessary to make a favorable trade-off between the power saved by periodically turning-off the power converter and the power lost in the charging and discharging process of the energy-storage device.

It should be noted that while optimal duty cycle D^*_{OPT} is precisely defined by Eq. (6), once power level P_{OPT} and load power P_{LOAD}<P_{BOUND} is known, the frequency at which the power converter is turned on and off can be set anywhere in a relatively wide frequency range. Generally, the upper frequency limit is related to the large signal dynamic response time of the converter, whereas the lower frequency limit is determined by the size and required energy-storage capacity of the energy-storage device because at lower frequencies more stored energy is required to support the load power during prolonged off times. For power levels of several hundred Watts, typical minimum frequency for electrolytic-capacitor-type energy storage is in the several-Hertz to several-hundred-Hertz range, whereas sub-hertz frequencies can be achieved by employing batteries, super capacitors, flywheels, and similar storage devices. Finally, it should be noted that it is desirable to keep the switching frequency outside the audio range to avoid acoustic noise associated with the switching of a relatively large power.

Many variations of the proposed efficiency optimization method are possible. Generally, these variations are related to realization of the charging and discharging paths of the energy-storage device. For example, the charging energy can be supplied from the input of the power converter instead of

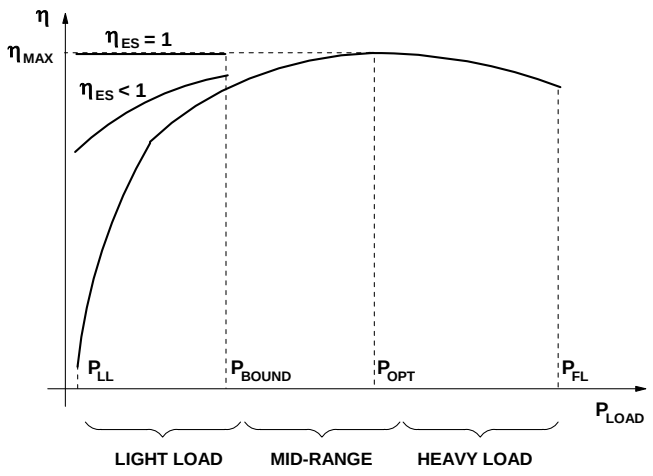

Fig. 4. General illustration of light-load efficiency improvements obtained by proposed efficiency optimization method.

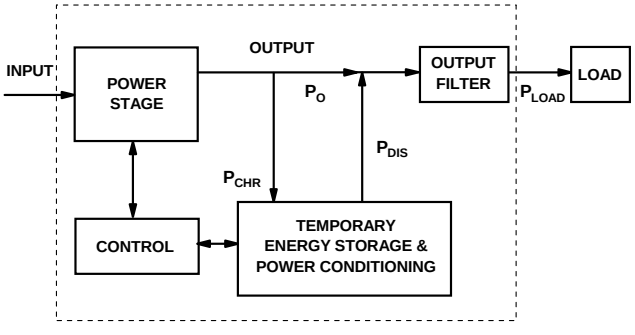

Fig. 5. Conceptual block diagram of another implementation of proposed light-load efficiency optimization method.

from the output. Also, the proposed method can be implemented with a common charging and discharging path. Furthermore, the charging and discharging paths do not need to be coupled directly to input and/or output, but can be coupled to any suitable point in the power conversion path. As an example, Fig. 5 shows the conceptual implementation of this method where the charging and discharging paths are coupled before the output filter of the power converter. If properly designed, these implementations can reduce, or even completely eliminate, transients caused by periodic turning on and off of the power converter. Namely, since in these implementations the output-filter inductor current is continuously flowing, i.e., it is either supplied from the converter or from the discharging energy-storage device, it does not exhibit significant transients if the circuit is designed so that the current supplied by the converter when it is on and the current supplied by the energy-storage and conditioning circuit during the off-time are reasonably matched.

III. CIRCUIT IMPLEMENTATIONS

Figures 6(a)-(e) show several dc/dc converter implementations of the proposed efficiency optimization method. The power stage box in the figures can be any single or interleaved power conversion topology such as, for example, half-bridge, full-bridge, single- or two-switch forward, or LLC topology. Figures 6(a)-(c) show the implementations of the concept according to Fig. 5 where the discharging path of the energy-storage devices, i.e., capacitor C_{ST}, is through the output filter of the power converter. Figures 6(d) and (e) show examples of the proposed method implementation according to Fig. 2 where the charging and discharging paths of energy-storage cap C_{ST} are coupled directly to the output.

In the implementation in Fig. 6(a), energy-storage capacitor C_{ST} is inductively charged by a dc output of the power stage when the power stage is turned on. During the time periods the power stage is turned off, the load power is provided by discharging C_{ST} through a buck converter that shares the output filter with the power stage. Generally, for isolated power converter stages, inductance L_l in the charging path can be the leakage inductance of the transformer. The implementation of L_l as the leakage inductance of the transformer is especially effective in topologies where the leakage inductance of the transformer is intentionally increased such as in the full-bridge converter with phase-shift control or LLC resonant converter.

The implementation in Fig. 6(b) employs a boost converter to charge energy-storage capacitor C_{ST} and a buck converter in the discharging path. Because of the boost converter, energy storage in capacitor C_{ST} can be done at a higher voltage, which makes it possible to reduce the size of the energy-storage capacitor. A variation of this implementation that employs a common charging and discharging path is shown in Fig. 6(c). In this implementation a bi-directional buck-boost converter is used to provide controlled charging and discharging of the energy-storage capacitor.

Figure 6(d) shows an implementation where the charging and discharging paths of capacitor C_{ST} are coupled to the output of the power converter. In fact, this implementation is a variation of the implementation in Fig. 6(c) since the boost converter is used for charging and the buck for discharging.

Finally, Fig. 6(e) shows the simplest implementation of the proposed method. In this implementation energy-storage

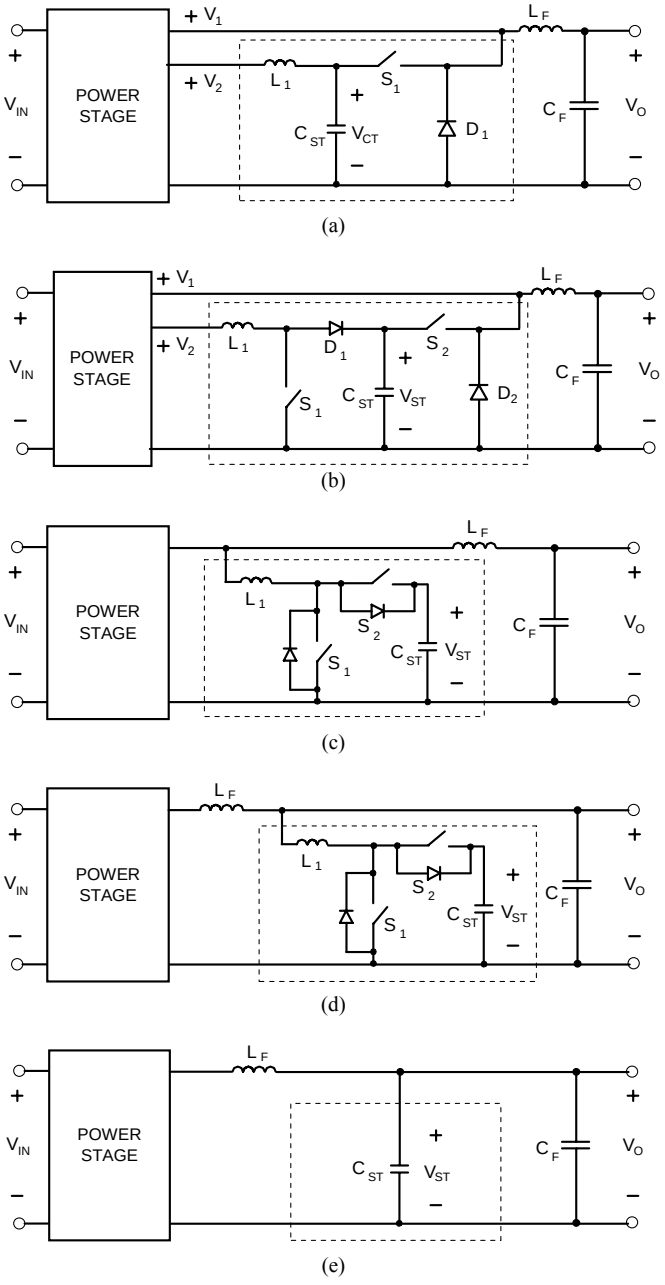

Fig. 6. Examples of circuit implementations of proposed light-load efficiency optimization method.

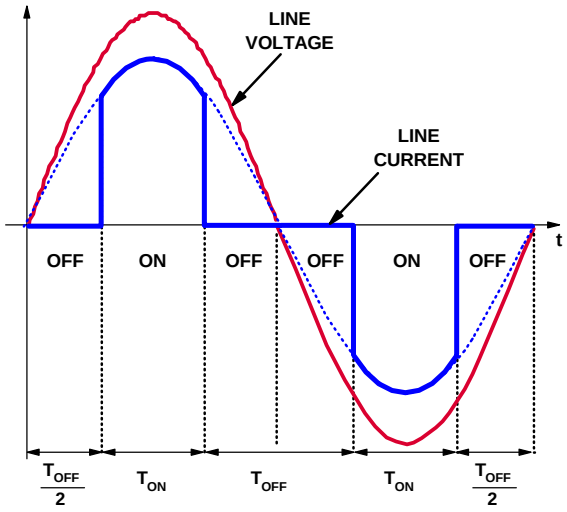

Fig. 7. Control implementation of proposed method in PFC applications.

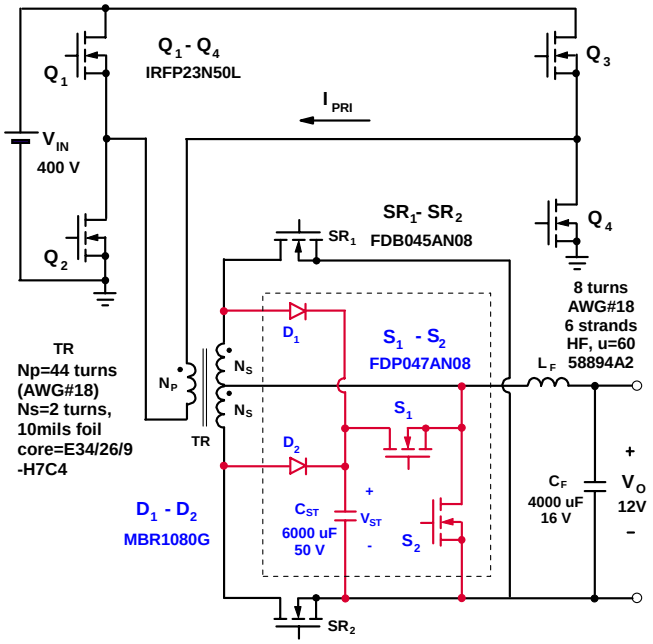

Fig. 8. Circuit diagram of 500-W, ZVS full-bridge dc-dc converter laboratory prototype. Added temporary energy storage and power conditioning circuit are shown inside dashed-line rectangular.

capacitor C_{ST} is directly connected in parallel with output-filter capacitor C_F. In fact, in applications where the output filter capacitor needs to store significant energy such, for example, in PFC applications, additional energy-storage capacitor C_{ST} may not be needed.

When the proposed efficiency optimization method is applied to the ac/dc PFC front end, it is necessary to recognize that the line-current harmonic limit specifications need to be met down to 75 W of input power [11]. As a result, a straightforward implementation of this method where the front-end power converter is periodically turned on and off with an arbitrary frequency is only possible below the input power of 75 W.

Because of the required compliance with the line-current harmonic limit specifications at input power levels above 75 W, the turning off and on of the converter can only be done within half-line cycles, as illustrated in Fig. 7. In the control approach shown in Fig. 7, the PFC converter is kept off near the zero-crossings of the line current and is enabled for power processing around the peaks of the line current. Since this conduction-angle control generates line-current distortions that increase as turn-off time T_{OFF} increases, the maximum duration of off time T_{OFF} is limited by the required harmonic-limit compliance of the line current. This maximum off-time can be easily figured out for a given power level either by using simulation or calculation software.

IV. Experimental Results

The performance of the proposed technique was separately evaluated on a 500-W dc/dc converter and a 1-kW ac/dc PFC boost front-end rectifier. The circuit diagram of the 500-W dc/dc converter prototype is shown in Fig. 8. The circuit in Fig. 8 implements the proposed method of light-load efficiency optimization according to Fig. 6(a) where V_1=V_2 and L_l is the leakage inductance of transformer TR, i.e., it combines a ZVS full-bridge converter with phase-shift control with a synchronous-buck converter discharging circuit.

The 500-W dc/dc prototype was designed to operate from a 400-V dc input and deliver up to 42 A at a 12-V output. The full-bridge converter operating at 110-kHz switching frequency was implemented with an IRFP23N50L MOSFET from IR for each bridge switch Q_1 - Q_4, whereas a FDB045AN08 MOSFET from Fairchild was employed for each synchronous rectifier SR_1 and SR_2. Transformer TR was built using a pair of ferrite E-cores (E34/26/9-H7C4) with 44 turns of magnet wire (AWG# 18) for the primary winding and 2 turns of copper foil (10 mil, 20 mm) for each of the secondary windings. Output filter inductor L_F was built using a toroidal high flux core (58894A2, u=60) from Magnetics with 8 turns of magnet wire (6 strands, AWG #18). Four low voltage aluminum capacitors (1000 µF, 16 VDC) were used for output capacitor C_F.

The buck converter that is periodically turned on at light loads to deliver power from energy-storage capacitor C_{ST} was implemented with an FDP047AN08 MOSFET from Fairchild for both the buck switch S_1 and synchronous-rectifier switch S_2. Schottky diodes MBR1080G from On Semi were used for charging diodes D_1 and D_2. Finally, six low voltage aluminum capacitors (1000 µF, 50 VDC) were used as storage capacitor C_{ST}. It should be noted that the buck converter shares the output filter, i.e., output inductor L_F and

output capacitor C_F, with the full-bridge converter. The switching frequency of the buck converter was set to approximately 100 kHz. This frequency is close enough to the 110-kHz frequency of the full bridge to keep the output filter-inductor current virtually unchanged during transitions between the full-bridge and buck operation, which ensures smooth transitions between these two modes of operation. Since the full-bridge converter and the buck converter do not operate at the same time, a frequency synchronization of two converters was not necessary. The maximum output power of

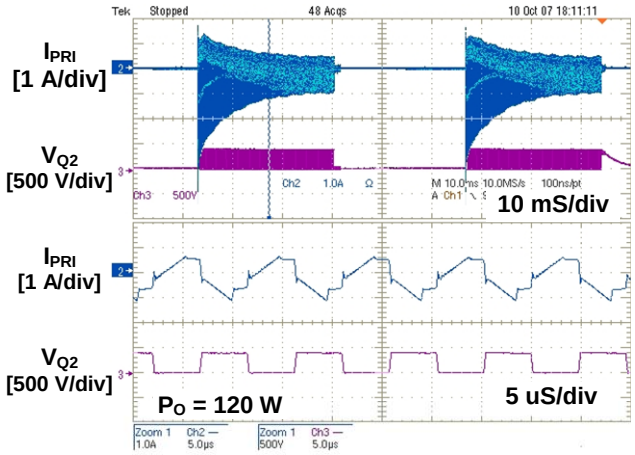

Fig. 9. Measured primary-current I_{PRI} and switch Q_2 drain-to-source voltage V_{Q2} waveforms of ZVS full-bridge converter prototype. Time scale for upper two traces is [10 mS/div]. Time scale for bottom two traces is [5 uS/div].

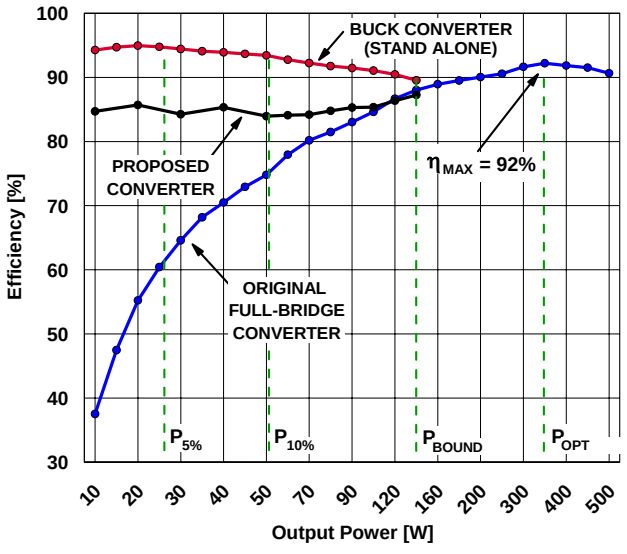

Fig. 10. Measured efficiencies of original full-bridge converter, stand-alone buck converter, and proposed converter as functions of output power.

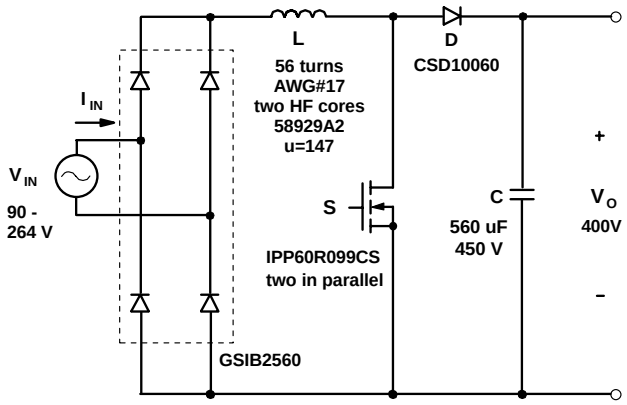

Fig. 11. Circuit diagram of experimental 1-kW PFC boost rectifier .

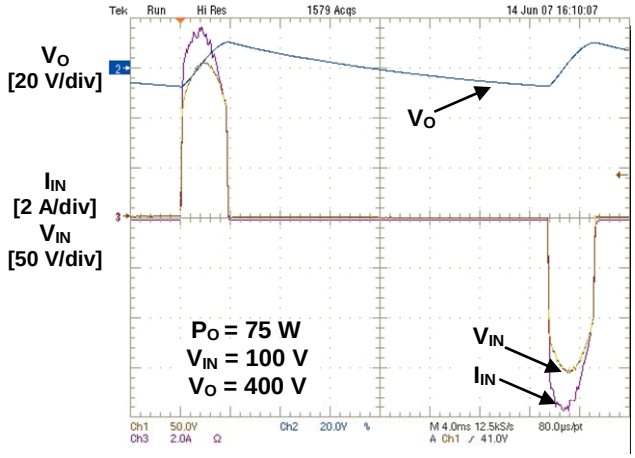

Fig. 12. Measured waveforms of experimental PFC boost rectifier. V_{IN} is line voltage, I_{IN} is line current, and V_O output voltage.

the buck converter was designed to be approximately 140 W which is enough to deliver up to 25% of the total output power.

Figure 9 shows the measured waveforms of the prototype circuit at approximately 120 W, whereas Fig. 10 shows measured efficiency of the proposed converter along with the measured efficiencies of the full-bridge converter and the buck converter. As can be seen from Fig. 10, the proposed converter exhibits higher efficiencies below approximately 100 W. The improvement of the efficiency is more pronounced as the load becomes lighter. For example, at 50 W, which is 10% of the full load, the efficiency improvement is around 8%, whereas at 25 W, i.e., at 5% of the full load, the improvement is approximately 24%.

Figure 11 shows the circuit diagram of the PFC boost rectifier prototype build to evaluate the performance of the proposed method in ac/dc applications. The 1-kW, 110-kHz PFC boost rectifier prototype was designed to operate from a universal ac-line input (90 V_{RMS}-264 V_{RMS}) and deliver up to

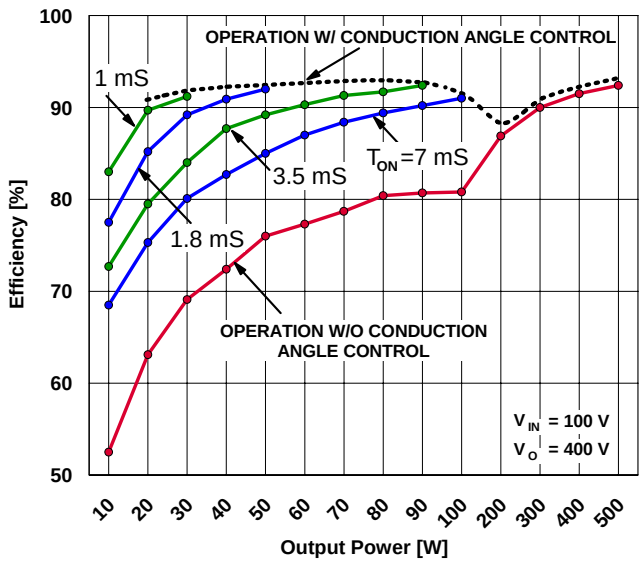

Fig. 13. Measured efficiency of PFC rectifier as functions of output power for different conduction times T_{ON}. Dashed line represents efficiency that can be obtained by changing (decreasing) T_{ON} as output power decreases.

2.5 A from a 400-V output. The prototype employs two IPP60R099CS MOSFETs (V_{DSS} = 600 V, R_{DS} = 0.099 Ω) in parallel for boost switch S and a CSD10060 SiC diode (V_{RRM} = 600 V, I_{FAVM} = 10 A) for boost diode D. In this implementation, the 560-μF bulk capacitor C_B that is sized based on the hold-up time requirement also serves as energy-storage capacitor C_{ST}.

Figure 12 shows the oscillograms of the input current, input voltage, and output voltage waveforms of the PFC rectifier prototype with the conduction-angle control. To simplify the experiment, i.e., to avoid implementing a conduction-angle control itself, the conduction angle of the input voltage waveform was actually controlled by a programmable ac source (6000LX, California Instrument). Because in the PFC boost rectifier the input current waveform follows the input voltage waveform, the desired operation was achieved without any modifications of the PFC control circuit.

The measured efficiencies of the PFC rectifier with and without conduction-angle control are shown in Fig. 13. As can be seen from Fig. 13, conduction-angle control was applied at power levels below 100 W, i.e., below 10% of the full power. With the conduction-angle control, the prototype PFC rectifier exhibits higher light-load efficiencies. In fact, at the same power level, the efficiency gains are larger as conduction time T_{ON} decreases from 7 mS to 1 ms. However, as the conduction time reduces the maximum power that can be delivered to the output also reduces. The maximum light-load efficiency gains can be obtained by implementing active conduction-time control, i.e., by reducing conduction time T_{ON} as the output power reduces. With this kind of control, the light-load efficiency is represented by the dashed line in Fig. 13.

V. Summary

A method of improving the light-load efficiency of power converters is proposed. In the proposed method, the light-load efficiency improvement is achieved by periodically turning off the power converter to reduce switching-related losses. During the time periods the converter is turned off, the required load power is supplied from an energy-storage device. During the time periods when the converter is delivering power to the load and charging the energy-storage device, it is controlled so that it operates at the power level that corresponds to the maximum conversion efficiency.

The proposed efficiency optimization method is applicable to any power conversion dc/dc or ac/dc system or topology. Generally, the energy storage medium can be any component/device that can store energy such as, for example, capacitors, batteries, flywheels, etc.

The performance of the proposed method is verified on two experimental prototypes; a 500-W, ZVS full-bridge dc/dc converter and a 1-kW boost PFC converter. Both prototypes showed remarkable light-load efficiency improvements with the proposed approach all the way down to 5% load.

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