

# Methods of Reducing Audible Noise Caused by Magnetic Components in Variable-Frequency-Controlled Switch-Mode Converters

Laszlo Huber and Milan M. Jovanović  
Delta Products Corporation  
P.O. Box 12173  
5101 Davis Drive  
RTP, NC 27709, USA

**Abstract - Methods and a circuit implementation of audible noise reduction in switch-mode converters with variable switching frequency are presented. The audible noise caused by magnetic components is reduced by controlling the switching frequency so that it stays above the audible range as the load decreases. This is accomplished by decreasing the peak value of the main switch current pulses in discrete steps until the peak value of the main switch current pulses is decreased to a level which is sufficiently low not to produce unacceptable audible noise. At very light loads and at no load, the audible noise reduction circuit can be disabled in order to meet various worldwide standards that limit the maximum input power. The performance of the proposed circuit was experimentally verified in a 90-W single-stage PFC flyback adapter.**

## I. INTRODUCTION

Prompted by environmental concerns and economic reasons caused by the continuous and aggressive growth of the Internet infrastructure and a relatively low energy efficiency of its power delivery system, the power supply industry today faces a very challenging task of making power conversion products that exhibit a high efficiency in the entire load range. These tough efficiency targets have already been defined in a number of voluntary and mandatory specifications issued by a number of worldwide agencies, most notable by the U.S. Energy Star [1] and its European Community's counterpart [2].

Generally, the optimization of efficiency across the entire load range reduces to finding the right balance between switching and conduction losses because the full load efficiency is predominantly determined by conduction losses of semiconductor and magnetic components, whereas light load efficiencies are for the most part determined by switching losses of semiconductors and core losses of magnetic components [3]-[5]. This iterative optimization process involves selection of the most suitable power supply architectures and power conversion topologies, as well as the optimal selection of semiconductor components, design optimization of magnetics, and implementation of power management techniques. While in the past the major research effort was on finding new architectures and topologies with improved performance [6]-[10], the major efficiency gains were enabled by the advances in semiconductor devices and by better understanding of magnetics design [11]-[13]. In fact, except for minor refinements, the architectures and topologies employed in today's high-performance power supplies are essentially the same as those used in the past.

As the silicon-based devices approach their theoretical performance limit, their ability to improve the performance of the next generation of power supplies is diminished. The emerging SiC and GaN technologies will certainly bring about future significant incremental efficiency improvements [14]-[16]. Nevertheless, the major improvements of the power supply efficiency in the future are expected to be achieved by power management. While power management, which is being enabled by the recent developments of digital infrastructure for power-supply applications, is shown indispensable in flattening efficiency curve across the entire load range, it is even more essential in maximizing the efficiency at very-light and no load conditions.

Generally, to meet the efficiency requirements at light loads and at no load, the switching frequency needs to be reduced. This can be achieved by employing cycle skipping, also called burst-mode of operation, or by employing a variable switching frequency control, i.e., by continuously decreasing the switching frequency as the load decreases. The burst mode of operation is typically employed in power supplies with a constant switching frequency control. However, reducing the switching frequency or operating in the burst mode may cause audible noise if the switching frequency or the burst frequency falls in the audible range (20 Hz - 20 kHz).

The main sources of the audible noise in switched-mode power supplies are cooling fans and magnetic components such as transformers, input filter inductors, and power-factor-correction (PFC) chokes. In today's power supplies that employ fan speed control, the fan noise caused by the air turbulence generated by the fins is dominant at heavy and medium loads, i.e., at loads above approximately 20-40% of the full load. As a result, the noise generated by magnetic components is not a concern at these loads. However, at lighter loads, with a reduced fan speed, the noise generated by magnetic components may become a design issue.

Magnetic-component's audible noise can be separated in two parts depending on different excitation mechanisms as described in [17]. The first and most dominant part of the noise is caused by magnetization of the core, generally assumed to arise from magnetostriction, where the core dimensions change when subjected to an applied magnetic field. The second part of the magnetic component noise is caused by electromagnetic forces created by the magnetic field of the currents in the component's windings. Generally, magnetostriction can cause a mechanical

interaction between the core and the windings that leads to vibrations. These mechanical vibrations are closely related to the magnetic flux swing.

While audible noise caused by mechanical vibrations of magnetic components is a problem in any power supply, it is especially undesirable in external ac-dc power supplies (adapters/chargers) for portable electronics because these adapters do not have a cooling fan and are usually placed close to the user. In the absence of any audible noise agency specifications, many companies have defined their own internal specifications. According to the majority of these internal specifications, if the audible noise of an adapter is above 25 dB(A)/20.0  $\mu$ Pa measured at a distance of 5 cm, appropriate measures should be taken to reduce the audible noise.

Methods for reducing the magnetic-components-related audible noise in switch-mode converters can be divided into mechanical and electrical methods. The mechanical approaches are based on techniques that prevent or damp vibrations by mechanical means such as varnishing, gluing, and potting. While these methods are successful in some applications, generally, they are undesirable since they involve extra manufacturing steps and, therefore, increase the cost. Electrical methods of controlling audible noise are preferred since they are more successful and cost effective.

The literature on audible-noise reduction methods in switch-mode converters caused by magnetic components is very scarce [18]-[21]. More importantly, the available literature does not offer any experimental evaluation of the effectiveness of the proposed audible-noise-reduction techniques.

Generally, in [18]-[20], methods for reducing the audible noise in burst-mode of operation are proposed. Specifically, in [18] and [20], shaping the envelope of the switch current pulses is proposed to reduce the audible noise in burst-mode of operation. In [19], the audible noise problem is solved by presetting the switching frequency values above the audible range and by decreasing the switch current limit as the load decreases until the lowest current limit has been reached, which is low enough such that the flux density in the core of the transformer does not produce unacceptable audible noise. Moreover, in [19], constant switching frequency power converters with on/off feedback control and with a relatively complex cycle skipping algorithm are considered.

In power supplies with variable switching frequency, the audible noise can be completely eliminated by preventing the switching frequency to drop below the upper threshold of the audible range. This can be achieved directly by limiting the maximum switching period or by limiting the maximum off time; or indirectly, by monitoring the switching frequency to detect when has the switching frequency dropped close to the upper threshold of the audible range and, then, instantly increasing the switching frequency, as described in [21]. It should be noted that [21] is aimed at the problem of reducing the audible noise in power converters with variable switching frequency, where the switching frequency decreases as the load increases and where the switching frequency can drop below the upper threshold of the audible range when exceptional operating circumstances exist

such as over power, short circuit, start up, or turning off the converter.

In this paper, methods and a circuit implementation for reducing audible noise caused by magnetic components in switch-mode converters with variable switching frequency and with continuous feedback control, where the switching frequency decreases as the load decreases, are described. Generally, the described audible-noise-reduction solutions are intended primarily for switch-mode converters that do not have cooling fans and where the only noise sources are magnetic components. Specifically, the most appropriate application of the presented work is for external ac/dc converters for portable electronics equipment such as notebook adapters/chargers that can be placed in close proximity to the user.

## II. AUDIBLE NOISE REDUCTION METHODS

The block diagram of a switch-mode power supply with variable switching frequency and with continuous feedback control is shown in Fig. 1. The variable-switching-frequency control is achieved by the voltage-controlled oscillator (VCO), controlled by the feedback voltage  $V_{FB}$  at the output of the error amplifier (EA). According to the control method in Fig. 1, as the load decreases, the feedback voltage decreases, and consequently, the switching frequency decreases, as illustrated in Fig. 2. For simplicity, in Fig. 2, a linear relationship between the switching frequency and load current is assumed, which is a good approximation for a converter operating in discontinuous conduction mode (DCM). A duty cycle is initiated by the VCO and is terminated when the current-sense (CS) voltage  $V_{CS}$  reaches reference voltage level  $V_{CS,Ref}$  as shown in Fig. 1. Principle of operation is illustrated in Fig. 3 on the example of the flyback converter. If the peak value of the switch current pulses  $I_{Peak}$  is constant, the switching frequency linearly changes with the load current so that when the switching frequency decreases twice, the average switch current also decreases twice, which means that the load current decreases twice.

In Fig. 2, the switching frequency enters the audible range at load current  $I_{Load1}$ . The minimum switching frequency,  $f_{swMin}$ , is obtained at no load, which is typically above the lower threshold

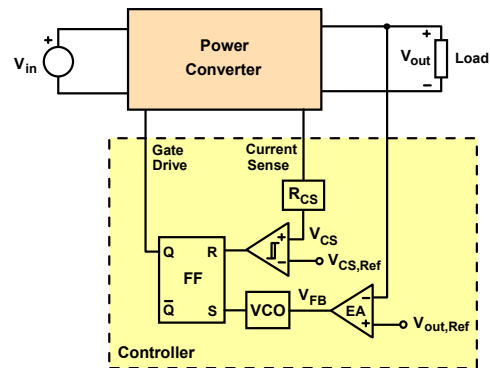


Fig. 1 Block diagram of a switch-mode power supply with variable switching frequency and with continuous feedback control.

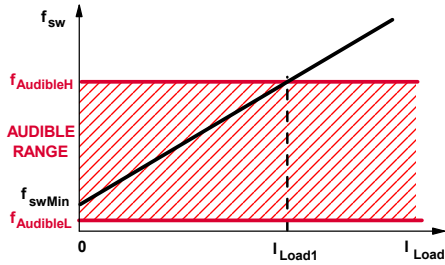


Fig. 2 Relationship between the switching frequency and load current of a converter operating in discontinuous conduction mode.

of the audible range,  $f_{AudibleL}$ . If the peak value of the switch current pulses is not sufficiently low, the corresponding magnetic flux swing in the core of the transformer will produce unacceptable audible noise.

In this paper, the audible noise is reduced by controlling the switching frequency so that it stays above the audible range as the load decreases by decreasing the peak value of the main switch current pulses in discrete steps, as illustrated in Fig. 4, until the peak value of the main switch current pulses is decreased to a level which is sufficiently low so that the corresponding magnetic flux swing in the core of the transformer does not produce unacceptable audible noise.

To detect when the switching frequency has dropped close to the upper threshold of the audible range, the switching frequency has to be monitored. The switching frequency can be directly monitored or indirectly monitored by monitoring either the feedback voltage or the load current.

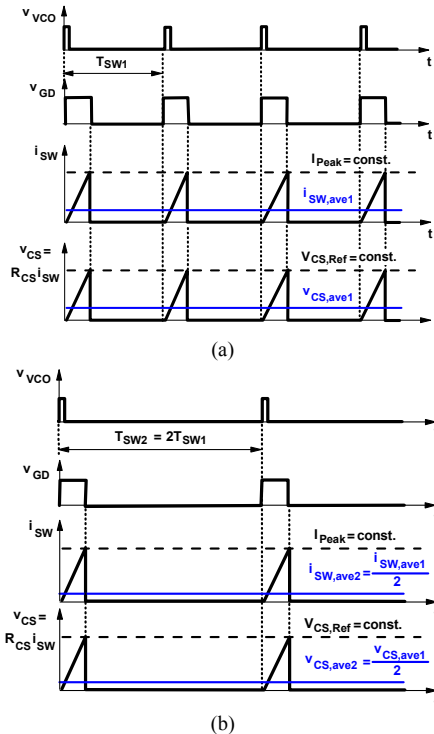


Fig. 3 Principle of operation corresponding to Fig. 2 on the example of the flyback converter.

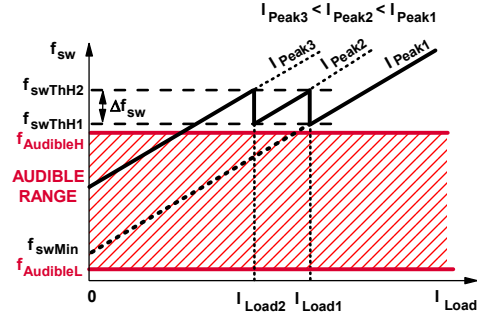


Fig. 4 Basic method of audible noise reduction.

After detecting that the switching frequency has dropped close to the upper threshold of the audible range, the peak value of the main switch current pulses is decreased in a discrete step. Consequently, the switching frequency increases ( $\Delta f_{sw}$  in Fig. 4) in order to provide the same power to the load. Three methods can be used to decrease the peak value of the main switch current pulses. First, by decreasing the reference value of the current-sense voltage  $V_{CS,Ref}$ ; second, by adding a dc bias to the current-sense voltage  $V_{CS}$ ; and, third, by increasing the value of the current-sense resistor  $R_{CS}$ .

To prevent the oscillation of the switching frequency when the peak value of the main switch current pulses changes between two consecutive discrete values, a hysteresis can be added to the control of the switching frequency, as illustrated in Fig. 5.

It should be noted that the switching frequency control by employing three discrete peak values of the main switch current pulses as shown in Figs. 4 and 5 is an illustrative example and that the number of the discrete peak values of the main switch current pulses can be selected from a minimum value of two to a finite large number.

At very light loads and at no load, an increased switching frequency will result in increased switching losses. Consequently, meeting standard requirements that limit the maximum input power at very light loads and at no load can be an issue. If necessary, at very light loads and at no load, the audible noise reduction circuit can be disabled and the switching frequency decreased to its original value as illustrated in Fig. 6 at  $I_{Load} = I_{Load3}$ . In fact, in Fig. 6, the switching frequency is

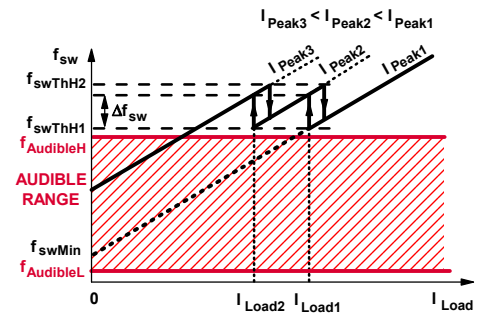


Fig. 5 Audible noise reduction method with hysteresis.

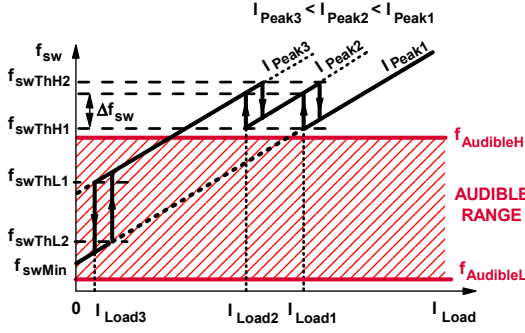


Fig. 6 Audible noise reduction method, where ANR is disabled at very light loads and no load.

decreased by increasing the peak value of the main switch current pulses to the original peak value  $I_{Peak1}$ . It should be noted that at very light loads and at no load, the original switching frequency is, typically, close to the lower threshold of the audible range and, therefore, a larger peak value of the main switch current pulses and, consequently, a larger magnetic flux swing in the core of the transformer will not produce unacceptable audible noise, which is the result of the nonlinear sensitivity of the human ear to the audible frequencies [23].

A simplified block diagram of the audible noise reduction (ANR) circuit is shown in Fig. 7, where the switching frequency is directly monitored by monitoring the switch driving signal. As mentioned above, the switching frequency can also be indirectly monitored by monitoring the feedback voltage or the load current. In that case, the input of the ANR block is connected to output of the error amplifier (EA) or to the output of the load current sensing circuit, respectively. It is also shown in Fig. 7 that the output of the ANR circuit, i.e., the output of the peak-current programming block, can modify either current-sense reference voltage  $V_{CS,Ref}$ , current-sense voltage  $V_{CS}$ , or current-sense resistor  $R_{CS}$ .

### III. IMPLEMENTATION

The implementation of the audible noise reduction circuit is based on the method shown in Fig. 6. The ANR circuit is implemented by directly monitoring the switching frequency and by adding a dc bias to the current-sense voltage in order to decrease the peak value of the main switch current pulses. For simplicity, only two discrete peak values of the main switch current pulses are employed to control the switching frequency. The simplified circuit diagram of the ANR circuit is presented in Fig. 8. Key waveforms that illustrate the operation of the circuit are presented in Figs. 9 and 10.

The control of the switching frequency at the upper threshold of the audible range around load current  $I_{Load} = I_{Load1}$  shown in Fig. 6 is implemented in Block H in Fig. 8; whereas, the control of the switching frequency inside the audible range at very light loads around  $I_{Load} = I_{Load3}$  shown in Fig. 6 is implemented in Block L in Fig. 8.

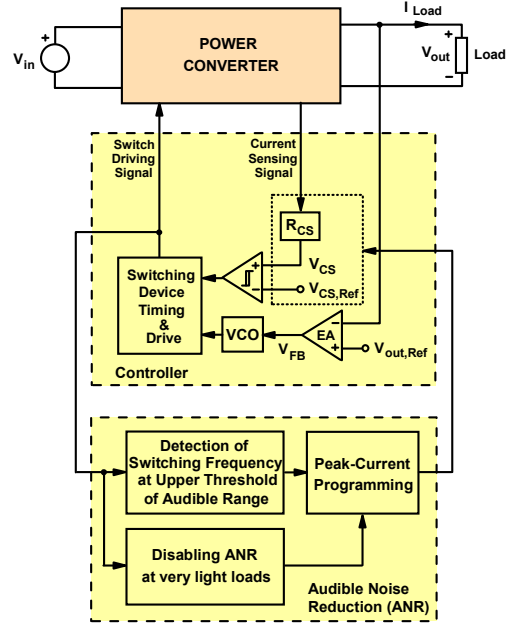


Fig. 7 Simplified block diagram of the ANR circuit.

The switching frequency, i.e., the switching period is monitored by converting time to voltage. The ramp voltages,  $v_{RampH}$  and  $v_{RampL}$ , are generated by charging the respective ramp capacitors  $C_H$  and  $C_L$  with a constant current,  $I_H$  and  $I_L$ , respectively. At the beginning of a switching period, the ramp capacitors are discharged by briefly turning on the respective ramp switches  $SW_{H1}$  and  $SW_{L1}$  in parallel with the ramp capacitors. The control signal for the ramp switches is obtained by differentiating the gate drive signal of the main switch.

The detection of the switching frequency at the upper threshold of the audible range is achieved by comparing ramp voltage  $v_{RampH}$  to reference voltage  $V_{CompH,Ref}$  at the inputs of comparator  $COMP_H$ , whereas, the detection of the switching frequency inside the audible range at very light loads is achieved by comparing ramp voltage  $v_{RampL}$  to the reference voltage  $V_{CompL,Ref}$  at the inputs of comparator  $COMP_L$ . To control the switching frequency according to the method shown in Fig. 6, each reference voltage has two discrete levels. It should be noted that the ramp voltages are clamped by Zener diodes  $ZD_H$  and  $ZD_L$  to a level slightly higher than the voltage of the respective reference voltage sources  $V_{RefH}$  and  $V_{RefL}$ .

The output voltage of a comparator becomes HIGH if the switching frequency is equal or smaller than the relevant reference frequency, i.e., if the switching period is equal or greater than the relevant reference period. The information about the switching frequency obtained in the current switching cycle is used in the next switching cycle to control the peak value of the main switch current pulses. In fact, the voltage level at the output of a comparator is stored in the corresponding D flip-flop at the positive edge of the gate drive signal. It should be noted that the output voltage of a comparator can easily meet the setup-time requirement of a positive-edge triggered D flip-flop due to the

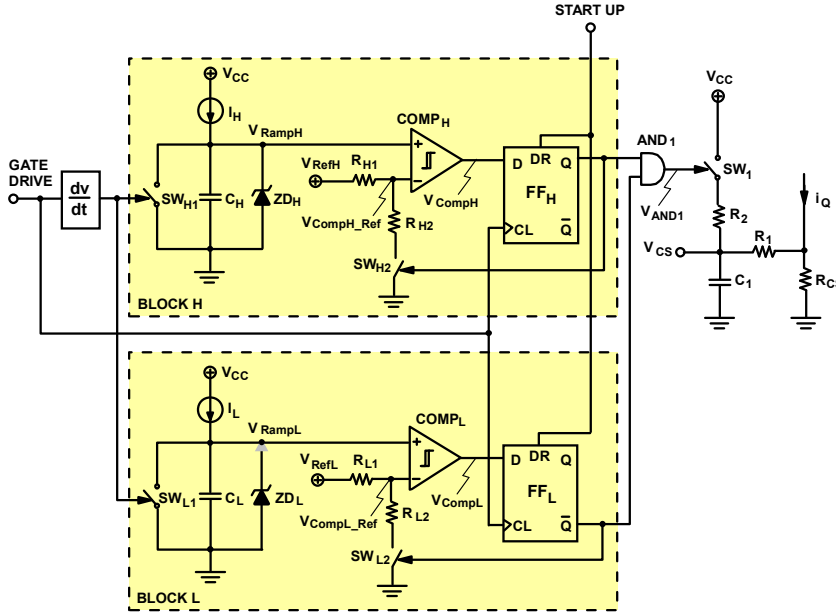


Fig. 8 Simplified circuit diagram of the ANR circuit.

delay time of the comparator. Initially, all D flip-flops are reset through the direct reset (DR) pins.

The peak current programming block is implemented by adding a dc bias to the current-sense voltage in order to decrease the peak value of the main switch current pulses. When the output of AND gate  $AND_1$  is LOW, switch  $SW_1$  is open and the current-sense voltage  $v_{CS}$  is equal to the voltage across the current-sense resistor. It should be noted in Fig. 8 that resistor  $R_1$  and capacitor  $C_1$  make a conventional low-pass filter at the current-sense input of the control circuit. When the output of AND gate  $AND_1$  is HIGH, switch  $SW_1$  is closed and the current-sense voltage  $v_{CS}$  is determined as

$$v_{CS} = \frac{R_2}{R_1 + R_2} \cdot R_{CS} i_Q + \frac{R_1}{R_1 + R_2} \cdot V_{CC} \quad (1)$$

where,  $i_Q$  is the main switch current. Eq. (1) can be rewritten as

$$v_{CS} = \frac{R_2}{R_1 + R_2} \cdot \left( R_{CS} i_Q + \frac{R_1}{R_2} \cdot V_{CC} \right) \approx R_{CS} i_Q + \frac{R_1}{R_2} \cdot V_{CC} \quad (2)$$

because  $R_2 \gg R_1$ . The second term in (2) represents the dc bias of the current-sense voltage.

The waveforms in Fig. 9 illustrate the operation of the circuit in Fig. 8 at  $I_{Load} = I_{Load1}$  shown in Fig. 6, where the switching frequency decreases close to the upper threshold of the audible range and, consequently, the peak value of the main switch current pulses decreases from  $I_{Peak1}$  to  $I_{Peak2}$ , resulting in an increased switching frequency,  $\Delta f_{sw}$  in Fig. 6.

Before instant  $t = T_0$ , the output voltage of both D flip-flops,  $FF_H$  and  $FF_L$ , is LOW and, therefore, the output of AND gate  $AND_1$  is LOW and  $I_{Peak} = I_{Peak1}$ . The reference voltage of comparator  $COMP_H$  has HIGH value,  $V_{CompH\_Ref} = V_{RefH}$ , whereas, the reference voltage of comparator  $COMP_L$  has LOW value,  $V_{CompL\_Ref} = V_{RefL} \cdot R_{L2} / (R_{L1} + R_{L2})$ . During switching cycle  $[T_0, T_1]$ ,

the switching frequency decreases below threshold frequency  $f_{swThH1}$ , i.e., the switching period increases above threshold period  $T_{swThH1}$ , and ramp voltage  $v_{RampH}$  crosses the reference voltage level of comparator  $COMP_H$ . Consequently, the output voltage of comparator  $COMP_H$  and D input of D flip-flop  $FF_H$  become HIGH. At the beginning of the next switching cycle,  $[T_1, T_2]$ , at the positive edge of the gate drive signal, the data at D input of D flip-flops, resulting in  $Q_{FFH} = 1$  and  $Q_{FFL} = 0$ . Consequently, the output of AND gate  $AND_1$  becomes HIGH and the peak value of the main switch current pulses decreases from  $I_{Peak1}$  to  $I_{Peak2}$ . It should be noted in Fig 9 that the gate drive pulse width in switching cycle  $[T_0, T_1]$  is larger than the gate drive pulse width in the succeeding switching cycles. To keep the output voltage of the power converter constant, the feedback voltage increases, resulting in an increased switching frequency.

When output  $Q$  of D flip-flop  $FF_H$  becomes HIGH, the reference voltage of comparator  $COMP_H$  decreases from HIGH to LOW level,  $V_{CompH\_Ref} = V_{RefH} \cdot R_{H2} / (R_{H1} + R_{H2})$ . As long as the switching frequency is lower than  $f_{swThH2}$ , i.e., the switching period is larger than  $T_{swThH2}$ , ramp voltage  $v_{RampH}$  will always cross the LOW reference voltage level of comparator  $COMP_H$  and, therefore, output  $Q$  of D flip-flop  $FF_H$  will stay HIGH, keeping the output of AND gate  $AND_1$  HIGH.

The waveforms in Fig. 10 illustrate the operation of the circuit in Fig. 8 at very light load  $I_{Load} = I_{Load3}$  shown in Fig. 6, where the switching frequency decreases to threshold level  $f_{swThL1}$  inside the audible range and, consequently, the peak value of the switch current pulses increases from  $I_{Peak2}$  to  $I_{Peak1}$ , resulting in a further decreased switching frequency as shown in Fig. 6.

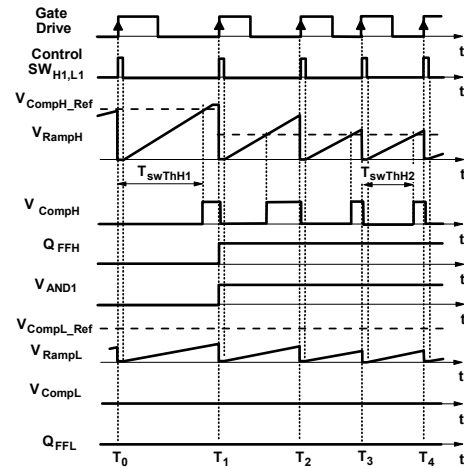


Fig. 9 Key waveforms that illustrate the operation of the circuit in Fig. 8 at load current  $I_{Load} = I_{Load1}$  shown in Fig. 6, where the switching frequency decreases close to the upper threshold of the audible range.

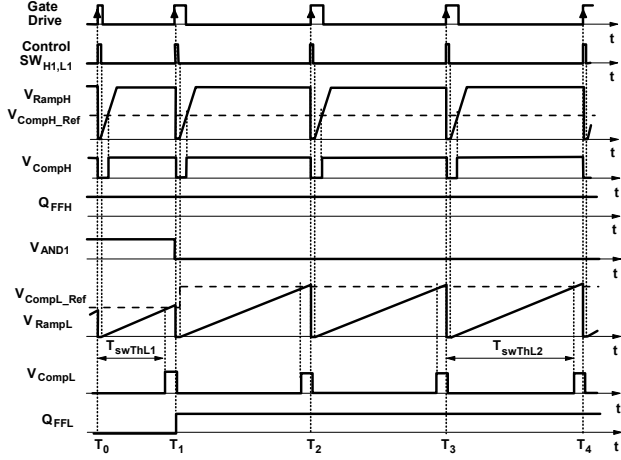


Fig. 10 Key waveforms that illustrate the operation of the circuit in Fig. 8 at very light load  $I_{Load} = I_{Load3}$  shown in Fig. 6, where the switching frequency decreases to threshold level  $f_{swThL1}$  inside the audible range.

Before instant  $t = T_0$ , the output voltage of D flip-flops  $FF_H$  and  $FF_L$  is HIGH and LOW, respectively. Therefore, the output of AND gate  $AND_1$  is HIGH and  $I_{Peak} = I_{Peak2}$ . The reference voltage of both comparators,  $V_{CompH\_Ref}$  and  $V_{CompL\_Ref}$ , is LOW. During switching cycle  $[T_0, T_1]$ , the switching frequency decreases below threshold frequency  $f_{swThL1}$ , i.e., the switching period increases above threshold period  $T_{swThL1}$ , and ramp voltage  $v_{RampL}$  crosses the reference voltage level of comparator  $COMP_L$ . Consequently, the output voltage of comparator  $COMP_L$  and D input of D flip-flop  $FF_L$  become HIGH. At the beginning of the next switching cycle,  $[T_1, T_2]$ , at the positive edge of the gate drive signal, the HIGH logic level at D input of D flip-flop  $FF_L$  is transferred to its Q output, resulting in  $Q_{FFL} = 1$ . Consequently, the output of AND gate  $AND_1$  becomes LOW and the peak value of the main switch current pulses increases from  $I_{Peak2}$  to  $I_{Peak1}$ . It should be noted in Fig 10 that the gate drive pulse width in switching cycle  $[T_0, T_1]$  is smaller than the gate drive pulse width in the succeeding switching cycles. To keep the output voltage of the power converter constant, the feedback voltage decreases, resulting in a further decreased switching frequency.

When output Q of D flip-flop  $FF_L$  becomes HIGH, the reference voltage of comparator  $COMP_L$  increases from LOW to HIGH level,  $V_{RefL}$ . As long as the switching frequency is lower than  $f_{swThL2}$ , i.e., the switching period is larger than  $T_{swThL2}$ , ramp voltage  $v_{RampL}$  will always cross the HIGH reference voltage level of comparator  $COMP_L$  and, therefore, output Q of D flip-flop  $FF_L$  will stay HIGH, keeping the output of AND gate  $AND_1$  LOW. of comparator  $COMP_L$  and, therefore, output Q of D flip-flop  $FF_L$  will stay HIGH, keeping the output of AND gate  $AND_1$  LOW.

#### IV. EXPERIMENTAL RESULTS

The audible noise reduction circuit in Fig. 8 was applied in a 90-W single-stage PFC flyback adapter with variable switching frequency [22]. The audible noise is measured as the “A” weighted sound pressure level (SPL) relative to  $20 \mu\text{Pa}$ , which is the lower threshold of the human perception of sound [23], i.e.,

$$L_{pA} [dB(A)] = 20 \log \frac{p}{20 \mu\text{Pa}} + L_{wA} [dB] \quad (3)$$

where  $p$  is the measured sound pressure in  $\mu\text{Pa}$  before weighting and  $L_{wA}$  is the transfer function of the “A” weighting network employed to compensate the characteristic of the human ear, which is differently sensitive to different frequencies. In fact, the transfer function of the “A” weighting network is approximately equal to the inverted equal loudness level contour of the human ear at a lower SPL.

The measured SPL after “A” weighting is converted into the frequency domain by using Fast-Fourier-Transform (FFT), as shown in Fig. 11.

To obtain the total SPL, a frequency analysis is performed by dividing the audible range into 1/3-octave bands [24]. This frequency analysis is called constant-percentage-bandwidth (CPB) analysis because the ratio of the upper and lower limits of each band is constant and the bandwidth is a constant percentage of the band center frequency. In each 1/3-octave band, based on the FFT spectrum, the rms value of the “A” weighted sound pressure is determined and plotted as a function of the band center frequency, as shown in Fig. 12. The total SPL is obtained as

$$L_{pA,tot} [dB(A)] = 10 \log \left( \sum_k 10^{\frac{L_{pA,k}}{10}} \right) \quad (4)$$

where  $L_{pA,k}$  is the “A” weighted SPL of the k-th 1/3-octave band.

The audible noise limits for power supplies can be specified by the 1/3-octave-band SPL limits or by the total SPL limit. The audible noise measurement methods are specified in [24]. The audible noise was measured by using the PULSE 3560C system from Bruel & Kjaer (B&K). The B&K 4190 microphone was used. The measurement was performed in a 45cm x 45cm x 65cm anechoic chamber.

Audible noise measurement results are presented in Table I. It can be seen from Table I that the worst-case audible noise at 110-Vrms line voltage is significantly reduced from 29.0 dB(A) to 20.2 dB(A). The corresponding “A”-weighted FFT-spectrum and 1/3-octave-spectrum measurements are shown in Figs. 11 and 12, respectively.

TABLE I  
WORST-CASE AUDIBLE NOISE MEASUREMENTS

Adapter	Line Voltage	
	110 Vrms	220 Vrms
Original (w/o ANR)	29.0 dB(A) at 0.595-A load	23.4 dB(A) at 0.647-A load
Modified (with ANR)	20.2 dB(A) at 0.093-A load	20.5 dB(A) at 0.019-A load

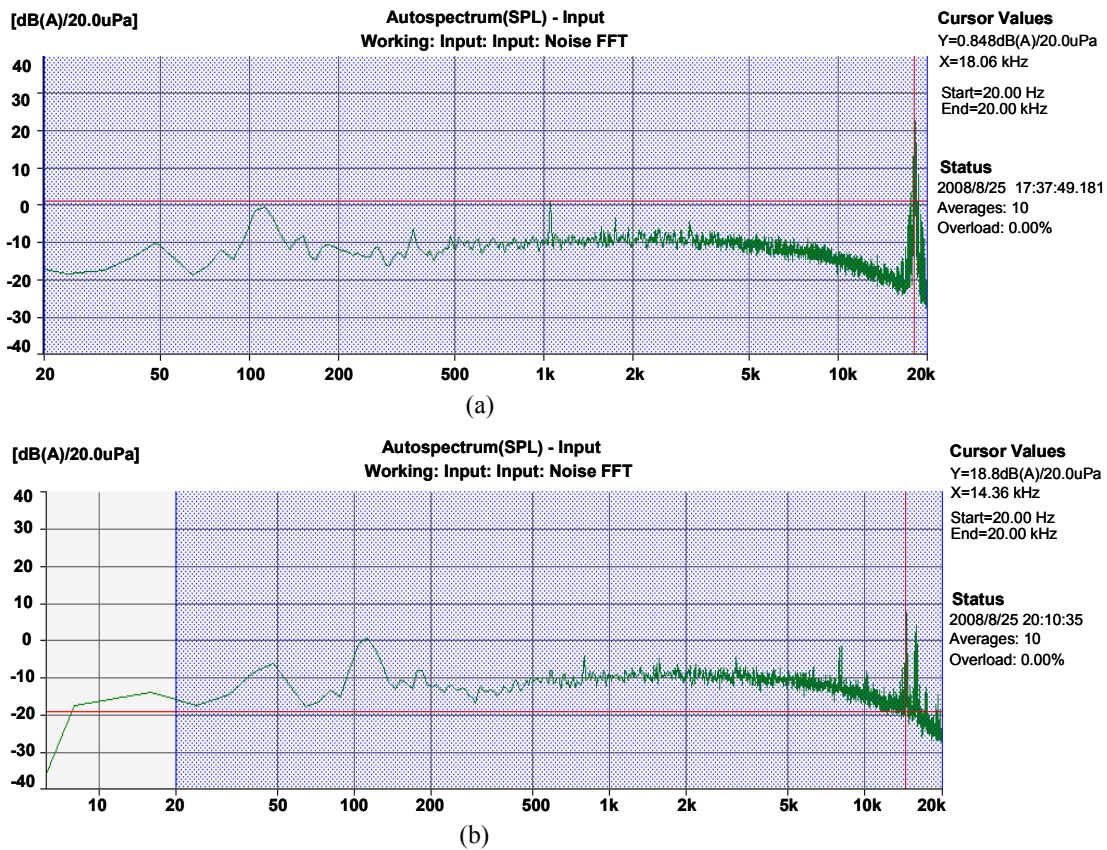


Fig. 11 Worst-case “A”-weighted FFT spectrum measurements obtained at 110-Vrms line voltage (a) without and (b) with ANR circuit.

## V. SUMMARY

Methods and a circuit implementation for reducing audible noise caused by magnetic components in switch-mode converters with variable switching frequency and with continuous feedback control, where the switching frequency decreases as the load decreases, are presented. The audible noise is reduced by controlling the switching frequency so that it stays above the audible range as the load decreases by decreasing the peak value of the main switch current pulses in discrete steps, until the peak value of the main switch current pulses is decreased to a level which is sufficiently low so that the corresponding magnetic flux swing in the core of the transformer does not produce unacceptable audible noise.

To detect when the switching frequency has dropped close to the upper threshold of the audible range, the switching frequency has to be monitored. The switching frequency can be directly monitored or indirectly monitored by monitoring either the feedback voltage or the load current.

The peak value of the main switch current pulses can be decreased by decreasing the reference value of the current-sense voltage, by adding a dc bias to the current-sense voltage, or by increasing the value of the current-sense resistor.

At very light loads and at no load, an increased switching frequency will result in increased switching losses. Consequently,

meeting standard requirements that limit the maximum input power at very light loads and at no load can be an issue. If necessary, at very light loads and at no load, the audible noise reduction circuit can be disabled and the switching frequency decreased to its original value.

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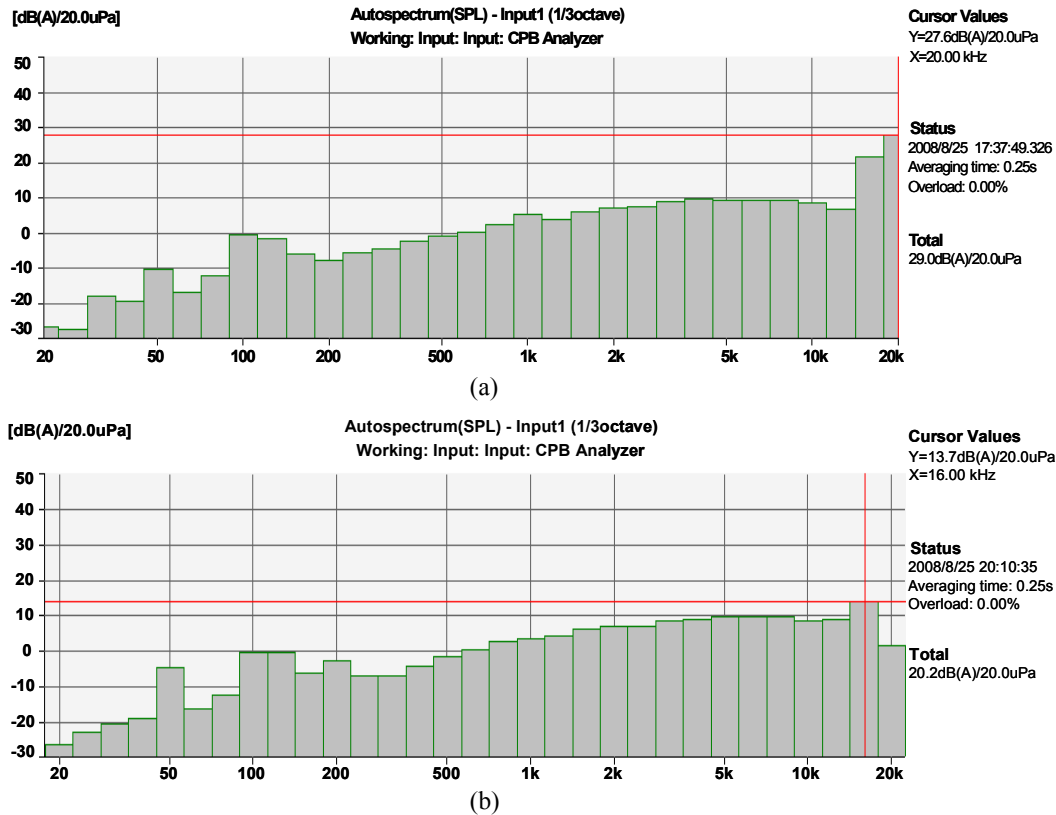


Fig. 12 Worst-case “A”-weighted 1/3-octave frequency spectrum measurements obtained at 110-Vrms line voltage (a) without and (b) with ANR circuit.

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