Startup Procedure for Three-Phase Three-Wire Isolated AC-DC Converter Implemented with Three Single-Phase Converter Modules

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Abstract – Three-phase isolated ac-dc converters can be implemented either with a direct three-phase PFC rectifier front end followed by an isolated dc-dc converter, or with three single-phase isolated ac-dc converters. Generally, the major advantage of the modular implementation with three single-phase converters is its ease of power expandability. In implementations with Y-connected single-phase modules in three-wire power systems, the major challenge is the design of a reliable control that limits the potential difference between the Y point of the single-phase modules and the neutral point of the three-phase source, $V_{Y0}$, so that the input voltage of the modules always stays within a specified range. Although a vast amount of literature on the balancing control is available, none of them addresses the startup of the modules, which is an indispensable part of control design of any practical circuit. To fill this gap, in this paper, a detailed startup procedure is described. This two-step startup procedure ensures that even with unbalanced source voltages, $V_{Y0}$ is properly controlled so that the input voltage of the modules stays within a specified limit, while PFC front-end output voltages increase monotonically and their inrush currents are below a specified level. The proposed startup procedure is illustrated with MATLAB/Simulink simulations and also experimentally verified.

I. INTRODUCTION

Three-phase isolated ac-dc converters can be implemented either with a direct three-phase PFC rectifier front end such as the Vienna rectifier or the six-switch PFC boost rectifier followed by an isolated dc-dc converter, or with three single-phase isolated ac-dc converters. Generally, the major advantage of the modular implementation with three single-phase converters is its ease of power expandability. To be able to employ single-phase modules designed for 220/277-Vrms phase-to-neutral voltage in three-phase power systems with nominal phase-to-phase voltage of 380/480 Vrms, the three single-phase modules must be connected in star (Y) configuration. The delta ($\Delta$) configuration cannot be used since it would require that single-phase modules be connected across two phases, i.e., to a voltage exceeding their rating.

In applications where the neutral point of the three-phase voltage source is available, the common point (Y point) of the single-phase converter modules is connected to the source neutral point and the three single-phase converters operate independently from each other with their input voltages equal to the respective phase-to-neutral voltages of the source. However, in applications where the source neutral point is not provided, such as, for example, in standard telecom power supplies, any unbalance in the three-phase source phase voltages and/or in the three single-phase modules will create a potential difference between the Y point of the single-phase modules and the source neutral point (neutral displacement voltage $V_{Y0}$), resulting in oscillations and significant variations of the input voltages of the single-phase converters [1]. For a stable and reliable operation, i.e., operation where the input voltage always stays within a specified range, a balancing control of the three single-phase modules is necessary. The stable and reliable operation also has to be guaranteed at startup, as well as in case of phase failure (open and short circuit) and load transients. The balancing control between the three single-phase modules can be achieved with additional passive components used to create a virtual (artificial) neutral point and by employing various balancing control methods [1]-[8], or by using only balancing control without additional passive components [9], [10].

Regardless of the balancing-control method used, the startup of the three single-phase modules should be controlled so that the PFC input currents and the PFC output voltages do not experience abrupt changes, such as significant current spikes and voltage overshoots. Until now, startup control methods of the Y-connected single-phase modules have not been addressed in the literature. Although the general principles of the single-phase ac-dc converter startup control are applied, such as monotonically increasing bulk voltage and limiting input current stress, the startup procedure of the Y-connected single-phase modules is much more complex and far from straightforward because of the coupling between the three single-phase modules.

In this paper, a detailed two-step startup procedure for the Y-connected single-phase modules is described. In the first step, during the precharging of the PFC output capacitors, the inrush currents are limited by employing silicon controlled rectifiers (SCRs). In the second step, the PFC output voltages are increased to their nominal value monotonically, with only minor overshoots, by modifying the conventional average-current control of the PFC stages. The complete startup procedure at both balanced and unbalanced input phase voltages is illustrated with MATLAB/Simulink simulation waveforms. Experimental results are also provided.

II. POWER STAGE AND CONTROL CIRCUIT

The simplified circuit diagram of the three single-phase modules with Y connection at the input and parallel connection at the output used to explain and verify the proposed startup-up procedure is shown in Fig. 1. For the circuit in Fig. 1, the input phase-to-phase voltage range is 320-530 Vrms, the line frequency range is 45-65 Hz, and the
nominal output voltage of the PFC stages is 400 V. The boost inductors and PFC output filter capacitors are $L_a = L_b = 90 \mu H$ and $C_{oa} = C_{ob} = C_{oc} = 810 \mu F$, respectively. The PFC stages operate with average current control as shown in Fig. 2. The switching frequency of the PFC stages is 100 kHz, whereas the current loop and voltage loop bandwidth is 8 kHz and 10 Hz, respectively. The PFC input current OCP is 50 A and the PFC output voltage OVP is 450 V. The dc-dc stages are LLC converters with current-mode control, where the output voltage controller is common for all three dc-dc stages [11]. The maximum output power is 6 kW. The circuit shown in Fig. 1 can be applied for different applications. For example, in telecom power supplies, the nominal output voltage of the dc-dc stages is 48V, whereas, in electric-vehicle chargers the dc-dc output voltage varies from 270 V to 430 V.

The balancing control between the three single-phase modules is achieved by balancing the input admittances of the PFC stages. To maintain equal input admittances, the outputs of the PFC voltage controllers must be equal [10]. With equal input admittances, for balanced source voltages, the total input power is equally distributed between the three single-phase modules. However, for unbalanced source voltages, to achieve equal input admittances, the total input power cannot be equally distributed between the three single-phase modules. In fact, a module connected to a reduced source voltage will draw less input current and, therefore, it will operate at reduced input power. The desired distribution of the total power between the single-phase modules that results in equal input admittances can be achieved by implementing the balancing-control circuit as introduced in [9] and explained in [10]. In this balancing circuit, the reference currents of the current controllers in the dc-dc stages are adjusted by balancing controllers that regulate the difference between the average output-voltage of the PFC controllers and the output voltage of an individual PFC controller. In the circuit in Fig. 1, the balancing loop bandwidth is 3 Hz.

It should be noted in Fig. 1 that the upper rectifiers in the input full-bridge rectifiers are replaced with silicon-controlled rectifiers (SCRs), which are used to limit the inrush currents during the startup; therefore, eliminating the startup resistors.

### III. Proposed Startup Procedure

Key waveforms during the proposed startup procedure for balanced source voltages and nominal phase voltage of 230 Vrms are shown in Fig. 3. The proposed startup procedure can be divided in two steps. In the first step, during time interval [$T_1-T_2$], the PFC output capacitors are precharged to one half of the peak value of the source phase-to-phase voltages ($230 \times \sqrt{2} \times \sqrt{3} / 2 = 282$ V) by controlling the conduction angle of the SCRs, while the boost switches are turned off. During [$T_2-T_3$], the dc-dc stages are also turned off, which means that the load current of the PFC stages is zero. In the second step, during time interval [$T_3-T_4$], the PFC output capacitors continue to charge at no load by the boost operation of the PFC switches until one output-capacitor voltage increases to the nominal value of 400 V and the corresponding dc-dc stage turns on carrying the total initial output load. During time interval [$T_4-T_5$], the voltage of the other two output capacitors sequentially increases to the nominal value of 400 V and the corresponding dc-dc stages turn on. At $T_5$, after all the three modules start carrying the initial output load, the balancing controller is turned on. Finally, during time interval [$T_5-T_6$], the transients of the load current between the three modules are settled and the system reaches a steady-state operation.

The conduction-angle control of the SCRs during the precharging of the PFC output capacitors is illustrated in Fig. 4. It can be seen in Fig. 4 that the control of SCRs is synchronized to the source phase-to-phase voltages. At the beginning of interval $T_6$ before the zero crossing of a phase-to-phase voltage (e.g., $v_{ab} > 0$), the corresponding pair of SCRs (SCR$_{a1}$ and SCR$_{a2}$) is turned on and two PFC output capacitors connected in series ($C_{oa}$ and $C_{ob}$) are equally charged through two small series resistors ($R_{oa}$ and $R_{ob}$) and two series diodes ($D_{oa}$ and $D_{ob}$) for a short time until the current through the SCRs decreases to zero and the SCRs turn off. By properly selecting the conduction angle of the SCRs, the inrush current pulses are limited below the OCP level. If for balanced source voltages of 230Vrms and $R_{sk} = 0.5 \Omega$,
$k \epsilon \{a, b, c\}$, $T_a$ is increased by 50 $\mu$s in every line cycle $T_1$ until $T_a$ increases to $T_1/4$, the inrush current pulses are limited below 25 A, which is well below the OCP level (50 A). With limited inrush currents, each PFC output capacitor gradually increases to one half of the peak value of the source phase-to-phase voltages. After $T_a$ increases to $T_1/4$, the gate pulses of the SCRs are permanently set high.

Key simulated waveforms during the precharging of the PFC output capacitors for unbalanced source phase voltages $V_{oa} = V_{ob} = 161 \text{ Vrms}$ and $V_{oc} = 230 \text{ Vrms}$, as an example, are presented in Fig. 5. It should be noted that waveforms in Fig. 5 are obtained by increasing $T_a$ by 50 $\mu$s in every line cycle similarly as in the case of the balanced input voltages in Fig. 3. It can be seen in Fig. 5 that the inrush current pulses are limited below 25 A and that the PFC output capacitors are precharged to different voltage levels ($V_{oa} = V_{ob} = 197 \text{ V}$ and $V_{oc} = 284 \text{ V}$). In fact, the PFC output capacitors are charged so that the total voltage on each pair of PFC output capacitors is equal to the peak value of the corresponding phase-to-phase voltage. It can be easily derived that for unbalanced source phase voltages $V_{oa} = V_{ob} = 161 \text{ Vrms}$ and $V_{oc} = 230 \text{ Vrms}$, the phase-to-phase voltages are $V_{ab} = 279 \text{ Vrms}$ and $V_{bc} = V_{ca} = 340 \text{ Vrms}$. Therefore,

$$V_{oa} = V_{ob} = \frac{\sqrt{2} \cdot V_{ab,rms}}{2} = \frac{\sqrt{2} \cdot 279}{2} = 197 \text{ V} \quad (1)$$

and

$$V_{oc} = \frac{\sqrt{2} \cdot V_{bc,rms}}{2} = \frac{\sqrt{2} \cdot 340}{2} = 284 \text{ V} \quad (2)$$

To better illustrate the rise of the PFC output capacitor voltages during the precharging interval, the waveforms in Fig. 5 around instant $T_1$ are zoomed in in Fig. 6. It can be seen in Fig. 6 that before the zero crossing of a particular phase-to-phase voltage, the corresponding pair of SCRs is turned on and the corresponding two capacitors connected in series are equally charged. However, as the peak values of the phase-to-phase voltages are unequal ($V_{ab, pk} < V_{bc, pk}$, $V_{bc, pk} = V_{ca, pk}$), PFC output capacitor voltages $V_{oa}$ and $V_{ob}$ increase with a smaller step before the zero crossing of phase-to-phase voltage $V_{ab}$ compared to the increase of pairs of PFC output capacitor voltages $V_{ab}$, $V_{oc}$ and $V_{oa, V_{oc}}$ before the zero crossing of phase-to-phase voltages $V_{bc}$ and $V_{ca}$, respectively.

As voltage $V_{oc}$ always increases with a larger step, its final value at the end of the precharging interval is larger than the final value of voltages $V_{oa}$ and $V_{ob}$.

In the second step of the proposed startup procedure, the input currents are limited below the OCP level by the soft start of the reference output voltage.
which represent the load controllers in the dc-dc stages for balanced source voltages, and with respect to Y point \([V]\), (b) input phase currents \([A]\), (c) PFC output voltages \([V]\), (d) PFC output voltages \([V]\), (e) PFC voltage controller outputs \([V]\), and (f) control pulses for SCR\(_{a1}\) and SCR\(_{a2}\), \(\epsilon\{a,b,c\}\).

It should be noted that in order to reduce the simulation time, in the simulation circuit the dc-dc output stages are replaced with current sources which represent the load currents of the PFC stages, i.e., the input currents of the dc-dc stages for balanced source voltages, and with controlled

current sources which are controlled by the output signals of the balancing controllers \([10]\). Instead of adjusting the reference currents of the current controllers in the dc-dc stages, the load currents of the PFC stages are adjusted.

**IV. MODIFIED AVERAGE-CURRENT CONTROL**

During time interval \([T_1-T_3]\) in Fig. 3, the balancing controller is turned off and, therefore, the neutral displacement voltage \(V_{Y0}\) can potentially increase, resulting in significant unbalances in the input voltages of the PFC stages and, eventually, one PFC output voltage could increase to the OVP level. In order to limit the increase of voltage \(V_{Y0}\), during \([T_1-T_3]\) the conventional average-current control of the PFC stages is modified so that instead of generating a reference input current to be proportional to its voltage-controller output, each reference input current is generated to be proportional to the average value of the outputs of all three voltage controllers. The difference in operation between the conventional and modified average-current control during startup is illustrated with simulated waveforms for balanced source phase voltages (230 Vrms) and no load in Figs. 7 and 8. All simulated results in this paper are obtained in MATLAB/Simulink.

In Fig. 7, with conventional average-current control, PFC output voltages \(V_{oa}\) and \(V_{oc}\) increase above 450 V, which would trigger OVP, whereas, \(V_{oa}\) stays constant at 410 V. After PFC output voltages increase above their nominal value of 400 V, PFC voltage controller outputs \(V_{E_{kav}}, k \epsilon\{a,b,c\}\), become unequal \((V_{E_{ab}}) > V_{E_{ab}}, V_{E_{ab}} \approx V_{E_{ak}}\) making input admittances \(Y_{a} \neq Y_{b}, Y_{b} \approx Y_{c}\), which results in an increased amplitude of voltage \(V_{Y0}\) that is in phase with input

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**Fig. 6** Zoomed-in waveform around instant \(T_1\) in Fig. 5: (a) source phase-phase voltages \([V]\), (b) input phase currents \([A]\), (c) PFC output voltages \([V]\), (d), (e), and (f) control pulses for SCR\(_{a1}\) and SCR\(_{a2}\), \(\epsilon\{a,b,c\}\).

**Fig. 7** Key simulated waveforms during startup with conventional average-current control for balanced source phase voltages (230 Vrms) and no load: (a) low-pass filtered input phase voltages with respect to Y point \([V]\), (b) input phase currents \([A]\), (c) rectified phase current references \([A]\), (d) PFC output voltages \([V]\), (e) PFC voltage controller outputs \([V]\), (f) low-pass filtered \(V_{oa}\) \([V]\), and (g) duty cycle of boost switches \([\text{digital values with respect to } C_{\text{osc}}=300]\).

**Fig. 8** Key simulated waveforms during startup with modified average-current control for balanced source phase voltages (230 Vrms) and no load: (a) low-pass filtered input phase voltages with respect to Y point \([V]\), (b) input phase currents \([A]\), (c) rectified phase current references \([A]\), (d) PFC output voltages \([V]\), (e) PFC voltage controller outputs \([\text{digital value in Q12 format}]\), (f) low-pass filtered \(V_{oa}\) \([V]\), and (g) duty cycle of boost switches \([\text{digital values with respect to } C_{\text{osc}}=300]\).
voltage of module “a”, $V_{oa}$, as shown in Fig. 7. Therefore, amplitude of $V_{av}=V_{ao}+V_{vb}$ is decreased, whereas, amplitude of $V_{av}$ and $V_{ov}$ is increased. Due to the increased input voltages of modules “b” and “c”, their output voltages $V_{ob}$ and $V_{oc}$ increase above 400 V.

In Fig. 8, with modified average-current control, the three PFC output voltages are approximately equal and well below the OVP limit. After the PFC output voltages increase above their nominal value of 400 V, despite the unequal outputs of their PFC voltage controllers, input admittances $Y_i$ are still approximately equal because the amplitudes of the reference input currents are equal since they are generated from the average value of the outputs of the three PFC voltage controllers. As a result, the amplitude of voltage $V_{yo}$ is significantly smaller compared to that in Fig. 7. Therefore, the amplitude of input voltages $V_{oy}$, $V_{oz}$, and $V_{oy}$ is approximately the same. Also, the amplitude of $V_{oy}$ and $V_{oz}$ is smaller than that in Fig. 7. Consequently, PFC output voltages $V_{oa}$, $V_{ob}$, and $V_{oc}$ are approximately equal and they increase to a lower level (= 420 V) compared to that in Fig. 7.

It follows from Figs. 7 and 8 that during startup with no load, the PFC output voltages cannot be regulated. To achieve regulation, an initial load should be applied to each module when its PFC output voltage increases to the nominal level of 400 V, as explained in Section III. Key simulated waveforms during the second step of the proposed startup procedure for balanced source voltages (230 Vrms) and 600-W load are presented in Fig. 9. During time interval $[T_1-T_2]$, the PFC output voltages increase following the reference voltage ramp whose initial value is equal to the precharged voltage of the PFC output capacitor voltages. At instant $T_2$, PFC output voltage $V_{ob}$ increases to 400 V and the total 600-W load (i.e., 1.5 A load current) is applied to the output of PFC stage “b”. Shortly after $T_2$, $V_{oc}$ increases to 400 V and the 1.5-A load current will be equally distributed between modules “b” and “c”. At instant $T_3$, PFC output voltage $V_{oa}$ also increases to 400 V and from that time on the 1.5-A load current will be equally shared between the three modules. It should be noted that during $[T_1-T_2]$, the PFC stages operate with modified average-current control, where the reference input currents are proportional to the average value of the outputs of the three voltage controllers, $V_{Edavg}$. As a result, during $[T_1-T_3]$ amplitude of voltage $V_{yo}$ is small, as can be seen in Fig. 9. At $T_3$, when all three PFC stages are loaded, the balancing controller is turned on and the average current control is changed from modified to conventional, where each input reference current is proportional to the output of its own voltage controller. This transition results in increased amplitude of voltage $V_{yo}$. At $T_4$, the transients of the load current between the three modules are settled and the system reaches a steady-state operation with a reduced amplitude of voltage $V_{yo}$. It should be noted in Fig. 9 that the overshoot of the PFC output voltages is only 10 V.

Key simulated waveforms during the second step of the proposed startup procedure for unbalanced source phase voltages, $V_{ao}=V_{bo}=161$ Vrms and $V_{co}=230$ Vrms, and 600-W load are presented in Fig. 10. It can be seen in Fig. 10 that PFC output voltage $V_{oc}$ increases above the OVP level ($V_{ow}=457$V), while $V_{oa}$ increases almost to the OVP level ($V_{oa}=447$V). It can also be seen in Fig. 10 that compared to Fig. 9, during $[T_1-T_3]$ the outputs of the PFC voltage controllers deviate more from their average value. As a result, at $T_3$, when balancing controller is turned on, the amplitude of adjustment currents is larger compared to that in Fig. 9. Also, after $T_3$, when average current control is changed from modified to conventional, the amplitude of

Fig. 9 Key simulated waveforms during startup with modified average-current control for balanced source phase voltages (230 Vrms) and 600-W load: (a) low-pass filtered input phase voltages with respect to Y point [V], (b) input phase currents [A], (c) PFC output voltages [V], (d) PFC voltage controller outputs [digital value in Q12 format], (e) low-pass filtered $V_{vo}$ [V], (f) adjustment currents [A], and (g) PFC load currents [A].

Fig. 10 Key simulated waveforms during startup with modified average-current control for unbalanced source phase voltages ($V_{ao}=V_{bo}=161$ Vrms, $V_{co}=230$ Vrms) and 600-W load: (a) low-pass filtered input phase voltages with respect to Y point [V], (b) input phase currents [A], (c) PFC output voltages [V], (d) PFC voltage controller outputs [digital value in Q12 format], (e) low-pass filtered $V_{vo}$ [V], (f) adjustment currents [A], and (g) PFC load currents [A].
voltage $V_{j0}$ increases to a larger value compared to that in Fig. 9.

In order to limit the overshoot of the PFC output voltages below 450V for unbalanced source voltages, two approaches can be used depending on applications. Generally, in applications where the startup can be performed at any load, an increased initial load should be used. However, in applications where the startup cannot be performed at higher loads, the PFC voltage-controller bandwidth should be increased.

To illustrate the startup with an increased initial load, key simulated waveforms during the second step of the proposed startup procedure for unbalanced source phase voltages, $V_{a0} = V_{b0} = 161$ Vrms and $V_{c0} = 230$ Vrms, and 1500-W load are presented in Fig. 11. It can be seen in Fig. 11 that the overshoot of the PFC output voltages is 20 V, i.e., it is well below the OVP level. It can also be seen in Fig. 11 that compared to Fig. 10, during $[T_1-T_3]$ the outputs of the PFC voltage controllers deviate less from their average value. As a result, at $T_3$, when balancing controller is turned on and the average current control changes from modified to conventional, the amplitude of the adjustment currents as well as the amplitude of voltage $V_{j0}$ are smaller compared to those in Fig. 10. Finally, at $T_4$, when the system reaches a steady state, the amplitude of $V_{j0}$ is significantly smaller than that in Fig. 10.

To illustrate the startup with an increased PFC voltage-controller bandwidth, key simulated waveforms during the second step of the proposed startup procedure for unbalanced source phase voltages, $V_{a0} = V_{b0} = 161$ Vrms and $V_{c0} = 230$ Vrms, 600-W load, and increased voltage-controller bandwidth from 10 Hz in steady state to 100 Hz are presented in Fig. 12. It can be seen in Fig. 12 that the overshoot of the PFC output voltages is 44 V, i.e., it is slightly below the OVP level. It can also be seen in Fig. 12 that compared to Fig. 10, during $[T_1-T_3]$ the outputs of the PFC voltage controllers deviate more from their average value. However, at $T_3$, when the average current control is changed from modified to conventional, the increased bandwidth of the PFC voltage controllers helps to achieve steady state values of the PFC voltage-controller outputs faster. This results in lower amplitude of $V_{j0}$ compared to that in Fig. 10. Also, after $T_3$, when balancing controller is turned on, the adjustment currents reach their steady state values faster than in Fig. 10. It should be noted in Fig. 12 that after the adjustment currents reach their steady state values and the load current transients are settled, the PFC voltage-controller bandwidth is changed back to 10Hz from 100Hz. It should also be noted in Fig. 12 that when PFC output capacitor voltage $V_{oc}$ increases above 400V, the output $V_{Ec}$ of the PFC voltage controller “c” becomes saturated. However, during $[T_1-T_3]$, phase “c” current reference is proportional to $V_{Edc}$ instead of $V_{Ec}$. As $V_{Edc}$ is greater than $V_{Ec}$, the amplitude of current reference of phase “c” is greater than the required value and, consequently, $V_{oc}$ exhibits an overshoot.

In order to reduce the overshoot of $V_{oc}$ in Fig. 12, the startup procedure is further modified as illustrated in Fig. 13. In fact, at $T_3$, when $V_{oc}$ increases to 400V, the average current control of phase “c” is changed from modified to conventional, where phase “c” current reference is proportional to the output of its own voltage controller. At

![Fig. 11 Key simulated waveforms during startup with modified average-current control for unbalanced source phase voltages ($V_{a0}=V_{b0}=161$Vrms, $V_{c0}=230$Vrms) and 1500W load: (a) low-pass filtered input phase voltages with respect to Y point [V], (b) input phase currents [A], (c) PFC output voltages [V], (d) PFC voltage controller outputs [digital value in Q12 format], (e) low-pass filtered $V_{vo}$ [V], (f) adjustment currents [A], and (g) PFC load currents [A].](image1)

![Fig. 12 Key simulated waveforms during startup with modified average-current control with ten times increased PFC voltage controller bandwidth (100Hz) for unbalanced source phase voltages ($V_{a0}=V_{b0}=161$Vrms, $V_{c0}=230$Vrms) and 600W load: (a) low-pass filtered input phase voltages with respect to Y point [V], (b) input phase currents [A], (c) PFC output voltages [V], (d) PFC voltage controller outputs [digital value in Q12 format], (e) low-pass filtered $V_{vo}$ [V], (f) adjustment currents [A], and (g) PFC load currents [A].](image2)
Fig. 13 Key simulated waveforms during startup with further modified average-current control with ten times increased PFC voltage controller bandwidth (100Hz) for unbalanced source phase voltages ($V_{a0}$=161Vrms, $V_{c0}$=230Vrms) and 600W load: (a) low-pass filtered input phase voltages with respect to Y point [V], (b) input phase currents [A], (c) PFC output voltages [V], (d) PFC voltage controller outputs [digital value in Q12 format], (e) low-pass filtered $V_{vo}$ [V], (f) adjustment currents [A], and (g) PFC load currents [A].

At the same time, the current references of phases “a” and “b” are still proportional to the average value of the outputs of all three voltage controllers. After $T_2$, when $V_{oc}$ increases to 400V, the average current control of phase “b” is changed from modified to conventional, while the current reference of phase “a” is still proportional to the average value of the outputs of all three voltage controllers. Finally, at $T_3$, when $V_{oa}$ increases to 400V, the average current control of phase “a” is changed from modified to conventional. At the same time, the balancing controllers are turned on. It can be seen in Fig. 13 that the overshoot of the PFC output voltages is only 15 V, i.e., it is well below the OVP level. It should be noted in Fig. 13 that the output $V_{Eoc}$ of the PFC voltage controller “c” is not saturated.

V. EXPERIMENTAL RESULTS

Experimental results obtained on an 11-kW prototype for balanced (230 Vrms) and unbalanced (207 Vrms, 230 Vrms, and 253 Vrms) source phase voltages and 5.5-kW load are presented in Figs. 14 and 15, respectively. It can be seen in Figs. 14 and 15, that the maximum overshoot of the PFC output voltages is 20 V, which is well below the OVP level of 450 V and that the maximum inrush current spike is approximately 90 A which is below the OCP level of 100 A specified for the 11-kW prototype. It should be noted that the limited overshoot of the PFC output voltages is achieved by implementing the proposed startup procedure at an increased initial load. It should also be noted that during the precharging of the PFC output capacitors, the inrush current spikes are limited by increasing interval $T_n$ before the zero crossing of a relevant phase-to-phase voltage by 20µs in every line cycle $T_1$ until $T_a$ is increased to $T_1/4$. Finally, it should be noted that in both Figs. 13 and 14, that unlike in the simulation results, a second group of current spikes exists near the end of the precharging interval of the PFC output capacitors. These additional current spikes are caused by inaccuracies in determining the line frequency and by setting the gate pulses of the SCRs permanently to high when $T_a$ is still smaller than $T_1/4$.

VI. SUMMARY

In this paper, a detailed two-step startup procedure for the Y-connected single-phase modules is described. The proposed startup procedure ensures that even at unbalanced source voltages, neutral displacement voltage $V_{yo}$ is properly controlled so that the input voltage of the single-phase modules stays within a specified limit, while PFC front end output voltages increase monotonically and their inrush currents are below a specified level.

During the first step of the proposed startup procedure, when all boost switches and the dc-dc stages are off, the PFC output capacitors are monotonically precharged to one half of the peak value of the source phase-to-phase voltages. The inrush currents are limited by employing conduction-angle control of silicon controlled rectifiers (SCRs). The control of the SCRs is synchronized to the zero crossing of the source phase-to-phase voltages.

During the second step of the proposed startup procedure, the PFC output voltages are increased almost monotonically to their nominal value by modifying the conventional average-current control of the PFC stages. The conventional
average-current control of the PFC stages is modified so that instead of generating a reference input current to be proportional to its voltage-controller output, each reference input current is generated to be proportional to the average value of the outputs of all three voltage controllers. With this modified control, the PFC output voltages sequentially increase to the nominal value of 400 V with the dc-dc stages turned off. After a PFC voltage increases to 400 V, its dc-dc stage with some initial load is turned on. After all three dc-dc stages are turned on and the three modules share the load current, the average current control is changed from modified to conventional and the balancing controllers are turned on. At the end of the second step, the transients of the load current between the three modules are settled and system reaches a steady-state operation.

The complete startup procedure at both balanced and unbalanced source phase voltages is illustrated with MATLAB/Simulink simulation waveforms. Experimental results are also provided.

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