DC-link Capacitor Voltage Balancing Control for Series Half Bridge LLC Resonant Converter

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Abstract—This paper presents control methods that achieve DC-link capacitor voltage balance of a series half bridge (SHB) LLC resonant converter operating at different modulation schemes. The principle of the proposed balancing control method is analyzed and studied based on six normally used operation modes of the SHB LLC converter. DC-link capacitor voltage balancing strategies are developed separately for two common modulation schemes in SHB topology. The performance of the proposed voltage balancing control method is experimentally verified on a 7.5-kW SHB LLC DC/DC converter prototype under different operating conditions.

Keywords—LLC, resonant converter, voltage balancing, series half bridge

I. INTRODUCTION

The LLC resonant converter topology has been widely employed as an isolated DC/DC converter, due to its high efficiency, simple structure achieved by magnetic integration, soft switching on both primary and secondary switches, and capability suitable for applications with wide voltage ranges, [1], [2], [3]. In comparison with the conventional full-bridge or half-bridge topology, three-level topology in [4] is more attractive in high power and high input voltage applications, because of the fact that each switching device needs to block only one half of the input voltage. Three-level topology was applied to LLC converters in [5]. The proposed converters achieve ZVS for the switches without additional auxiliary circuit. In [6], SHB topology was proposed for the first time. This topology removes the two clamping diodes in comparison with the conventional three-level topology from [4]. In [7], an asymmetric modulation was investigated and employed to halve the switching frequency of the primary switches and effectively reduce the driving loss. For applications with wide input voltage ranges, both symmetric and asymmetric modulations were applied to SHB LLC converters as reported in [8] and [9]. The SHB topology modulation schemes have been further discussed for isolated multilevel DC-DC converter in solid state transformer applications in [10]. In [11], two-level and three-level modulations were applied to the SHB LLC converter to approximately double the range of its input voltage. Recently, many other studies have been carried out on the LLC converter that adopts SHB topology at the primary side. For example, [12] mainly focuses on phase-shift modulation control that is suitable for wide input voltage applications, and [13] focuses on balancing control of the currents flowing through the power switches.

Voltage imbalance between the series connected DC-link capacitors is mainly caused by the parameter mismatch of the equivalent series resistances (ESR) and capacitances of the DC-link capacitors as well as the timing mismatch of gate signals for the switches. Imbalance of the voltages can be severe at high switching frequency and high input voltage, which can cause damage to devices and system failure by excessive voltage stresses. However, until now, there are few studies discussing about the voltage balancing in SHB LLC resonant converter.

In this paper, a voltage balancing control method for the split DC-link capacitors of the SHB LLC resonant converter is presented. Imbalance between the voltages of the split DC-link capacitors is investigated and the operating principle of the balancing control is analyzed. Balanced strategies suitable for two common modulations in the SHB structure are developed. The performance of the proposed balancing method is experimentally verified on a 7.5-kW SHB LLC DC/DC converter prototype that operates at various operating conditions.

II. PRINCIPLE OF THE PROPOSED BALANCING CONTROL

A. DC-link Capacitor Voltage Imbalance in SHB Topology

Fig. 1 shows SHB LLC topology that employs SHB structure on the primary side, which includes four switching devices $S_I$ to $S_4$ and DC-link capacitors $C_1$ and $C_2$. Resonant capacitor $C_R$, transformer leakage inductor $L_s$ and transformer magnetizing inductor $L_m$ form the LLC resonant tank. A full bridge diode rectifier is placed on the secondary side of the transformer, which can also be replaced by active switches for synchronize rectification. The reference directions of capacitor currents $i_{C_1}$ and $i_{C_2}$, neutral point (NP) current $i_{NP}$, and resonant current $i_{L_R}$ are also depicted in Fig. 1.

Ideally, when the top capacitor and bottom capacitor deliver the same amount of power to the resonant tank, the DC-link capacitor voltage is automatically balanced without any additional control. However, the parameter mismatch of the ESRs and capacitances of the DC-link capacitors as well as the timing mismatch of the gate signals are inevitable in any practical circuit, which leads to the DC-link capacitor voltage imbalance under various conditions. The influence of the aforementioned mismatches to the DC-link capacitor voltage imbalance is thoroughly investigated by simulations based on the parameters of a prototype.
When all the components in the simulation are ideal, a few nanoseconds of gate signals delay for $S1$ and $S2$ in symmetric modulation can cause divergence of the capacitor voltages and results in one capacitor voltage eventually increasing to the total input voltage. In every switching period, the gate signals delay leads to a charging process to one DC-link capacitor and a discharging process to another DC-link capacitor until one capacitor voltage reaches the total input voltage. But if component parasitics are considered in the simulation, the divergence of the capacitor voltage becomes mitigated by the switching process of non-ideal power devices. For instance, when the MOSFETs output capacitances are considered in the simulation, the DC capacitor voltages can reach steady state below full input voltage under the same conditions. Fig. 2 shows the imbalance of capacitor voltages when the SHB LLC circuit operates at 1000 V input voltage for 7.5 kW output power under symmetric modulation, where a few nanoseconds of gate signals delay for $S1$ and $S2$ can cause significant voltage imbalance. In addition, the imbalance becomes larger as the switching frequency increase due to the fact that the same amount of time mismatch becomes larger duty cycle mismatch at higher switching frequencies. On the other hand, when the SHB LLC circuit operates at 1000 V input voltage for 3.75 kW output power under asymmetric modulation, the capacitor voltage mismatch is summarized in Fig. 3, where the voltage imbalance is not as severe as that in symmetric modulation.

The impact on the voltage imbalance due to the capacitance mismatch and ESR mismatch of DC-link capacitors is also thoroughly investigated at the same conditions in simulation. These mismatches can cause voltage imbalance at transient when power devices are turned on and off, but no obvious voltage imbalance is observed at steady state.

Therefore, an effective balancing control method becomes critical for safe operation of the SHB LLC converter.

**B. Principle of the Proposed Voltage Balancing Control**

When the SHB topology operates under either symmetric modulation or asymmetric modulation, total six modes are defined based on NP current direction, resonant current direction, and turned-on switches, shown in Fig. 4. Table 1 lists six modes and their corresponding conditions.

<table>
<thead>
<tr>
<th>Mode</th>
<th>$i_{SN}$</th>
<th>$i_{SR}$</th>
<th>On Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Zero</td>
<td>Positive or Negative</td>
<td>$S1$ &amp; $S4$</td>
</tr>
<tr>
<td>2</td>
<td>Zero</td>
<td>Positive or Negative</td>
<td>$S2$ &amp; $S3$</td>
</tr>
<tr>
<td>3</td>
<td>Positive</td>
<td>Negative</td>
<td>$S1$ &amp; $S3$</td>
</tr>
<tr>
<td>4</td>
<td>Negative</td>
<td>Positive</td>
<td>$S1$ &amp; $S3$</td>
</tr>
<tr>
<td>5</td>
<td>Positive</td>
<td>Positive</td>
<td>$S2$ &amp; $S4$</td>
</tr>
<tr>
<td>6</td>
<td>Negative</td>
<td>Negative</td>
<td>$S2$ &amp; $S4$</td>
</tr>
</tbody>
</table>

The principle of the proposed DC-link capacitor voltage balancing control is described as follows. When $S1$ and $S4$ are on as shown in Fig. 4 (a), the full input voltage $V_{in}$ is applied to the resonant tank. No current is coming out of or going into the neutral point $O$. This is also valid when $S2$ and $S3$ are on, during which the resonant current is freewheeling through $S2$ and $S3$, as shown in Fig. 4 (b). Equation (1) describes the behavior of the DC-link capacitors voltages during these two modes, where these two modes do not change the DC-link capacitor voltage.

\[
i_{c1} = i_{c2} = 0
\]

\[
\Delta V_{c1} = \Delta V_{c2} = \int \frac{i_{c1}}{C_1} dt = \int \frac{i_{c2}}{C_2} dt = 0 \tag{1}
\]

In contrast, when $S1$ and $S3$ or $S2$ and $S4$ are on, either the top capacitor or the bottom capacitor voltage is applied to the
equal to the input DC voltage \( V_0 \) given the capacitances are equal. When \( i_{\text{NP}} \) is positive, the top capacitor is charged while the bottom capacitor is discharged, which increases \( V_{\text{PO}} \) and decreases \( V_{\text{ON}} \) according to equation (2).

\[
\begin{align*}
\Delta V_{C_1} &= \int_{t_1}^{t_2} \frac{i_{\text{c1}}}{C_1} \, dt, \\
\Delta V_{C_2} &= \int_{t_2}^{t_3} \frac{i_{\text{c2}}}{C_2} \, dt, \\
\Delta V_{\text{NP}} &= \Delta V_{C_1} - \Delta V_{C_2} > 0 \tag{2}
\end{align*}
\]

On the other hand, when \( i_{\text{NP}} \) is negative, the top capacitor is discharged while the bottom capacitor is charged, which decreases \( V_{\text{PO}} \) and increases \( V_{\text{ON}} \). This process can be described in equation (3).

\[
\begin{align*}
\Delta V_{C_1} &= \int_{t_1}^{t_2} \frac{i_{\text{c1}}}{C_1} \, dt, \\
\Delta V_{C_2} &= \int_{t_2}^{t_3} \frac{i_{\text{c2}}}{C_2} \, dt, \\
\Delta V_{\text{NP}} &= \Delta V_{C_1} - \Delta V_{C_2} < 0 \tag{3}
\end{align*}
\]

Similarly, equation (2) and (3) are also valid when \( S_1 \) and \( S_3 \) are off and \( S_2 \) and \( S_4 \) are on as shown in Fig. 4(e) and (f), respectively.

In summary, regardless of other conditions, positive \( i_{\text{NP}} \) increases voltage difference, \( \Delta V = V_{\text{PO}} - V_{\text{ON}} \), negative \( i_{\text{NP}} \) reduces \( \Delta V \), and zero \( i_{\text{NP}} \) has no influence on \( \Delta V \). Therefore, DC-link capacitor voltage balance can be achieved by controlling the NP current.

III. DC-LINK CAPACITOR VOLTAGE BALANCE STRATEGIES IN DIFFERENT MODULATIONS

Voltage balancing strategies are developed for two commonly used modulation schemes in this section based on the analysis in Section II.

A. Symmetric Modulation

Symmetric modulation is the most common modulation in SHB LLC topology, which utilizes the full input voltage and is capable of delivering the full power to load. With the modulation shown in Fig. 5(a), the SHB circuit delivers the full input voltage to the resonant tank when \( S_1 \) and \( S_4 \) are on, and zero voltage when \( S_2 \) and \( S_3 \) are on. Because this modulation contains only two modes as shown in Fig. 4(a) and (b), simply modifying the duty cycle of these two modes cannot affect the voltage imbalance according to the previous analysis. Thus, extra modes should be introduced to balance the capacitor voltage. When the imbalance voltage \( \Delta V > 0 \), mode 4 and mode 6 with negative NP current are applied to reduce \( \Delta V \). When the imbalance voltage \( \Delta V < 0 \), mode 3 and mode 5 with positive NP current are used to increase \( \Delta V \).

In order to generate desired modes and control their duration, a phase shift technique is utilized. Leading \( S_1 \) and \( S_2 \) with respect to \( S_4 \) and \( S_3 \) introduces mode 3 and mode 5, and lagging \( S_1 \) and \( S_2 \) to \( S_4 \) and \( S_3 \) provides mode 4 and mode 6. An example is shown in Fig. 5(b) to generate mode 4 and mode 6 with phase angle \( \phi \). The voltage difference \( V_{\text{diff}} \) during mode 4 or mode 6 can be calculated according to equation (4), where \( C = C_1 = C_2 \). Negative \( i_{\text{NP}} \) in mode 4 and mode 6 results in negative \( V_{\text{diff}} \) while positive \( i_{\text{NP}} \) in mode 3 and mode 5 introduces positive \( V_{\text{diff}} \).

\[
V_{\text{diff}} = \Delta V_{C_1} - \Delta V_{C_2} = \int_{t_1}^{t_2} \frac{i_{\text{c1}}}{C_1} \, dt - \int_{t_2}^{t_3} \frac{i_{\text{c2}}}{C_2} \, dt = \int_{t_1}^{t_2} \frac{i_{\text{NP}}}{C} \, dt \tag{4}
\]
The control diagram of the proposed voltage balancing control for symmetric modulation is shown in Fig. 5. (c). The top capacitor voltage $V_{PO}$ and bottom capacitor voltage $V_{ON}$ are sensed and compared with each other to generate the voltage difference $\Delta V$. When voltage difference is smaller than the threshold voltage $V_{th}$, no phase shift command is generated to avoid undesired control oscillation. Once the voltage difference is larger than the threshold voltage $V_{th}$, a phase angle $\phi$ command is calculated through a proportional controller, which is an effective compensator in this controller. The phase shift angle command is further passed to the phase shift generation block, 

![Diagram](image-url)
where the carrier is then phase shifted to finally produce desired gate signals for all the switches.

B. Asymmetric Modulation

Asymmetric modulation shown in Fig. 6 (a) delivers only one half of the input voltage to the resonant tank while halving the switching frequency of the primary switches, [7]. This modulation is often applied to reduce the switching frequency on the primary devices or decrease the gain of the LLC circuit. Rather than having only mode 1 and mode 2 in symmetric modulation, asymmetric modulation includes mode 3 to mode 6 from (c) to (f) in Fig. 4.

According to the previous analysis, mode 4 and mode 6 with negative NP current can decrease $\Delta V$, while mode 3 and mode 5 with positive NP current can increase $\Delta V$. Therefore, when $\Delta V > 0$, mode 4 or mode 6 is extended while mode 3 or mode 5 is narrowed. Similarly, when $\Delta V < 0$, mode 4 or mode 6 is shortened. An example is illustrated in Fig. 6 (b) where mode 4 gets shortened by reducing the duty cycle of $S_1$ while mode 5 becomes extended by increasing the duty cycle of $S_4$. The voltage difference between the top and bottom capacitors in one switching period is shown in equation (5).

$$V_{\text{diff}} = \Delta V_{C_1} - \Delta V_{C_2} = \left[-\int_{t_1}^{t_2} \frac{I_{L1}}{C_1} \, dt - \int_{t_3}^{t_4} \frac{I_{L2}}{C_2} \, dt \right] + \left[\int_{t_3}^{t_4} \frac{I_{L1}}{C_1} \, dt + \int_{t_3}^{t_4} \frac{I_{L2}}{C_2} \, dt \right]$$

(5)

Assuming the resonant current is not affected when the modes are slightly extended or shortened, $V_{\text{diff}}$ is only dependent on the duration of $t_1$-$t_2$ and $t_3$-$t_4$. By adjusting the duty cycle of $S_1$ and $S_4$, the duration of $t_1$-$t_2$ and $t_3$-$t_4$ can be modified, and the DC-link capacitor voltage balance can then be obtained.

The control diagram of the proposed voltage balancing control for asymmetric modulation is shown in Fig. 6 (c). Rather than sending the phase shift command to gate signal generation block in symmetric modulation, the controller passes the duty cycle difference command once voltage difference exceeds the threshold voltage $V_{th}$.

IV. EXPERIMENTAL RESULTS

A prototype hardware which adopts SHB LLC topology has been built in the lab shown in Fig. 7. Table 2 lists all key parameters of this prototype.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage $V_{in}$</td>
<td>1000 V</td>
</tr>
<tr>
<td>Output Voltage $V_o$</td>
<td>750 V</td>
</tr>
<tr>
<td>Resonant Capacitance $C_r$</td>
<td>253 nF</td>
</tr>
<tr>
<td>Resonant Inductance $L_r$</td>
<td>10 uH</td>
</tr>
<tr>
<td>Magnetizing Inductance $L_m$</td>
<td>80 uH</td>
</tr>
<tr>
<td>Turns ratio $n$</td>
<td>10:15</td>
</tr>
<tr>
<td>DC-link Capacitance $C_1$</td>
<td>713 uF</td>
</tr>
<tr>
<td>DC-link Capacitance $C_2$</td>
<td>705 uF</td>
</tr>
</tbody>
</table>
The proposed DC-link capacitor voltage balancing strategies have been tested at various conditions on this prototype. Without balancing control, when the converter operates at 1-kV input voltage for 7.5 kW output power using symmetric modulation, voltage imbalance exists between the top and bottom capacitors as illustrated in Fig. 8 (a) to (c). Testing results reveal this imbalance is more severe at 120 kHz switching frequency in Fig. 8 (c) than at 100 kHz switching frequency in Fig. 8 (a), which verifies the analysis in Section II. Due to the practical non-ideal switching process of the power devices, the mismatch is further mitigated in testing results compared with simulation results in Fig. 2. In Fig. 8 (d), implementing the proposed balancing control method results in only 1-V voltage difference at 120 kHz switching frequency. Fig. 9 summarizes the voltage imbalance with symmetric modulation under various conditions.

Fig. 8 Voltage imbalance under symmetric modulation (a) 5-V without balancing control at $f_{sw}$=100 kHz, (b) 8-V without balancing control at $f_{sw}$=110 kHz, (c) 12-V without balancing control at $f_{sw}$=120 kHz, (d) only 2-V with balancing control at $f_{sw}$=120 kHz.

Fig. 9 Voltage difference comparison at various condition under symmetric modulation

Fig. 9 Voltage imbalance under asymmetric modulation (a) 6-V average voltage imbalance without balancing control at $f_{sw}$=50 kHz, (b) 2-V average voltage imbalance with balancing control at $f_{sw}$=50 kHz.

The proposed DC-link capacitor voltage balancing strategies have been tested at various conditions on this prototype. Without balancing control, when the converter operates at 1-kV input voltage for 7.5 kW output power using symmetric modulation, voltage imbalance exists between the top and bottom capacitors as illustrated in Fig. 8 (a) to (c). Testing results reveal this imbalance is more severe at 120 kHz switching frequency in Fig. 8 (c) than at 100 kHz switching frequency in Fig. 8 (a), which verifies the analysis in Section II. Due to the practical non-ideal switching process of the power devices, the mismatch is further mitigated in testing results compared with simulation results in Fig. 2. In Fig. 8 (d), implementing the proposed balancing control method results in only 1-V voltage difference at 120 kHz switching frequency. Fig. 9 summarizes the voltage imbalance with symmetric modulation under various conditions.
Without balancing control, when the converter runs at 1-kV input voltage for 3.75 kW output power using asymmetric modulation, 6-V voltage imbalance exists between the top and bottom capacitors as illustrated in Fig. 9 (a). In Fig. 9 (b), implementing the proposed balancing control method results in only 2-V voltage difference at the same conditions.

V. CONCLUSION

In this paper, DC-link capacitor voltage balancing control methods for SHB topology applied in an LLC DC/DC converter are presented. In the proposed approach, the neutral point voltage is controlled by adjusting the neutral point current. Balancing strategies are developed separately for two widely used modulation schemes in SHB topology. Finally, the performance of the proposed balancing control methods is experimentally verified on a 1000-V input, 7.5 kW SHB based LLC DC/DC converter prototype. The measured results are line with the theory presented in the show that the DC-link capacitor voltage is well balanced when the SHB is operating at both symmetric and asymmetric modulation schemes.

REFERENCES


