A New Two-Switch PFC DCM Boost Rectifier for Aviation Applications

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Abstract—A new two-switch, single-phase, power-factor-correction (PFC), discontinuous-conduction-mode (DCM) boost rectifier that features zero-voltage switching (ZVS) and can achieve less than 5% input-current total harmonic distortion (THD) by injecting a simple feedforward signal obtained from input and output voltages to the output voltage feedback control is introduced. Since low THD is achieved without high bandwidth active current shaping control, the proposed topology is suitable for modern aviation applications that require line frequency up to 800 Hz. The evaluation was performed on a 320 W prototype designed to operate from 94-134 V line input and deliver 220 V dc output. The prototype achieves 2.3% THD at full load over the line frequency range from 360 Hz to 800 Hz and meets the required harmonic limits specified by the DO-160 standard that describes the environmental conditions and test procedures for airborne equipment.

Keywords—ZVS, PFC, boost rectifier, aviation, single phase, DCM

I. INTRODUCTION

In the aviation industry, electric power loads and source properties are regulated by the DO-160 standard [1] that specifies stringent harmonic limits of airborne power equipment. Moreover, modern airborne power distribution systems employ line frequency up to 800 Hz to increase the performance of on-board generators and to reduce the size of on-board passive elements such as transformers and filters [2]-[4].

Conventional continuous-conduction-mode (CCM) PFC boost rectifiers are well optimized to the line frequency of 50 or 60 Hz by employing an active input current shaping control with bandwidth around 3-5 kHz to obtain low THD. To achieve similar current shaping performance at the line frequency of 800 Hz, the current control bandwidth should be designed to be around 50 kHz. However, it is not possible to achieve the high bandwidth current control with hard-switching CCM PFC boost rectifiers that are mostly designed to operate below 100 kHz switching frequency to meet the required efficiency and thermal performance [5]-[8].

Recently, totem-pole bridgeless PFC rectifiers with wide-bandgap (WBG) devices operating in the critical conduction mode were introduced [9]-[11]. To achieve low THD, zero crossing of boost inductor current as well as line input voltage should be properly detected without much delay. However, by using the existing current sensing techniques, commercially available gate drivers with propagation delay, and a digital controller that has limited processing speed [12-13], it is virtually impossible to achieve less than 5% THD at 800 Hz line frequency.

In this paper, a new, two-switch, single-phase, PFC, DCM boost rectifier that features ZVS and can achieve less than 5% input-current THD by injecting a simple feedforward signal obtained from input and output voltages to the output voltage feedback control is introduced. The converter topology is based on the Taipei rectifier introduced in [14] and further expanded into three-level [15] and single-stage [16] structures. Since low THD is achieved without additional high bandwidth active current shaping control, the proposed topology is suitable for modern aviation applications that require line frequency up to 800 Hz. The evaluation was performed on a 320 W prototype designed to operate from 94-134 V line input and deliver 220 V dc output. The prototype achieves 2.3% THD at full load over the line frequency range from 360 Hz to 800 Hz and meets the required harmonic limits specified by the DO-160 standard.

II. TWO-SWITCH ZVS PFC DCM BOOST RECTIFIER

Figure 1 shows the proposed two-switch ZVS PFC DCM boost rectifier. The input of the rectifier consists of two boost inductors L1 and L2 coupled to input ac source VAC and two capacitors C1 and C2. The main purpose of adding split input capacitors C1 and C2 is to create common point N that has the medium potential of ac input source VAC. As a result, voltages VAN and VBN across capacitors C1 and C2 are substantially equal to one half of input voltage VAC and have opposite polarities. Common point N between capacitors C1 and C2 is connected to the mid-point between switches S1 and S2 and also to the mid-point of split output capacitors C01 and C02. As a result, the potential of the mid-point of output capacitors C01 and C02 as well as the mid-point of switches does not experience step changes with high dV/dt, which makes it possible for the rectifier to operate with low common-mode EMI noise. Switches S1 and S2 are controlled by two complementary gate

![Fig. 1. Proposed two-switch ZVS PFC DCM boost rectifier.](image-url)
signals with 50% duty cycle and a small dead time necessary to achieve ZVS of the switches.

As shown in Fig. 1, because the mid-point between switches S1 and S2 is directly connected to common point N and bridge diodes D1-D4 are located between the switches and phase voltages \( V_{AN} \) and \( V_{BN} \) across capacitors \( C_1 \) and \( C_2 \), bridge diodes D1-D4 only allow the phase voltage with positive potential to deliver current through switch S1 when it is turned on. Similarly, the phase voltage with negative potential delivers current through switch S2 when it is turned on. Therefore, during the time when switch S1 is on, the boost inductor connected to the positive phase voltage stores energy and carries positive current whereas, during the time when switch S2 is on, the other boost inductor connected to the negative phase voltage stores energy and carries negative current. During the time when switch S1 is off, the stored energy in the boost inductor connected to the positive phase voltage is delivered to flying capacitor \( C_R \) whereas, during the time when switch S2 is off, the stored energy in the boost inductor connected to the negative phase voltage is delivered to flying capacitor \( C_R \). Because the voltage of each terminal of flying capacitor \( C_R \) changes with high \( dV/dt \) at every switching cycle, coupled inductor \( L_C \) is connected between output capacitors \( C_{O1} \) and \( C_{O2} \) and flying capacitor \( C_R \) to isolate the common-mode noise sources to a small area.

III. ANALYSIS OF OPERATION

To simplify the analysis of operation, it is assumed that ripple voltages of the input and output filter capacitors shown in Fig. 1 are negligible such that the voltage across the input and output filter capacitors can be represented by constant-voltage sources \( V_{AN}, V_{BN}, V_{O1}, \) and \( V_{O2} \) as shown in Fig. 2. Also, it is assumed that in the on state, semiconductors exhibit zero resistance, i.e., they are short circuits. However, the output capacitances of the switches are not neglected in this analysis. Coupled inductor \( L_C \) in Fig. 1 is modeled as a two-winding ideal transformer with magnetizing inductance \( L_M \) and leakage inductances \( L_{K1} \) and \( L_{K2} \). Finally, since the average voltage across capacitor \( C_R \) is equal to output voltage \( V_O = V_{O1} + V_{O2} \), capacitor \( C_R \) is modeled as a constant voltage source. The reference directions of voltages and currents in the circuit diagram of the simplified rectifier shown in Fig. 2 correspond to the 180-degree segment of a line cycle when \( V_{AC} \neq 0, V_{AN} \neq 0, \) and \( V_{BN} \neq 0 \).

To further facilitate the explanation of the operation, Fig. 3 shows topological stages of the circuit in Fig. 2 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms.

As can be seen from the gate-drive timing diagrams for switches S1 and S2 in Fig. 4, both switches operate with 50% duty cycle in an alternative fashion with short dead time between turn-off of switch S1 and turn-on of switch S2 or vice versa. Because of this gating strategy, both switches can achieve ZVS. To maintain ZVS with 50% duty cycle for a varying input voltage and/or output load, the proposed rectifier must employ a variable switching frequency control. The minimum frequency is determined at full load and the minimum input voltage while the maximum frequency is determined at light load and the maximum input voltage. The rectifier operates in PWM mode or burst mode at no load or at very light load, to avoid unnecessarily high frequency operation.

As shown in Fig. 3(a) and Fig. 4, when switch S1 is on, inductor current \( i_{L1} \) flows through switch S1. The slope of inductor current \( i_{L1} \) is equal to \( V_{AN}/L_1 \). The peak of the inductor current is approximately

\[
I_{L1(peak)} = \frac{V_{AN}}{L_1} \times \frac{T_S}{2}
\]

where \( V_{AN} \) is the phase voltage across input capacitor \( C_1 \) and \( T_S \) is the switching period. Because the dead time between turn-off of switch S1 and turn-on of switch S2 is very small in comparison with switching period \( T_S \), the effect of the dead time is neglected in Eq. (1). During the period between \( T_0 \) and \( T_1 \), current \( i_{O1} \) decreases by the rate as \(-V_{O1}/(2L_{M}+L_{KK1})\) while current \( i_{O2} \) increases by the rate as \((V_{CR}+V_{O2})/(2L_{M}+L_{KK2})\). Magnetizing current \( i_{O3} \) is the difference between currents \( i_{O1} \) and \( i_{O2} \). It should be noted that the inductance value of coupled inductor \( L_M \) is designed to be sufficiently large such that the ripple current of the coupled inductor doesn't significantly affect rectifier operation. As shown in Fig. 1, the two windings of inductor \( L_M \) are coupled in such a way as to cancel the magnetic fluxes from the differential current of the two windings so that the large magnetizing inductance can be obtained by a small gap in the core without saturation. Since the effect of currents \( i_{O1} \) and \( i_{O2} \) is negligible, they are no longer discussed, although they are shown in topological stages in Fig. 3.

At \( t = T_1 \), when switch S1 is turned off, inductor current \( i_{L1} \) starts charging the output capacitance of switch S1, as shown in Fig. 3(b). Since switches S1 and S2 are clamped to capacitor voltage \( V_{CR} \), the output capacitance of switch S2 discharges at the same rate as the charging rate of the output capacitance of switch S1. This period ends when the output capacitance of switch S2 is fully discharged and the anti-parallel body diode of switch S2 starts to conduct at \( t = T_2 \), as shown in Fig. 3(c) and Fig. 4. Because the body diode of switch S2 is forward biased, inductor current \( i_{L2} \) begins to increase linearly. At \( t = T_3 \), switch S2 is turned on with ZVS and inductor current \( i_{L2} \) is commutated from the antiparallel diode of switch S2 to the switch, as illustrated in Fig. 3(d). This period ends when inductor current \( i_{L1} \) decreases to zero at \( t = T_4 \). To maintain DCM operation, the time period between \( T_3 \) and \( T_4 \) must be less than one-half of switching period \( T_S \) which means that the rising slope of inductor current \( i_{L1} \) should be smaller than its falling slope. As a result, minimum voltage \( V_{CR}\text{(MIN)} \) across capacitor \( C_R \), which is equal to minimum output voltage \( V_{O}\text{(MIN)} \), should be
\[ V_{\text{CR(MIN)}} \geq 2 \times V_{\text{AN(PK)}} = \sqrt{2} \times V_{\text{AC,rms}} \] (2)

where \( V_{\text{AN(PK)}} \) is the peak phase voltage.

It also should be noted that because inductor current \( i_{L2} \) flows in the opposite direction from inductor current \( i_{L1} \) during the time period between \( t = T_2 \) and \( t = T_4 \), the average current through switch \( S_2 \) is reduced so that the switches in the proposed rectifier exhibit reduced power losses.

During the period between \( t = T_4 \) and \( t = T_5 \), inductor current \( i_{L2} \) continues to flow through switch \( S_2 \), as illustrated in Fig. 3(e). As shown in Fig. 4, the slope of inductor current \( i_{L2} \) during this period is equal to \( V_{\text{BN}}/L_2 \). The peak of the inductor current at the moment when switch \( S_2 \) turns off at \( t = T_5 \) is approximately

\[ I_{L2}^{(\text{PK})} = \frac{V_{\text{BN}} L_1}{T_S} \times T_{S_2} \] (3)

As can be seen in Eqs. (1) and (3), the peak of each inductor current is proportional to its corresponding input voltage.

After switch \( S_2 \) is turned off at \( t = T_5 \), inductor current \( i_{L2} \) starts to simultaneously charge the output capacitance of switch \( S_2 \) and discharge the output capacitance of switch \( S_1 \), as shown in Fig. 3(f). This period ends at \( t = T_6 \) when the output capacitance of switch \( S_1 \) is fully discharged and its anti-parallel diode starts conducting, as shown in Fig. 3(g) and Fig. 4. After \( t = T_6 \), switch \( S_1 \) can be turned on with ZVS. In Fig. 4, switch \( S_1 \) is turned on at \( t = T_7 \). As shown in Fig. 3(h), once switch \( S_1 \)

Fig. 3 Topological states of proposed rectifier when \( V_{\text{AC}} > 0 \).
where L is the inductance of a boost inductor assuming boost inductors L1 and L2 have an identical value, and ω is the angular frequency of the line voltage. To achieve PFC, switching period $T_s$ should be proportional to $2V_{cr} - \sqrt{2}V_{Ac \text{rms}}\sin\theta$, i.e.,

$$T_s(t) = K(2V_{cr} - \sqrt{2}V_{Ac \text{rms}}\sin\theta) \quad (5)$$

where $K$ is a constant. With the proposed control method, averaged inductor current $\langle I_{L-\text{AVG}} \rangle_{T_S}$ of each boost inductor becomes

$$\langle I_{L-\text{AVG}} \rangle_{T_S} = \frac{V_{cr} \cdot K}{8L} \left(\sqrt{2}V_{Ac \text{rms}}\sin\theta\right) \quad (6)$$

Since voltage $V_{cr}$ and inductance L are also constant, the averaged inductor current that is equal to the input current is proportional to the input voltage. Figure 5 shows the simplified control block diagram that depicts the injection of the simple feedforward signal obtained from input and output voltages to the output voltage feedback control. As shown in the non-linear compensator block in Fig. 5, the sensed AC input voltage is rectified and scaled to be subtracted from the scaled output voltage, which creates the non-linear term of Eq. (5). The result of the non-linear compensator is multiplied with signal G of the output voltage feedback compensator. Voltage controlled oscillator VCO generates gate signals that are alternate pulses with approximately 50% duty cycle and switching period $T_s$ for switches $S_1$ and $S_2$ as depicted in Fig. 4. Since switching period $T_s$ is proportional to the multiplier output signal with the constant VCO gain, the condition derived at Eq. (5) is met and the proposed rectifier automatically achieves PFC without active current shaping control. It should be noted that $K$ in Eq. (5) is equal to the multiplication of $k$, $G$, and VCO gain shown in Fig. 5.

IV. DESIGN CONSIDERATIONS

Design guidelines and performance evaluation of the proposed rectifier for aviation applications with the following key specifications are presented:

- Single-phase ac input voltage $V_{AC}$: 94 – 134 Vrms
- Line frequency range: 360 Hz – 800 Hz
- THD: meets the DO-160 standard (THD less than 10% with limit on each current harmonic as shown in Fig. 9)
- PF: ≥ 0.98
- Efficiency: ≥ 95% from 30% to 100% load at nominal input line voltage
- Output voltage $V_o$: 220 V
- Maximum output power $P_{MAX}$: 320 W

A. Design of Boost Inductor

For the design of the boost inductor with 25% margin, the maximum value of the average boost inductor current over a switching period $\langle I_{L-\text{AVG}} \rangle_{T_S}$ is calculated as

$$\langle I_{L-\text{AVG}} \rangle_{T_S} = I_{L-\text{AVG}}^{\text{max}} = \sqrt{2} \cdot \frac{P_{MAX}}{V_{AC \text{rms}} \cdot 1.25} = 6.02 \text{ A.} \quad (7)$$

To achieve the desired power density, the minimum switching frequency $f_{SW}$ at the maximum value of peak line

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**Fig. 4.** Key waveforms of proposed rectifier when $V_{AN} > 0$ and $V_{BN} < 0$.

**Fig. 5.** Simplified control block diagram showing feedback and feedforward control.
current $I_{\text{AC(peak)}}$ is set to 40 kHz. Substituting Eq. (7) in Eq. (4), the value of boost inductor L can be calculated using $V_{\text{CR}} = 220\, \text{V}$, $T_S = 1/f_{\text{SW}} = 25 \, \mu\text{s}$ as

$$L = \frac{V_{\text{CR}} T_S}{8 \cdot I_{\text{AC(peak)}}^\text{max}} \left( \frac{\sqrt{2} V_{\text{AC rms}}}{2 V_{\text{CR}} - \sqrt{2} V_{\text{AC rms}}} \right) \approx 50 \, \mu\text{H}. \quad (8)$$

To obtain the desired inductance of boost inductors $L_1$ and $L_2$ of approximately 50 $\mu\text{H}$, each inductor was built using a pair of ferrite cores (PQ-26/20, 3C95) with 18 turns of Litz wire (200 strands / AWG #38).

**B. Switch Selection**

The voltage stress of switches $S_1$ and $S_2$ is approximately equal to bus voltage $V_{\text{CR}} = 220 \, \text{V}$. Due to ZVS operation and practically no overshoot in the voltage across switches $S_1$ and $S_2$, IPP220N25NFD MOSFET ($V_{\text{DS}} = 250 \, \text{V}$, $R_{\text{DS}} = 22 \, \text{m}\Omega$, $C_{\text{OSS}} = 299 \, \text{pF}$, $Q_{\text{RR}} = 623 \, \text{nC}$) was used in this prototype.

**C. Rectifier Diode Selection**

As input diodes $D_1$-$D_4$ block the same voltage and conduct the same current as the switches, the STTH803 rectifier was selected ($V_{\text{Frm}} = 300 \, \text{V}$, $I_A = 8 \, \text{A}$, $t_{\text{rr}} = 625 \, \text{ns}$). The crucial part of the diode selection is the tradeoff between diode forward voltage drop $V_F$ and output capacitance $C_{\text{OSS}}$. Diode voltage drop $V_F$ reduces power conversion efficiency while diode output capacitance $C_{\text{OSS}}$ resonates with the boost inductor since the boost inductor current is discontinuous. Due to the variable-frequency operation and time-varying input voltage $V_{\text{AC}}$, the number of resonant cycles is not constant, which might lead to additional line current harmonics.

**D. Capacitor Selection**

Input capacitors $C_1$ and $C_2$ provide filtering of the switching frequency ripple and facilitate phase-decoupling. The current rating of the capacitors is determined by the peak boost inductor current that occurs at full load and low line. A low-ESR film capacitor (1 $\mu\text{F}$, 305 $V_{\text{AC}}$) was selected. The input capacitor value is limited by the power factor requirement since the capacitive current leads the line voltage. The peak current of $C_0$ capacitor is equal to the boost inductor current peak and the current drawn from the bulk capacitor. A film capacitor (4.4 $\mu\text{F}$, 250 $\text{V}$) was used for flying capacitor $C_{\text{f}}$. The output bulk capacitance was an aluminum capacitor (2.4 $\text{mF}$, 320 $\text{V}$).

**V. CONTROL STRUCTURE**

The control of the prototype rectifier was implemented with TMS320F28027 DSP from TI. Since the rectifier naturally achieves high power factor without an active current shaping control, the control consists only of a low-bandwidth feedback loop that varies the switching frequency to regulate the output voltage. Switches $S_1$ and $S_2$ operate with variable frequency, alternate switching pulses with 50% duty cycle. Generally, a converter with variable frequency control employs burst-mode operation at light load, in which the switching pulses are enabled and disabled at regular intervals to regulate the output voltage. However, the burst mode operation significantly increases the magnitude of the output voltage ripple. To reduce the peak-ripple of the output voltage at light load, pulse width modulation (PWM) is employed instead of a burst mode operation. Switches $S_1$ and $S_2$ operate with constant-frequency, 180 degree phase shifted, variable-duty-cycle pulses. The PWM frequency is selected as 20 kHz to avoid audible noise and to limit converter losses since the switches lose ZVS turn-on in the PWM mode.

Figure 6 shows the simplified block diagram of the proposed digital control implementation. As can be seen in Fig. 6, for both the variable frequency control and the PWM control, the switching period and the switching pulse on-time are determined by output $V_{\text{EA}}$ of voltage controller $G_{\text{C}}$. Voltage controller $G_{\text{C}}$ processes the error between sensed and sampled output voltage $V_{\text{O(SEN)}}$ and reference $V_{\text{O(REF)}}$. It can be seen from Fig. 6 that sensed and sampled output voltage $V_{\text{O(SEN)}}$ is obtained from output voltage $V_{\text{O}}$. Output voltage $V_{\text{O}}$ is scaled and passed through an anti-aliasing filter $G_{\text{AF}}$ (5 with corner frequency $f_{\text{AF}} = 16 \, \text{kHz}$. This sensed and filtered signal is then converted to the digital domain with the 12-bit analog-to-digital converter (ADC), which has a full-scale range (FSR) of 3.3 $\text{V}$. In the DSP, the signal at the output of the ADC is multiplied with unscaling gain $K_{\text{s}}$ to obtain sensed and sampled output voltage $V_{\text{O(SEN)}}$ so that the value of $V_{\text{O(SEN)}}$ is equal to the value of output voltage $V_{\text{O}}$.

In the implementation in Fig. 6, the drive signals of switches $S_1$ and $S_2$ are generated by digital pulse width modulator (DPWM) with an up-down counter as digital carrier ramp. The up-down counter is generated by counting the clock period $T_{\text{CLK}}$. Since carrier ramp period $T_{\text{S}} = 2 \cdot N_{\text{CAR}} \cdot T_{\text{CLK}}$, where $N_{\text{CAR}}$ is the number of clock periods, carrier ramp period $T_{\text{S}}$ is proportional to $N_{\text{CAR}}$. It should be noted that in the variable frequency control mode, carrier ramp peak $N_{\text{CAR}}$ is determined by the product of the output of voltage controller $V_{\text{EA}}$ and normalized feedforward injection signal $V_{\text{FI}}$. In fact, in the variable frequency mode, the output of voltage controller $V_{\text{EA}}$ is equal to the output of the “Calculation of Switching Period” block $N_{\text{CAR AVG}}$ so that $V_{\text{EA(MAX)}} = N_{\text{MAX}}$ and $V_{\text{TH EA}} = N_{\text{MIN}}$.

Normalized feedforward injection signal $V_{\text{FI}}$ is calculated as

$$V_{\text{FI}} = \frac{2 \cdot V_{\text{O(SEN)}} - |V_{\text{AC(SEN)}}|}{K_{\text{N}}} \quad (9)$$

where $V_{\text{AC(SEN)}}$ is the sensed and sampled ac input voltage whose value is equal to the ac input voltage $V_{\text{AC}}$ and $K_{\text{N}}$ is the normalization factor. The value of normalization factor $K_{\text{N}}$ is calculated such that the average value of normalized feedforward injection signal $V_{\text{FI}}$ over a line cycle is 1, as

$$K_{\text{N}} = 2 \cdot V_{\text{O(SEN)}} - \frac{2}{\pi} V_{\text{AC(SEN)}}^\text{peak} \quad (10)$$

where $V_{\text{AC(SEN)}}^\text{peak}$ is the peak value of the sensed and sampled ac input voltage. By using a normalized feedforward injection signal, the steady-state value of the output of voltage controller $V_{\text{EA}}$ with and without the feedforward injection will be approximately the same. In addition, with the normalized feedforward injection, the gain of the output voltage control loop will not be affected, and therefore, the dynamic response of the output voltage control loop will not be affected. Figure 7 shows the experimental waveforms of rectified ac input voltage $|V_{\text{AC}}|$ and the normalized feedforward injection signal at line
frequency $f_L = 800$ Hz, $V_O = 220$ V, and $V_{AC} = 94$ V\text{RMS}. It is important to note that the control frequency of 50 kHz is selected to attain sufficient number of calculations in a line cycle to achieve low THD at maximum line frequency $f_{L(MAX)} = 800$ Hz.

Further in Fig. 6, it should be noted that the maximum value of $N_{CAR}$, i.e., $N_{MAX} = 750$ which corresponds to minimum switching frequency $f_{SW\ MIN} = 40$ kHz and the minimum value of $N_{CAR}$, i.e., $N_{MIN} = 120$ which corresponds to maximum switching frequency $f_{SW\ MAX} = 250$ kHz. The selection of the maximum switching frequency is to limit the switch turn off losses and magnetic losses of the boost inductor.

The output voltage controller is implemented with a PI compensator. To achieve reasonably low bandwidth of the output voltage feedback loop, the proportional gain of PI compensator $K_P = 0.78$ and the integral gain $K_I = 195$ s$^{-1}$ were selected using SIMPLIS$^{TM}$ simulations. Since the control frequency in the prototype circuit is $f_{CTRL} = 50$ kHz, the $z$-domain transfer function of output voltage controller $G_C(z)$ obtained by bilinear (Tustin’s) transformation is

$$G_C(z) = 0.78 + 0.0039 \frac{z^{-1}}{1 - z^{-1}}$$ (11)

At light loads, when voltage controller output $V_{EA}$ reaches threshold value $V_{TH\ EA}$, which corresponds to the maximum switching frequency of 250 kHz, the controller changes its control mode to the PWM mode. In the PWM mode, the variable duty-cycle is achieved by varying DPWM carrier frequency $f_{SW\ MAX}$ to 250 kHz. The selection of the PWM carrier frequency is to limit the switch turn off losses and magnetic losses of the boost inductor.

The drive signal of switch $S_1$ is obtained by comparing the carrier ramp with comparison level $N_{CAR} - N_{ON}$ whereas the drive signal of switch $S_2$ is obtained by directly comparing the carrier ramp with $N_{ON}$. In the variable frequency mode, switches $S_1$ and $S_2$ operate in an alternate fashion with 50% duty cycle and therefore, $N_{ON} = N_{CAR}/2$. 

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Fig 6. Simplified block diagram of digital control implementation.

Fig 7. Experimental waveforms of rectified ac input voltage $|V_{AC}|$ and the normalized feedforward injection signal at line frequency $f_L = 800$ Hz, $V_O = 220$ V, and $V_{AC} = 94$ V\text{RMS}. 

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VI. EXPERIMENTAL RESULTS

The performance of the proposed converter shown in Fig. 1 was evaluated on a 320-W prototype circuit designed according to the procedure and key specifications given in Section IV.

Figures 8 (a) and (b) show the measured waveforms of the ac input voltage and input current at 360 Hz and 800 Hz line frequencies. The measured THDs were 2.28% at 360 Hz and 2.36% at 800 Hz. Moreover, the measured power factor was 0.997 at 360 Hz and 0.984 at 800 Hz.

Figure 9 shows the comparisons between each harmonic limit specified by DO-160 and measured line current harmonic content when prototype rectifier delivers full load at 360 Hz and 800 Hz line frequencies. Each measured harmonic is well below its required limit.

![Graph of measured power factor over load at V_{AC} = 115 V_{RMS}, V_o = 220 V, and f_L = 360 Hz.](image)

![Graph of measured THD over load at V_{AC} = 115 V_{RMS}, V_o = 220 V, and f_L = 360 Hz.](image)
Figure 10 shows the measured waveforms of gate and drain voltages of switch $S_1$ and the current waveform of boost inductor $L_1$ at 800 Hz line frequency and full load. The measured waveforms in Fig. 10 are in good agreement with the ideal waveforms shown in Fig. 4. It should be noted that switch $S_1$ turns on when its drain voltage is substantially zero. Dead-time duration is 400 ns. Due to soft switching and small inductive loop, there is no voltage overshoot across the switch.

Power factor as a function of load at line frequency of 360 Hz is shown in Fig. 11. Measured THD across the entire power range is shown in Fig. 12. It should be noted that THD increases with reduced load level because of more pronounced non-ideal circuit properties such as switch output capacitance $C_{OSS}$, diode forward voltage drop $V_F$, etc. Moreover, lower power levels occur at higher switching frequencies, where the 400 ns dead-time forms a more significant portion of the entire switching period.

Power conversion efficiency as a function of load is shown in Fig. 13. Measured efficiency of the prototype circuit was approximately 95.2% at full load and nominal line voltage of $V_{AC}$ of 115 V_{RMS}. Calculated loss distribution of the converter at nominal line voltage and full load is shown in Fig. 14. The four bridge diodes contribute to nearly half of all losses, which is expected since the diode voltage drop forms a significant fraction of the input voltage. Switch conduction and turn-off losses contribute only 0.7%. Finally, the loss of the common-mode choke contributes nearly 0.8% loss, which could be easily reduced by using a higher-gauge wire.

VII. CONCLUSIONS

A new, two-switch, PFC, DCM boost rectifier that features ZVS and can achieve less than 5% input-current THD is proposed and evaluated. Since low THD is achieved without high bandwidth active current shaping control, the proposed topology is suitable for modern aviation applications that require line frequency up to 800 Hz. The prototype achieves 2.3% THD at full load of 320 W and nominal line input voltage 115 V over the line frequency range from 360 Hz to 800 Hz and meets the required harmonic limits specified by the DO-160 standard.

REFERENCES

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