Line Current Distortions of DCM/CCM Boundary Boost PFC Converter

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Abstract - A systematic analysis of line current distortions of the DCM/CCM boundary boost PFC converter due to valley switching and switching-frequency limitation is provided. Closed form expressions for the line current are derived. It is shown that if the switching frequency is limited and valley switching is not maintained, the line current is more distorted with voltage mode control than with current mode control. The effects of line current distortions are demonstrated with both simulation and experimental results.

I. Introduction

In low-power, off-line power supplies, a boost converter operating at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) is a popular topology for implementing the front-end converter with active power-factor correction (PFC) [1]-[6]. The major benefit of the DCM/CCM boundary boost converter, compared to the CCM boost converter, is that the reverse-recovery losses related to the boost diode are eliminated. In addition, turn-on with zero-voltage switching (ZVS) or near ZVS of the boost switch, also called valley switching, can be easily achieved. A major drawback of the DCM/CCM boost converter is that its switching frequency, which changes as a function of line and load, varies over a wide range leading to excessive turn-off switching loss of the main switch, as well as excessive core and winding loss of the inductor. This becomes a significant problem at light loads, where most consumer products are required to meet the Energy Star standards [7] and/or the 80-plus program [8]. Generally, switching losses can be controlled by limiting the switching frequency. However, by limiting the switching frequency, the line current becomes distorted resulting in decreased power factor (PF) and increased total harmonic distortion (THD). In addition, ZVS of the main switch can be lost, which degrades the efficiency and leads to excessive electromagnetic-interferance (EMI) noise and, therefore, additional input filtration is needed.

This paper presents a systematic analysis of the line current distortions of the DCM/CCM boundary boost PFC converter due to valley switching and switching-frequency limitation. The effects of line current distortions are demonstrated with both simulation and experimental results.

II. Analysis of Line Current Distortions

When the boost converter, shown in Fig. 1, operates at the DCM/CCM boundary with a constant on-time T_{on} of boost switch S_B, the line current follows the line voltage. In fact, line current i_{in} is equal to the inductor current i_{LB} averaged over a switching period T_{sw}, i.e.,

$$i_{in} = \langle i_{LB} \rangle_{T_{sw}} = \frac{v_{in} T_{on}}{2L_B} \tag{1}$$

where $v_{in} = \sqrt{2}\, V_{in,rms} \sin(\omega_L t)$. On-time T_{on} is determined as

$$T_{on} = \frac{2L_B P_o}{\eta V_{in,rms}^2} \quad , \tag{2}$$

where, $\eta = P_o / P_{in}$.

However, operating at the DCM/CCM boundary, switch S_B turns on with hard switching, as shown in Fig. 2(a), resulting in elevated turn-on losses. The turn-on losses can be significantly reduced or even completely eliminated if the turn-on instant of switch S_B is delayed until its drain-source voltage v_{DS} resonates down to a valley (when $v_{in} > V_o/2$) or to zero (when $v_{in} < V_o/2$), as shown in Fig. 2(b). This additional delay T_d, which is due to the parasitic capacitances (e.g., C_{oss}) resonating with boost inductor L_B, increases the turn-off time of the switch and introduces line current distortions, i.e.

$$i_{in} = \frac{v_{in} T_{on}}{2L_B} \cdot \frac{1}{1 + \frac{T_d}{T_{on}} \cdot \left(1 - \frac{v_{in}}{V_o}\right)} \quad . \tag{3}$$

It follows from (3) that delay time T_d related line current distortions are more pronounced around the zero crossing of

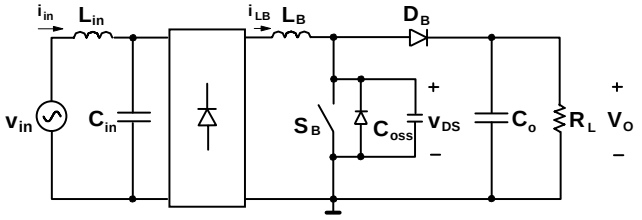

Fig. 1 Simplified circuit diagram of PFC boost converter

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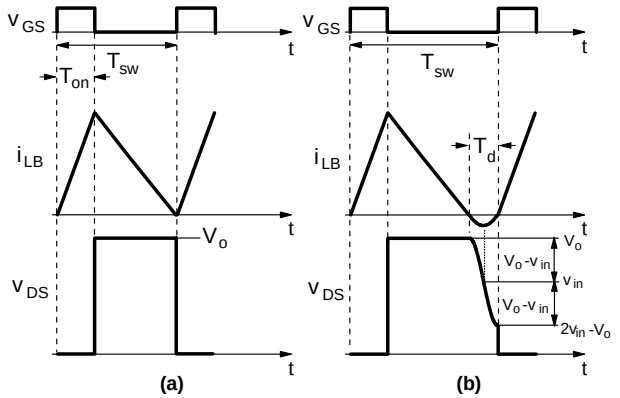

Fig. 2 Key switching waveforms of DCM/CCM boundary operation (a) without delay (b) with delay T_d

the line voltage v_{in} and at light load where T_{on} is minimal. Normalized line current waveforms as a function of the normalized delay time ($T_{d,norm}$=T_d/T_{on}) at 115-V_{rms} and 230-V_{rms} line voltages (nominal low-line and high-line voltages), at 385-V output voltage, are presented in Figs. 3 and 4, respectively.

The line current distortion can be quantitatively expressed by the power factor, defined as

$$PF = \frac{P_{in}}{V_{in,rms} \cdot I_{in,rms}} \quad . \tag{4}$$

Power factor values corresponding to the line current waveforms in Figs. 3 and 4 are shown in Table I. It can be concluded from Table I that delay time T_d related line current distortions are practically negligible.

When the boost converter operates at the DCM/CCM boundary with constant on-time T_{on}, the switching frequency changes as

$$f_{sw} = \frac{1}{T_{on}} \cdot \left(1 - \frac{v_{in}}{V_o}\right) \quad . \tag{5}$$

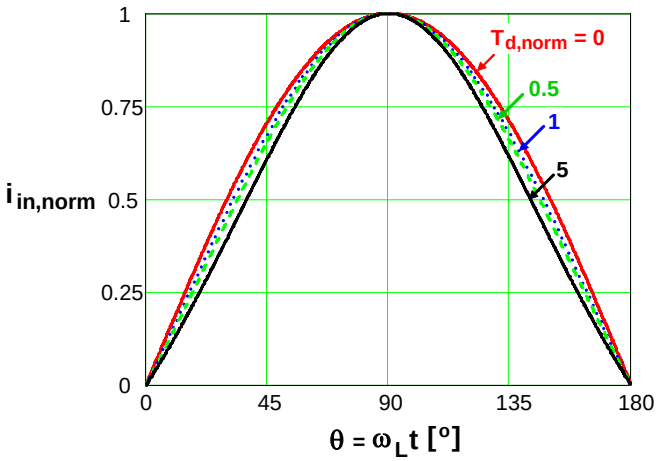

Fig. 3 Normalized line current waveforms as a function of normalized delay time $T_{d,norm}$ at 115-V_{rms} line voltage and 385-V output voltage.

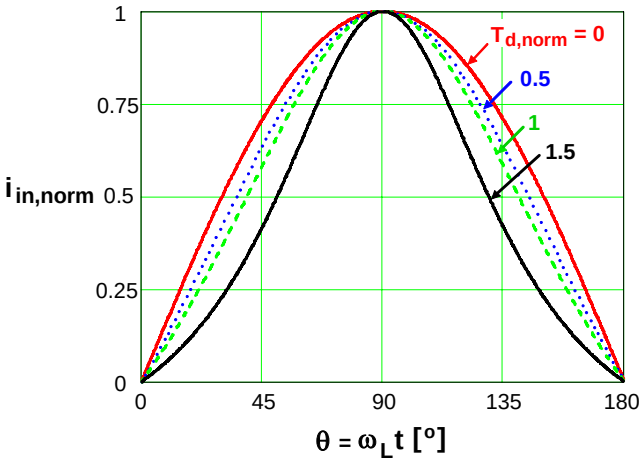

Fig. 4 Normalized line current waveforms as a function of normalized delay time $T_{d,norm}$ at 230-V_{rms} line voltage and 385-V output voltage.

Using (2), the switching frequency is determined as

$$f_{sw} = \eta \frac{V_{in,rms}^2}{2L_B P_o} \cdot \left(1 - \frac{v_{in}}{V_o}\right) \quad . \tag{6}$$

It follows from (6) that, for example, at 230-V_{rms} line voltage, 385-V output voltage, and a constant load, the switching frequency over a half-line cycle varies more than six times, whereas a ten times change in load will lead to approximately a ten times change in the switching frequency. At light loads, the switching frequency can become very high and, therefore, it is desirable to limit it in order to decrease the switching losses, which include the boost switch turn-off and, eventually, turn-on losses, gate drive loss, and the inductor core and copper loss.

When operating with a switching frequency limit, generally, the boost switch can operate with or without valley switching. If operating with valley switching, the boost switch can maintain valley switching or it can lose valley switching after the onset of the switching frequency limit, depending on the employed control method.

If a switching frequency limit is implemented and the boost switch always operates without valley switching, the line current is determined as

$$i_{in} = \begin{cases} \dfrac{v_{in} T_{on}}{2L_B} & \text{if} \quad \dfrac{v_{in}}{V_o} > 1 - T_{on} f_{sw,max} \\ \dfrac{v_{in} T_{on}}{2L_B} \cdot \dfrac{T_{on} f_{sw,\max}}{1 - \dfrac{v_{in}}{V_o}} & \text{if} \quad \dfrac{v_{in}}{V_o} \le 1 - T_{on} f_{sw,max} \end{cases} . \tag{7}$$

Normalized line current waveforms as a function of the normalized on time ($T_{on,norm}$=T_{on} $f_{sw,max}$) at 230-V_{rms} line voltage and 385-V output voltage are presented in Fig. 5. It

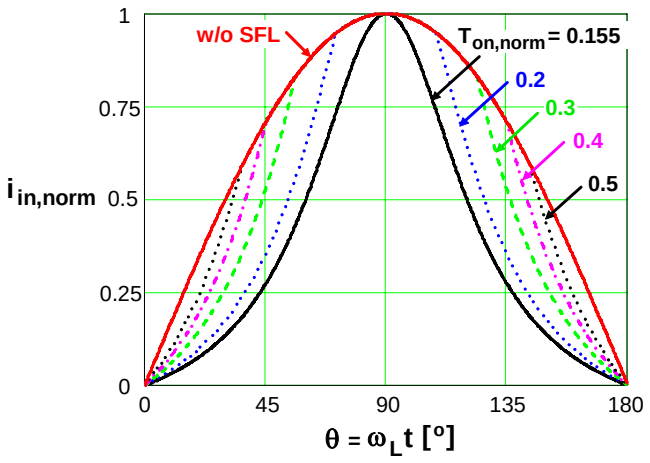

Fig. 5 Normalized line current waveforms for different switching frequency limits (SFLs) (i.e., as a function of normalized on time $T_{on,norm}$=T_{on} $f_{sw,max}$) at 230-V_{rms} line voltage and 385-V output voltage.

should be noted that the switching frequency is typically limited in the high line-voltage range.

Power factor values corresponding to the line current waveforms in Fig. 5 are shown in Table II. It can be seen in Table II that in the case where the switching frequency is limited in the entire half-line cycle, the power factor is limited to 0.9369.

The line current expression in (7) is obtained by neglecting the oscillation of the boost inductor current after the reset of the boost inductor. If the oscillation of the boost inductor current is also taken into consideration, it can be easily shown that the line current distortion depends on the control method used. When voltage mode control is used, the peak inductor current depends on the initial value of the inductor current during the resonant interval at the moment switch S_B is turned on because the on-time T_{on} is constant, as shown in Fig. 6(a). Therefore, the peak inductor current and, consequently, the average value of the inductor current can change abruptly between two consecutive switching cycles, resulting in significant line-current distortions. When current mode control is used, the peak inductor current is constant, and, instead, on-time T_{on} changes, but only slightly, resulting in approximately the same averaged value of the inductor current in two consecutive switching cycles, as shown in Fig. 6(b). Consequently, the line current is only slightly distorted. By reducing the amplitude of the resonant current, e.g., by selecting a switch with lower output capacitance, the line-current distortion can be further reduced. Although damping of the resonance is possible using an RCD snubber as

TABLE I
POWER FACTOR VS NORMALIZED DELAY TIME AT NOMINAL LOW-LINE AND HIGH-LINE VOLTAGES (V_o = 385 V)

$V_{in,rms}$ [V]	$T_{d,norm} = T_d/T_{on}$			
	0	0.5	1	5
115	1	0.99965	0.99914	0.99703
230	1	0.99829	0.99515	0.97419

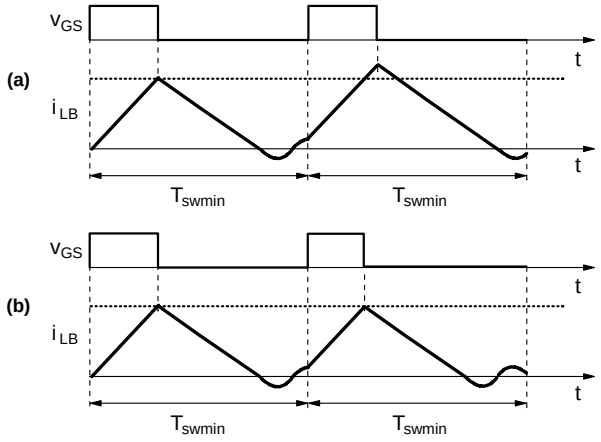

Fig. 6 Key switching waveforms of DCM/CCM boundary boost with switching frequency limit (a) voltage mode control (b) current mode control.

suggested in [9], the additional power loss due to the snubber is undesirable.

If a switching frequency limit is implemented and the boost switch operates with valley switching until the onset of the switching frequency limit, the line current is determined as

$$i_{in} = \begin{cases} \dfrac{v_{in}T_{on}}{2L_B} \cdot \dfrac{1}{1+\dfrac{T_d}{T_{on}} \cdot \left(1-\dfrac{v_{in}}{V_o}\right)} & \text{if} \quad \dfrac{v_{in}}{V_o} > 1 - A_1 \\ \dfrac{v_{in}T_{on}}{2L_B} \cdot \dfrac{T_{on} f_{sw,\max}}{1-\dfrac{v_{in}}{V_o}} & \text{if} \quad \dfrac{v_{in}}{V_o} \le 1 - A_1 \end{cases}, \quad (8)$$

where

$$A_1 = \frac{T_{on} f_{sw,max}}{1 - T_d f_{sw,max}} \quad . \quad (9)$$

If a switching frequency limit is implemented and valley switching is always maintained, additional distortions in the line current are introduced, as follows from Fig. 7. In fact, if the first valley in the present switching period occurs just after interval $T_{sw,min}$ = 1/$f_{sw,max}$, switch S_B turns on at the first valley; however, if the first valley in the next switching period occurs just before interval $T_{sw,min}$, the turn-on of switch S_B is delayed until the second valley (also called valley skipping), resulting in an abrupt change in the averaged inductor current and, therefore, in an abrupt change in the line current. The line current waveform is determined as

TABLE II
POWER FACTOR VS NORMALIZED ON TIME AT 230-V_{rms} NOMINAL HIGH-LINE VOLTAGE (V_o = 385 V)

$T_{on,norm} = T_{on}$ $f_{sw,max}$	≤ 0.155	0.2	0.3	0.4	0.5
PF	0.9369	0.9555	0.9828	0.9937	0.9979

$$i_{in} = \begin{cases} \dfrac{v_{in} T_{on}}{2L_B} \cdot \dfrac{1}{1 + \dfrac{T_d}{T_{on}} \cdot \left(1 - \dfrac{v_{in}}{V_o}\right)} & \text{if } \dfrac{v_{in}}{V_o} \geq 1 - A_1 \\ \dfrac{v_{in} T_{on}}{2L_B} \cdot \dfrac{1}{1 + k \cdot \dfrac{T_d}{T_{on}} \cdot \left(1 - \dfrac{v_{in}}{V_o}\right)} & \text{if } A_1 < 1 - \dfrac{v_{in}}{V_o} \leq A_k \end{cases} \quad (10)$$

where

$$A_k = \frac{T_{on} f_{sw,max}}{1 - k \cdot T_d f_{sw,max}}, \quad k = 3,5,7,\ldots \quad . \quad (11)$$

Normalized line current waveforms for a 130-W, universal-input, 385-V output DCM/CCM boundary boost PFC converter with $L_B = 230$ µH and with 250-kHz switching frequency limit are shown in Fig. 8 at 230-V_{rms} line voltage. The solid-line and dash-line waveforms are for the cases where the valley switching is lost and where it is maintained after the onset of the switching frequency limit, respectively. Key normalized parameters of the line current waveforms in Fig. 8 are $T_{on,norm} = T_{on} f_{sw,max} = 0.2825$ and $T_{d,norm} = T_d / T_{on} = 0.422$. The power factor for the line current with valley switching always maintained is only slightly lower than the power factor for the line current with valley switching lost after the onset of the switching frequency limit, as shown in Fig. 8.

The line current expression in (10) is obtained under the assumption that the valley skipping is monotonic. However, in a real circuit, in addition to the valley skipping, a jittering effect can be observed during a few switching cycles when the switching period is approximately equal to $T_{sw,min}$, where the turn-on of switch S_B randomly happens between two consecutive valleys. Besides the line current distortion, the valley jittering may also result in audible noise. This valley jittering and, consequently the audible noise, can be reduced by using a sophisticated valley counting (also called anti-jittering) algorithm [10].

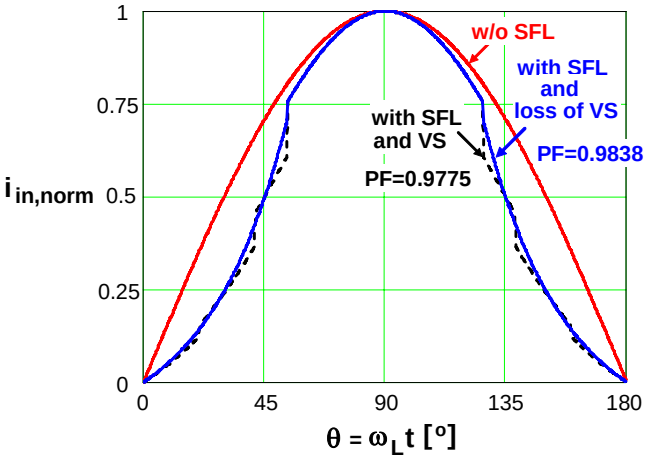

Fig. 8 Normalized line current waveforms for the case without switching frequency limit (SFL) (in red), and for the case with switching frequency limit where valley switching (VS) is lost (in blue) and where it is maintained (in black) after the onset of switching frequency limit.

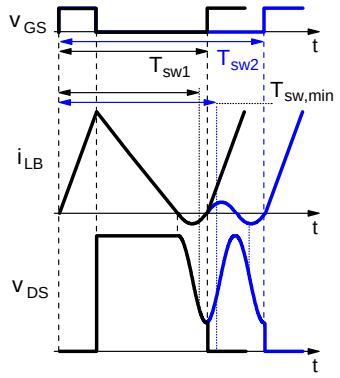

Fig. 7 Key switching waveforms of DCM/CCM boundary boost with switching frequency limit and valley switching.

III. Simulation Results

To further illustrate the effect of switching frequency limit and valley skipping on the line current waveform during the entire line cycle, SIMPLIS™ simulations were performed. Figure 9 shows the line current waveform (in red) of a 130-W, universal-input, 385-V output, DCM/CCM boundary boost PFC converter with $L_B = 230$ µH and with 250-kHz switching frequency limit, at 230-V_{rms} line voltage, operating with current mode control and valley switching. The switching frequency variation during the entire line cycle is also included in Fig. 9 (in red). It is shown in Fig. 9 that switching frequency f_{sw} is not firmly clamped to its limit due to valley skipping, i.e., due to the fact that the circuit must wait for the next resonant valley before turning on. It can be seen in Fig. 9 that a discontinuity occurs in the line current waveform whenever switching frequency f_{sw} reaches its 250-kHz limit. For comparison with the case without switching frequency limitation, the corresponding line current

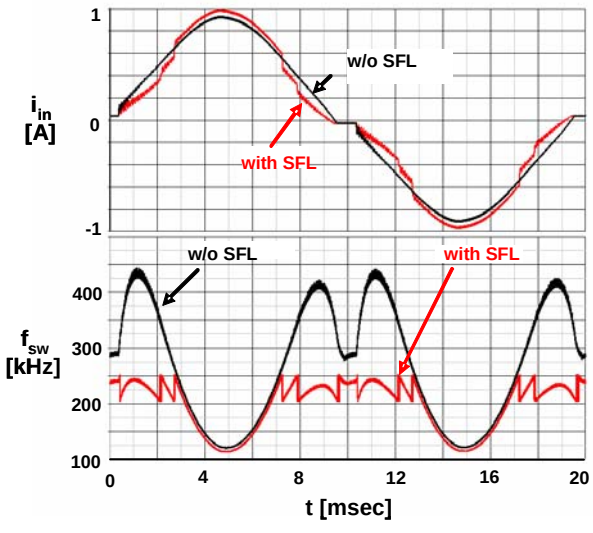

Fig. 9 Simulation of DCM/CCM boundary boost PFC with and without switching frequency limit (SFL);
- w/o SFL: PF=0.994, THD=0.9%, $f_{sw,avg}$=245 kHz
- with SFL: PF=0.9795, THD=4.4%, $f_{sw,avg}$=197 kHz

waveform and switching frequency variation are also presented in Fig. 9 (in black). It should be noted that in the case where the switching frequency is not limited by the control circuit, it is nevertheless limited by the effect of the filter capacitor at the output of the full-bridge rectifier, which prevents the rectified line voltage to decrease to zero.

It follows from Fig. 9 that the line current waveform with switching frequency limitation is more distorted than without switching frequency limitation. Calculated PF and THD values are also included in Fig. 9.

The benefit of limiting the switching frequency is reduced switching loss, both in the capacitive turn-on loss P_{Con} and gate drive loss P_G of switch S_B, as well as the core and copper loss of the inductor. Using simulation, drain-source voltage v_{DS} a moment prior to switch S_B turn-on (i.e., V_{Con}) can be sampled along with switching frequency f_{sw} and used to determine both turn-on loss P_{Con} and gate-drive loss P_G during a line period T_L, defined as

$$P_{Con} = \frac{1}{T_L}\int_0^{T_L} \frac{1}{2} f_{sw} C_{oss} V_{Con}^2 dt \quad , \tag{12}$$

and

$$P_G = V_{GG} Q_G \frac{1}{T_L}\int_0^{T_L} f_{sw} dt \quad , \tag{13}$$

respectively, where, V_{GG} is the gate-drive voltage and Q_G is the total gate charge. Simulated waveforms during a half-line cycle and calculation results are presented in Fig. 10 for three cases: without switching frequency limit with valley switching (in black); and switching frequency limit $f_{sw,max}$ = 250 kHz, with (in red) and without (in blue) valley switching. The simulation was performed at 230-V_{rms} line voltage and full load, i.e., 130 W (V_{GG}=15V, C_{oss}=100pF, and Q_G=60 nC). Although gate drive loss P_G is similar in all cases, capacitive turn-on loss P_{Con} is nearly three times higher when valley switching is lost. However, performing a similar simulation at 20% load (Fig. 11) shows that gate drive loss P_G nearly triples when the frequency is not limited, and capacitive turn-on loss P_{Con} nearly triples when valley switching is lost when operating with switching frequency limit. In addition to an increased loss, the effect of losing valley switching is also an increased conducted EMI, which may necessitate additional filtration, that further increases the loss.

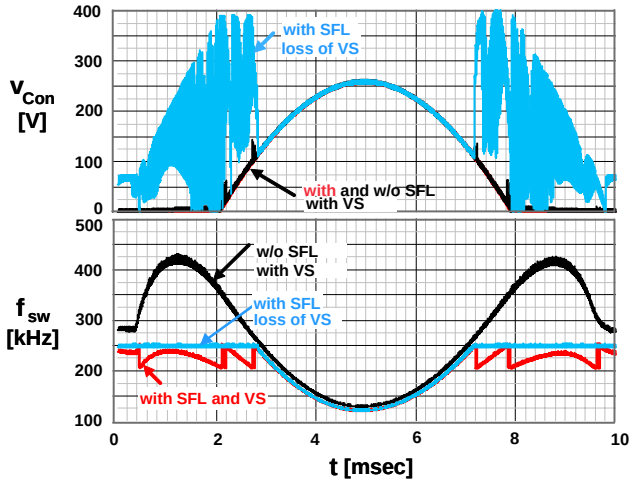

Fig. 10 Simulation of drain-source voltage just prior to switch S_B turn on (i.e., V_{Con}) and switching frequency f_{sw} with and without switching frequency limit (SFL) and valley switching (VS) at full load;
- w/o SFL and VS: $f_{sw,avg}$=245 kHz, P_{Con}=0.16 W, P_G=0.24 W
- with SFL and VS: $f_{sw,avg}$=197 kHz, P_{Con}=0.15 W, P_G=0.18 W
- with SFL and loss of VS: $f_{sw,avg}$=209 kHz, P_{Con}=0.41 W, P_G=0.19 W

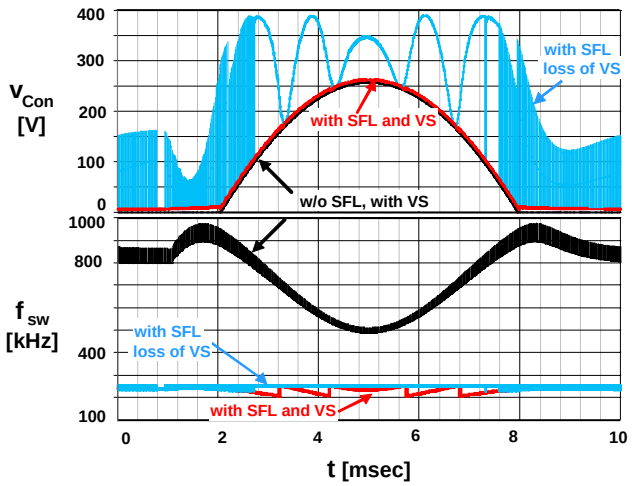

Fig. 11 Simulation of drain-source voltage just prior to switch S_B turn on (i.e., V_{Con}) and switching frequency f_{sw} with and without switching frequency limit (SFL) and valley switching (VS) at 20% load;
- w/o SFL and VS: $f_{sw,avg}$=728 kHz, P_{Con}=0.57 W, P_G=0.66 W
- with SFL and VS: $f_{sw,avg}$=230 kHz, P_{Con}=0.24 W, P_G=0.21 W
- with SFL and loss of VS: $f_{sw,avg}$=243 kHz, P_{Con}=0.74 W, P_G=0.22 W

IV. Experimental Results

Experimental waveforms presented in Fig. 12 illustrate the line current distortions when valley switching is not maintained and a maximum switching frequency limit is implemented with voltage-mode control. The experimental waveforms in Fig. 12 were obtained on a 150-W, universal-input, 385-V output DCM/CCM boundary boost PFC prototype circuit controlled by the NCP1601 voltage-mode controller IC from ON Semiconductor. The line voltage was 200-V_{rms}, the switching frequency limit was 133-kHz, and valley switching was lost after the onset of switching frequency limit. As shown in Fig. 12(a), the boost inductor current i_{LB} waveform and, consequently, the line current waveform, contains abrupt changes around the zero crossings of the line voltage. These non-monotonic distortions are due to the abrupt increase in the peak of the inductor current, as illustrated in Fig. 12(b), which is a result of the inductor current increasing from zero at the start of one switching cycle, and then increasing from a positive value at the start of the next switching cycle.

Experimental waveforms presented in Fig. 13 illustrate that there is minimal line current distortion when valley switching

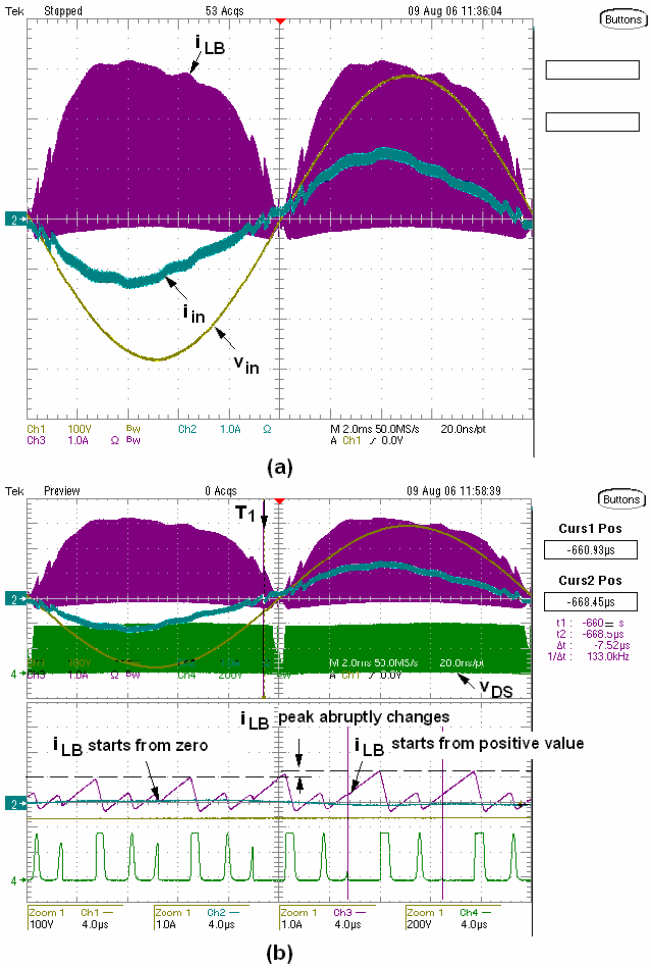

Fig. 12 Key experimental waveforms of 150-W/385-V, universal input DCM/CCM boundary boost PFC with voltage mode control, 133-kHz switching frequency limit, and loss of valley switching after the onset of switching frequency limit (a) during a line cycle (b) zoomed in around instant T_1.

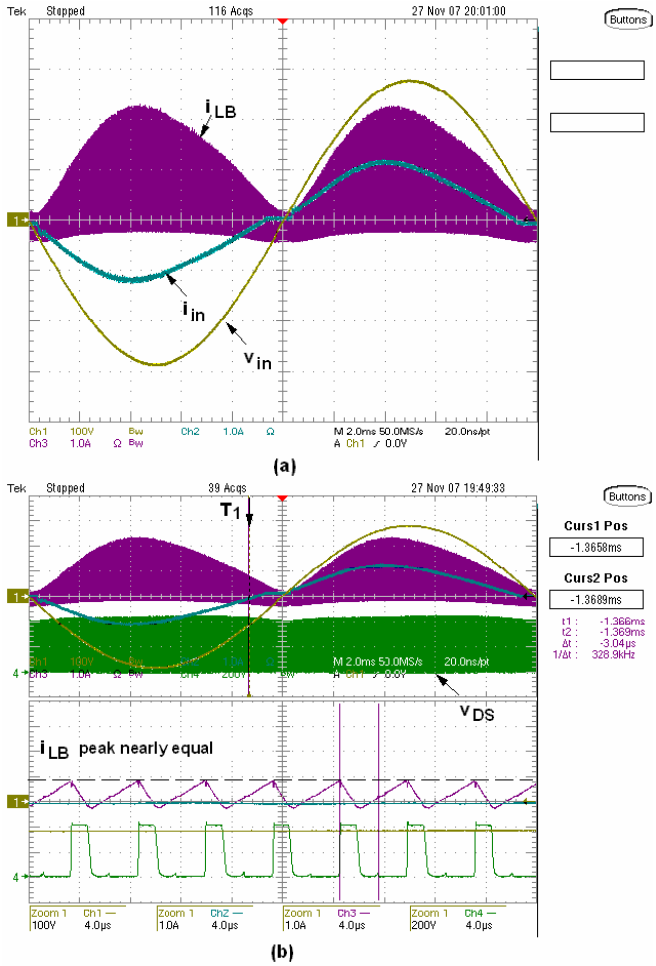

Fig. 13 Key experimental waveforms of 130-W/385-V, universal input DCM/CCM boundary boost PFC with current mode control, 180-kHz switching frequency limit, and loss of valley switching after the onset of switching frequency limit (a) during a line cycle (b) zoomed in around instant T_1.

is not maintained and a maximum switching frequency limit is implemented with current-mode control. The experimental waveforms in Fig. 13 were obtained on a 130-W, universal input, 385-V output DCM/CCM boundary boost PFC prototype circuit controlled by the MC33368 current-mode controller from ON Semiconductor. The line voltage was 200-V_{rms}/50-Hz, the switching frequency limit was 180-kHz, and valley switching was lost after the onset of switching frequency limit. As shown in Fig. 13(a), the boost inductor current and the line current waveforms do not have non-monotonic distortions. In fact, the peak of the inductor current does not have any abrupt changes, as illustrated in Fig. 13(b). It should be noted that the MC33368 controller ensures a minimum off-time, which indirectly limits the switching frequency, whereas the NCP1601 controller directly limits the switching frequency.

V. SUMMARY

A systematic analysis of line current distortions of the DCM/CCM boundary boost PFC converter due to valley switching and switching-frequency limitation is provided. Closed form expressions for the line current are derived. It is shown that line current distortions due to valley switching are practically negligible; whereas, line current distortions due switching frequency limitation can be considerable in the high line-voltage range similarly to the boost PFC converters operating in DCM. It is also shown that if the switching frequency is limited and valley switching is not maintained, the line current is more distorted with voltage mode control than with current mode control. Recommendations how to reduce the line current distortions are also provided. The effects of line current distortions are demonstrated with both simulation and experimental results.

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