Implementation of Open-Loop Control for Interleaved DCM/CCM Boundary Boost PFC Converters

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Abstract - This paper is focused on the implementation of the open-loop control method for interleaved DCM/CCM boundary boost PFC converters where the slave converter is synchronized to the turn-on instant of the master converter and both converters operate with current-mode control. It is shown that this method is the only open-loop control method that provides a stable operation. Implementations of the master-slave synchronization circuit in both analog and digital technology are described. Experimental results obtained on a 400-W, universal input, 400-V output prototype circuit with two interleaved DCM/CCM boundary boost PFC converters controlled by an integrated control circuit currently being developed are provided.

I. INTRODUCTION

In low-power off-line power supplies which require active power factor correction (PFC), a boost converter operating at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) is a widely employed topology [1]-[3]. The major benefit of the DCM/CCM boundary boost PFC converter, compared to the CCM boost PFC converter, is that the reverse-recovery losses related to the boost diode are eliminated [4]. In addition, turn-on with zero-voltage switching (ZVS) of the boost switch can be easily achieved. However, a major drawback of the DCM/CCM boundary boost converter is that its peak input current is twice its average current, which often requires a large differential-mode (DM) electromagnetic-interference (EMI) filter [5]. Another drawback is that its switching frequency, which changes with the instantaneous line voltage and the output power, varies over a very wide range [6]. In order to prevent excessive switching losses at light load, a maximum switching frequency limit is often implemented.

The large input current ripple and, consequently, a large input DM-EMI filter, can be significantly reduced by interleaving two or more boost converters as shown in Fig. 1. In addition, the output current ripple is also significantly reduced, resulting in a reduced equivalent-series-resistance (esr) loss of the output capacitor, and possibly a reduction in capacitor volume. Finally, by interleaving, the application of the DCM/CCM boundary boost PFC converter becomes more attractive at higher power levels. However, since the switching frequency is variable, the synchronization of interleaved DCM/CCM boundary boost PFC converters presents a challenging task.

Very few implementations of the interleaved DCM/CCM boundary boost PFC converters have been published in the literature [5], [7]-[14]. All previously published implementations are based on a master-slave relationship, where the master converter operates as a stand-alone converter, whereas, the slave converter is partially controlled by the master in order to achieve proper interleaving, i.e., a proper phase shift with respect to the master. It has been shown that the slave converter can be synchronized to the master converter with an open-loop method [5], [7]-[11], i.e., by generating a time delay equal to half the switching period of the master determined from its previous switching cycle, or with a closed-loop method [12]-[14], i.e., by measuring the phase difference between the converters and adjusting the phase of the slave based on the phase error. The slave converter with open-loop synchronization can be synchronized to the turn-on instant of the master converter [7]-[10] or to the turn-off instant of the master converter [5], [11]. In both cases, the converters can operate either with current-mode control or with voltage-mode control. A detailed analysis of the open-loop synchronization methods of the slave converter to the master converter is presented in [15]. It is shown in [15] that among the open-loop synchronization methods, the only method that results in a stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control. The slave converter with closed-loop synchronization has been synchro-

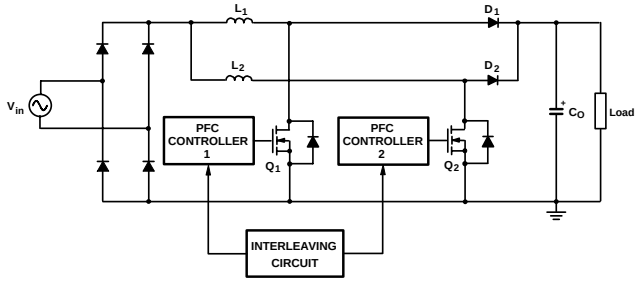

Fig. 1 Basic topology of two interleaved PFC boost converters

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nized to the master converter by using a phase-locked-loop (PLL) approach and adjusting the turn-off instant of the slave converter [12]-[14].

Implementing the interleaving circuit discretely in conjunction with commercially available DCM/CCM boundary control ICs is impractical due to its complexity, which leads to a high component count and large board area. In addition, the reference voltage, which is compared to the sensed ramp voltage at the input of the pulse-width modulator (PWM), is inaccessible in today's control ICs. Consequently, the master and slave cannot share the same reference voltage. Although the master and slave can have separate reference voltages, this leads to an additional interleaving error. Therefore, the development of an integrated control IC for the interleaved DCM/CCM boundary boost PFC converters is highly desirable.

This paper is focused on the implementation of the open-loop control method where the slave converter is synchronized to the turn-on instant of the master converter and both converters operate with current-mode control. In Section II, a review of the open-loop synchronization methods is provided. In Section III, possible implementations of the master-slave synchronization circuit are presented. Experimental results obtained on a 400-W, universal input, 400-V output, interleaved DCM/CCM boundary boost PFC prototype circuit controlled by an integrated control circuit currently being developed are presented in Section IV.

II. Review of Open-Loop Synchronization Methods

As mentioned in Section I, with open-loop synchronization, the slave converter can be synchronized to the turn-on instant or to the turn-off instant of the master converter. In both cases, the converters can operate either with current-mode control or with voltage-mode control.

A. Synchronization of Slave to Turn-on Instant of Master

The basic control circuit and key waveforms of two interleaved DCM/CCM boundary boost PFC converters with current-mode control, when the slave is synchronized to the turn-on instant of the master, is shown in Fig. 2. The master

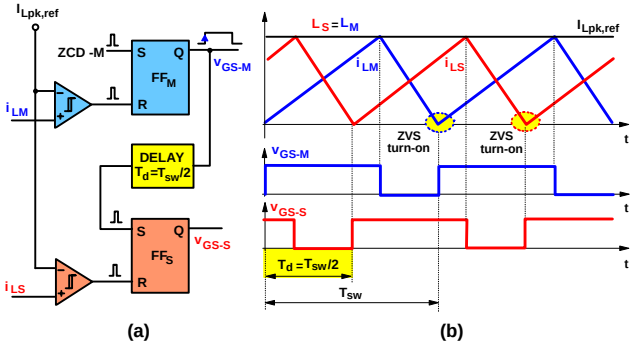

Fig. 2 (a) Basic control circuit and (b) key waveforms of two interleaved DCM/CCM boundary boost PFC converters operating with current-mode control, when the slave is synchronized to the turn-on instant of the master

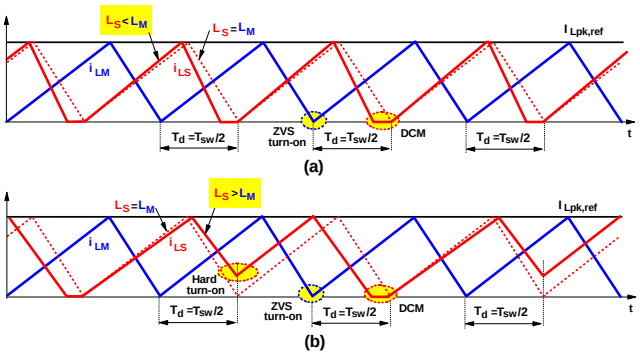

Fig. 3 Inductor current waveforms of the master and slave operating with current-mode control, when the slave is synchronized to the turn-on instant of the master: (a) $L_S < L_M$, and (b) $L_S > L_M$

is turned on by zero-current-detection pulse ZCD-M, while the slave is turned on after delay T_d, which is equal to half the switching period of the master determined from the master's previous switching cycle with respect to the turn-on instant of the master. Both the master and slave are turned on with ZVS. It is assumed that the resonant interval, during which the voltage of a boost switch resonates down to its valley, is negligible compared to the switching period. The master and slave are turned off by their own PWM, which compares the corresponding inductor current $i_{LM(S)}$ used as a ramp signal to the sinusoidal reference current $I_{Lpk,ref}$ used as a feedback signal, which is proportional to the output of the voltage-loop error amplifier. The basic control circuit and key waveforms with voltage-mode control are identical to those in Fig 2 except that the corresponding ramp signals are voltage ramps with a constant slope, each synchronized to the turn-on instant of the corresponding boost converter; whereas, the feedback signal is the output voltage of the voltage-loop error amplifier.

The key difference between current-mode and voltage-mode control is that the slope of the ramp in current-mode control, i.e., i_L, changes proportionally with the voltage across inductor L, and inversely with the inductance of inductor L, whereas, the slope of the ramp in voltage-mode control is always constant. This difference results in very different operation when the inductances are mismatched, or, when delay time T_d is perturbed.

If the inductances of the master and slave with current-mode control are mismatched, the boost switch of the slave will lose ZVS turn-on. In fact, if $L_S < L_M$, the slave will operate in DCM, as shown in Fig. 3(a) and, if $L_S > L_M$, the boost switch of the slave will alternately turn on with hard

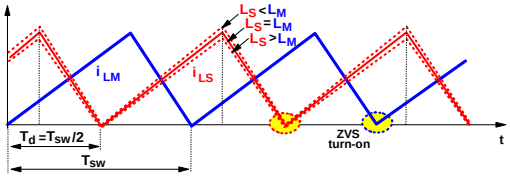

Fig. 4 Inductor current waveforms of the master and slave operating with voltage-mode control, with mismatched inductances, when the slave is synchronized to the turn-on instant of the master

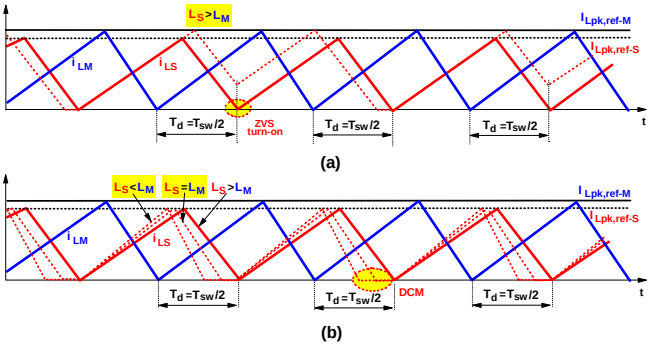

Fig. 5 Inductor current waveforms of the master and slave operating with current-mode control and with the slave synchronized to the turn-on instant of the master, when the slave's reference current is reduced with respect to the master's reference current

switching and in DCM, i.e., the slave will operate with a sub-harmonic oscillation, as shown in Fig. 3(b). With voltage-mode control, if the inductances of the master and slave are mismatched, the ZVS turn-on of the slave switch will not be disturbed, as shown in Fig. 4.

To prevent the turn-on of the boost switch of the slave with hard switching in current-mode control and, consequently, an increased switching loss, the slave's reference current can be reduced with respect to the master's reference current, as shown in Fig. 5(a). Unfortunately, by reducing the slave's reference current, the current sharing between the master and slave becomes significantly worse as illustrated in Fig. 5(b).

A better approach to prevent the turn-on of the boost switch of the slave with hard switching in current-mode control is to identify the master and the slave during the initi-

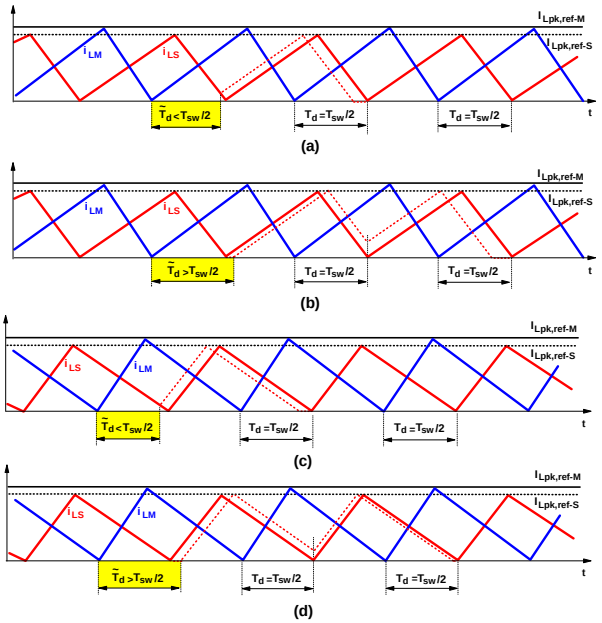

Fig. 6 Effect of delay-time perturbation on the operation of the slave with current-mode control, when the slave is synchronized to the turn-on instant of the master: (a) $D>0.5$, $\tilde{T}_d < T_{sw}/2$, (b) $D>0.5$, $\tilde{T}_d > T_{sw}/2$, (c) $D<0.5$, $\tilde{T}_d < T_{sw}/2$, and (d) $D<0.5$, $\tilde{T}_d > T_{sw}/2$

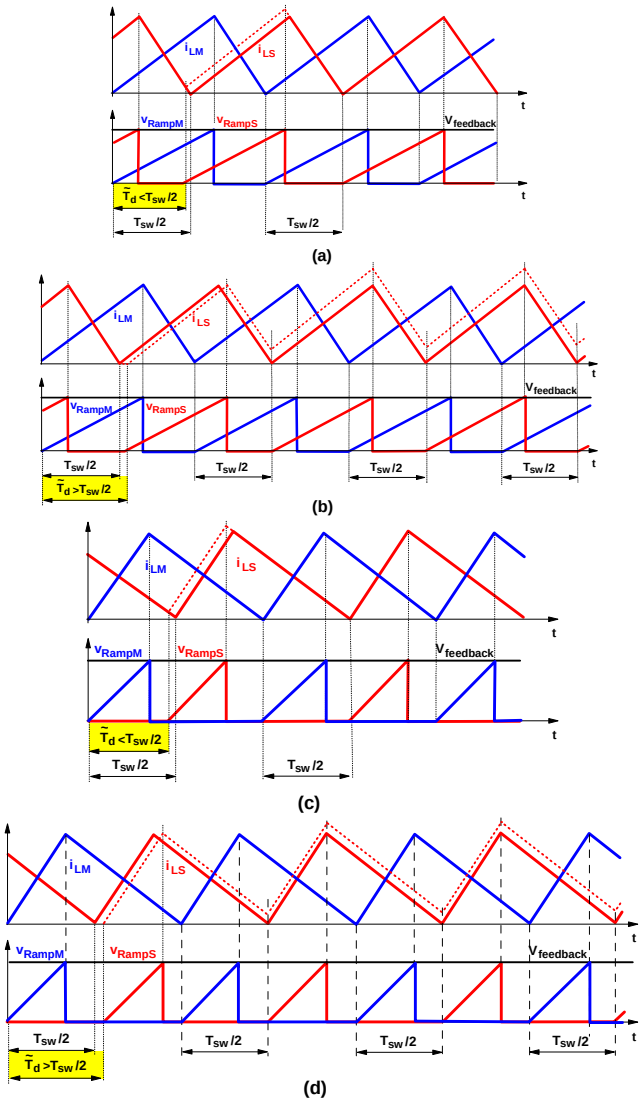

Fig. 7 Effect of delay-time perturbation on the operation of the slave with voltage-mode control, when the slave is synchronized to the turn-on instant of the master: (a) $D>0.5$, $\tilde{T}_d < T_{sw}/2$, (b) $D>0.5$, $\tilde{T}_d > T_{sw}/2$, (c) $D<0.5$, $\tilde{T}_d < T_{sw}/2$, and (d) $D<0.5$, $\tilde{T}_d > T_{sw}/2$

alization phase, i.e., to ensure that the inductance of the slave is always smaller than the inductance of the master. In that case, the inductor currents of the master and slave with mismatched inductances follow the waveforms shown in Fig. 3(a).

Effects of the delay-time perturbation on the operation of the slave with current-mode control and with voltage-mode control are shown in Figs. 6 and 7, respectively. As shown in Fig. 6, the slave with current-mode control always returns to normal operation after one or two switching cycles. In fact, the slave with current-mode control returns to normal operation after one switching cycle when the perturbed delay time is smaller than $T_{sw}/2$, as shown in Figs. 6(a) and 6(c), and after two switching cycles when the perturbed delay time

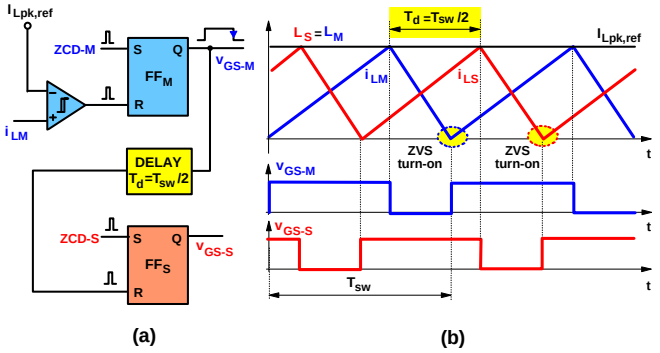

Fig. 8 (a) Basic control circuit and (b) key waveforms of two interleaved DCM/CCM boundary boost PFC converters operating with current-mode control, when the slave is synchronized to the turn-off instant of the master

is greater than $T_{sw}/2$, as shown in Figs. 6(b) and 6(d). However, the slave with voltage-mode control cannot always returns to normal operation, as shown in Fig. 7. When the perturbed delay time is smaller than $T_{sw}/2$, the slave with voltage-mode control returns to normal operation by the next switching cycle, as shown in Figs. 7(a) and 7(c). When the perturbed delay time is greater than $T_{sw}/2$, the slave with voltage-mode control cannot return to normal operation, as shown in Figs. 7(b) and 7(d).

B. Synchronization of Slave to Turn-off Instant of Master

The basic control circuit and key waveforms of two interleaved DCM/CCM boundary boost PFC converters with current-mode control, when the slave is synchronized to the turn-off instant of the master, is shown in Fig. 8. Both the master and slave are turned on with ZVS initiated by their respective ZCD pulses. The master is turned off by its PWM, while the slave is turned off with a delay T_d with respect to the turn-off instant of the master. Delay T_d is equal to half the switching period of the master determined from the master's previous switching cycle. In voltage mode control, the operation of the master is the same as described in Subsection II.A, whereas, the operation of the slave is identical in both control modes.

If the inductances of the master and slave with either current-mode or voltage-mode control are mismatched, the ZVS turn-on of the slave switch will not be disturbed, as shown in Fig. 9.

Effects of the delay-time perturbation on the operation of the slave are shown in Fig. 10. Since the operation of the slave is identical in both current-mode and voltage-mode

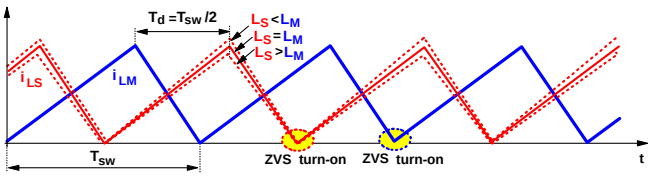

Fig. 9 Inductor current waveforms of the master and slave operating with either current-mode control or voltage-mode control, with mismatched inductances, when the slave is synchronized to the turn-off instant of the master

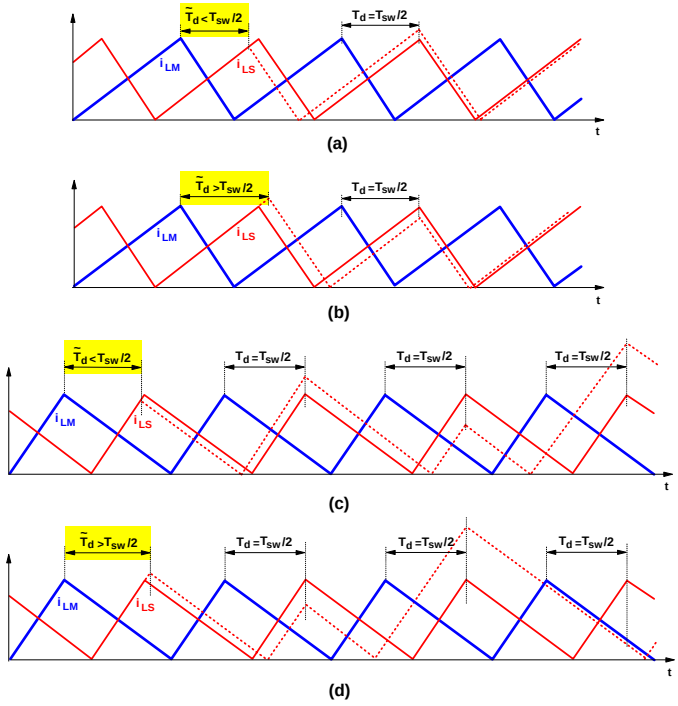

Fig. 10 Effect of delay-time perturbation on the operation of the slave with current-mode control or voltage-mode control, when the slave is synchronized to the turn-off instant of the master: (a) $D > 0.5$, $\tilde{T}_d < T_{sw}/2$, (b) $D > 0.5$, $\tilde{T}_d > T_{sw}/2$, (c) $D < 0.5$, $\tilde{T}_d < T_{sw}/2$, and (d) $D < 0.5$, $\tilde{T}_d > T_{sw}/2$

control, the effects of the delay time perturbation on the operation of the slave shown in Fig. 10 include both control modes. As shown in Figs. 10(a) and (b), if the duty cycle is greater than 0.5, the slave returns to normal operation after a few switching cycles. It can be seen in Figs. 10(a) and (b) that the error between the disturbed and non-disturbed inductor currents of the slave continuously decreases with each switching cycle. However, if the duty cycle is smaller than 0.5, the slave cannot return to normal operation and, in fact, oscillates, as shown in Figs. 10(c) and (d). It can be seen in Figs. 10(c) and (d) that the error between the disturbed and non-disturbed inductor currents of the slave continuously increases with each switching cycle.

A summary of open-loop synchronization methods is presented in Table I [15]. The only open-loop method that results in stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control.

III. Implementation of Master-Slave Synchronization Circuit

To determine the delay time $T_d = T_{sw}/2$, i.e., the half-period instant of the master, the switching period of the master measured in the previous switching cycle is used. This is

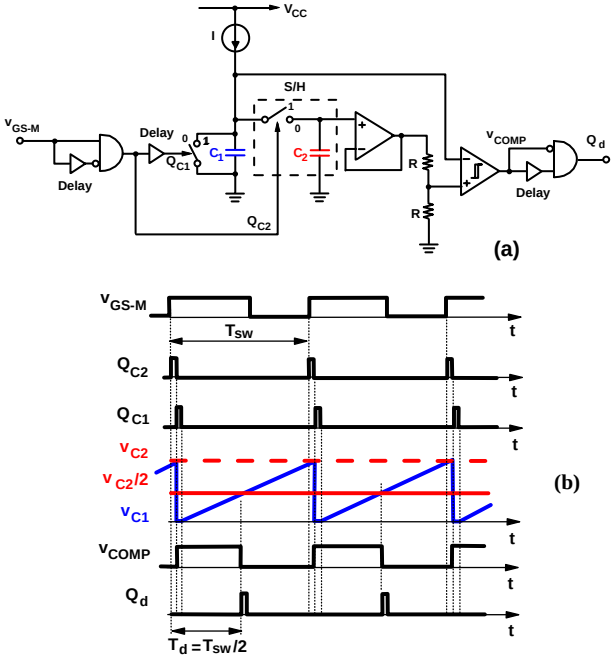

Fig. 11 Implementation of delay circuit $T_d = T_{sw}/2$ in analog technology with single-ramp technique: (a) circuit diagram, (b) key waveforms

possible because the switching frequency is much greater than the line frequency and, therefore, the line voltage is nearly constant during a switching cycle. As a result, the switching period is approximately constant for several switching cycles. The switching period of the master is measured by converting time to voltage by generating a voltage ramp. The voltage ramp is generated by charging a capacitor with a constant current source. The half-period instant of the master can be obtained either with a single-ramp technique [9] or with a dual-ramp technique [7]-[8].

The single-ramp technique based on the approach proposed in [9] is shown in Fig. 11. Voltage v_{C1} across capacitor C_1 is a ramp whose peak is sampled and held (S/H) across capacitor C_2 at the end of each switching cycle. Voltage v_{C2} is then buffered and divided by two, and compared to ramp voltage v_{C1}. The half-period instant of the master is obtained at the intersection of ramp voltage v_{C1} of the present switching cycle with voltage $v_{C2}/2$ from the previous switching cycle, as shown in Fig. 11(b).

The dual-ramp technique based on the approach proposed in [7]-[8] is shown in Fig. 12. The half-period instant of the master is obtained at the intersection of two voltage ramps with equal but opposite slopes. The two voltage ramps are generated by alternately charging and discharging two identical capacitors with constant current source I. It should be noted in Fig. 12(a) that the block MF is a monoflop that can be triggered on both positive and negative edge of its input pulses.

The delay circuit $T_d = T_{sw}/2$ in Figs. 11 and 12, implemented in analog technology, can be also implemented in digital technology. Furthermore, a digital implementation

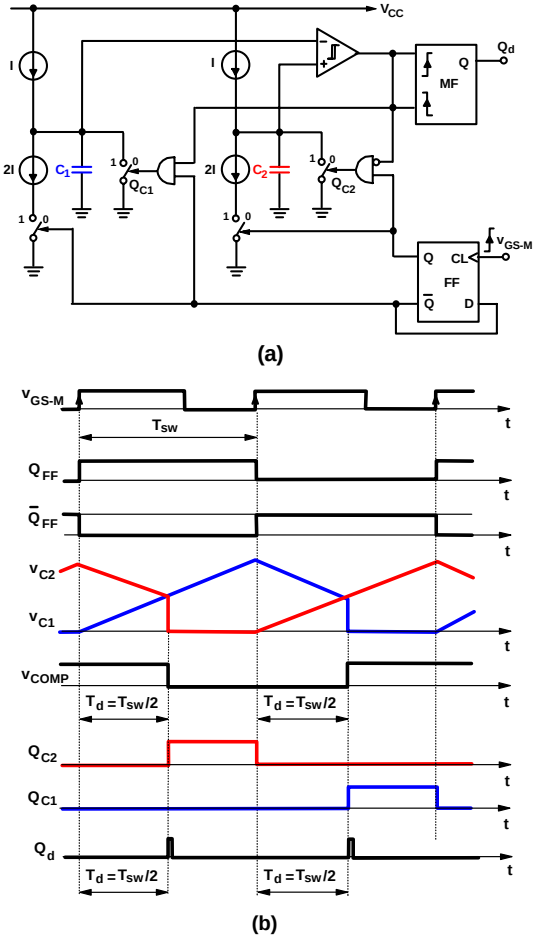

Fig. 12 Implementation of delay circuit $T_d = T_{sw}/2$ in analog technology with dual-ramp technique: (a) circuit diagram, (b) key waveforms

can be cost-effective compared to an analog implementation. An implementation of the delay circuit in Fig. 12 in digital technology is presented in Fig. 13. The voltage ramps in Fig. 13 are implemented with two counters: up-counter UC and down-counter DC. The half-period instant of the master is obtained when the content of down-counter DC becomes zero. With this dual-ramp method, which is slightly different from that in Fig. 12, one digital comparator, which would compare the contents of two voltage ramps with opposite slopes, is eliminated.

IV. Experimental Results

To verify the viability of the open-loop control method when the slave converter is synchronized to the turn-on instant of the master converter, where both converters operate with current-mode control, a 400-W, universal-input, 400-V output prototype circuit with two interleaved DCM/CCM boundary boost PFC converters was built. The control circuit is based on a new integrated controller currently being developed, where the master and the slave are identified during the initialization phase.

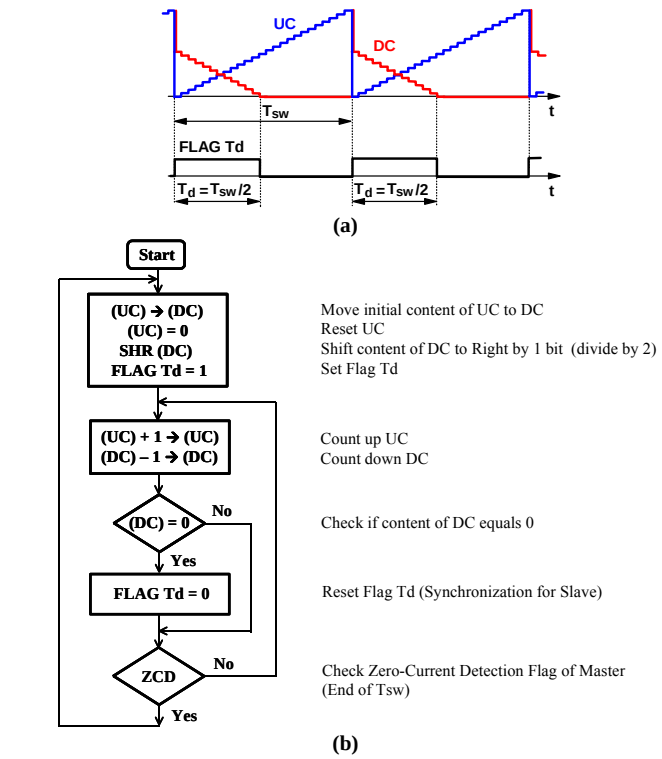

Fig. 13 Implementation of delay circuit $T_d = T_{sw}/2$ in digital technology with dual-ramp method: (a) principle of operation, (b) flow chart

The simplified block diagram of the controller IC is shown in Fig. 14. The master-slave synchronization circuit is implemented in digital technology by using the single-ramp technique shown in Fig. 11. The master-slave identification circuit is implemented with two counters. During the initialization phase, both converters operate independently. The faster converter, i.e., the one with the smaller boost inductance, will reach the end-state of its counter first and, consequently, this converter will be identified as the slave converter.

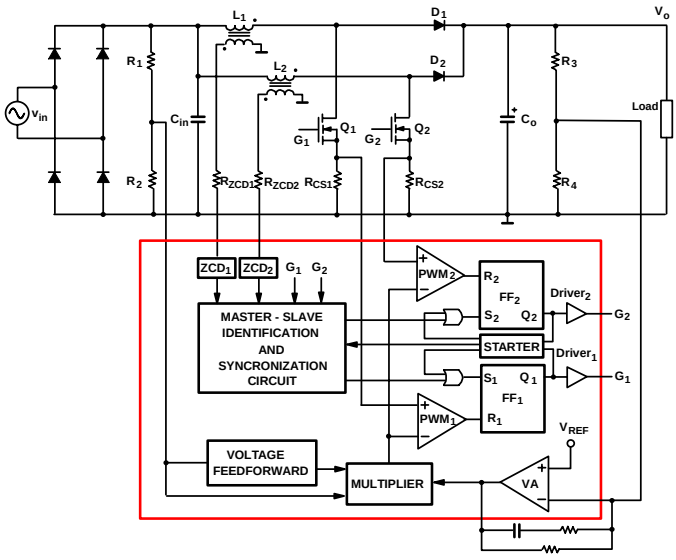

Fig. 14 Block diagram of the experimental circuit

The measured inductor current of the master and slave, i_{LM} and i_{LS}, as well as the sum of the inductor currents, $i_{LM} + i_{LS}$, at full load (400 V, 1 A), at 100-Vrms and 230-Vrms line voltage are shown in Figs. 15(a) and 15(c), respectively. The corresponding zoomed-in waveforms around the peak of the line voltage are shown in Figs. 15(b) and 15(d). The inductor current of the master is shown to operate at the DCM/CCM boundary and the inductor current of the slave is shown to operate slightly in DCM. Both the master and slave operate with valley switching. The interleaved current waveforms in Fig. 15 are in a good agreement with the theoretical waveforms.

V. Summary

Four open-loop interleaving methods for DCM/CCM boundary boost PFC converters with a master-slave relationship are reviewed. With open-loop synchronization, the slave converter can be synchronized to the turn-on or to the turn-off instant of the master converter. In both cases, the converters can operate either with current-mode or voltage-mode control.

It is shown that the only open-loop method that results in stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control.

Possible implementations of the master-slave synchronization circuit in both analog and digital technology are described.

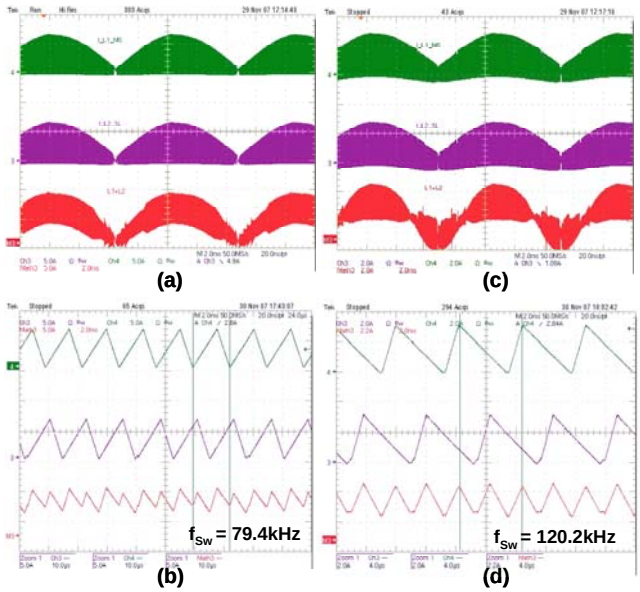

Fig. 15 Measured inductor current of master (top), slave (middle), and interleaved (bottom) at full load (400V, 1A) at (a), (b) 100-V_{rms} (c), (d) 230-V_{rms} line voltage (L_M=175 µH, L_S=166 µH, $\Delta L/L = \pm 2.6\%$). Waveforms in (b), (d) are zoomed in at the peak of the line voltage.

Experimental results obtained on a 400-W, universal input, 400-V output prototype circuit with two interleaved DCM/CCM boundary boost PFC converters controlled by an integrated control circuit currently being developed are provided. The new controller IC is based on the open-loop control method where the slave is synchronized to the turn-on instant of the master and both converters operate with current-mode control.

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TABLE I
SUMMARY OF OPEN-LOOP SYNCHRONIZATION METHODS

Open-loop synchronization methods	Synchronization of Slave to turn-on instant of Master				Synchronization of Slave to turn-off instant of Master			
	Current-mode control		Voltage-mode control		Current-mode control		Voltage-mode control	
Current-sharing error for ±5% (±10%) mismatch of inductances	10% (20%)* 29.8% (58.5%)**		10% (20%)		10% (20%)		10% (20%)	
Normal operation after delay-time perturbation	D > 0.5	D < 0.5	D > 0.5	D < 0.5	D > 0.5	D <0.5	D > 0.5	D < 0.5
	Yes	Yes	No	No	Yes	No	Yes	No

* Master and Slave are identified during the initialization phase (always $L_S < L_M$)
** Master and Slave are NOT identified during the initialization phase ($L_S \leq L_M$ or $L_S \geq L_M$)