Loop Gain Measurement Of Paralleled Dc-Dc Converters With Average-Current-Sharing Control

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Abstract - **Paralleled operation of dc-dc converters is widely used in today's distributed power systems. Special control circuitry is usually necessary to ensure current sharing among the paralleled modules. The average-current-sharing control method is very popular due to its simple implementation and good performance. Although the analysis and design of the average current-sharing control were presented in the past, a loop gain measurement technique has not been published. This paper presents a practical loop gain measurement technique which uses two excitation sources. Measured and theoretical data are compared to verify the proposed technique.**

I. Introduction

Parallel operation of dc-dc converters is widely used in today's distributed power systems due to redundancy, expandability of output power, easy standardization, and improved thermal management. Generally, it is desirable to distribute the load current equally among paralleled converters. However, because of limited component tolerances and an asymmetric layout of the converters, their output currents can be significantly different. To balance the load current among the paralleled modules, a variety of approaches, with different complexities and current-sharing performances, were proposed and employed by industry [1] – [6].

The simplest current-sharing technique is the open-loop (droop) method [1]–[2], which relies on the output resistance of paralleled modules to maintain relatively even current distribution among the modules. The droop method is easy to implement and it does not require any communication (control-wire connection) between the modules. However, this technique has poor output voltage regulation as a result of droop output characteristics and requires individual converter reference voltages to be trimmed to closely match each other.

More complex, closed–loop (active) current-sharing techniques [3]-[6] overcome the disadvantage of poor output regulation by employing feedback control. One of the most popular closed-loop methods is an average-current-sharing method [4] due to its simple implementation and high performance. A simplified functional diagram of paralleled converters with average-current-sharing control is shown in Fig. 1.

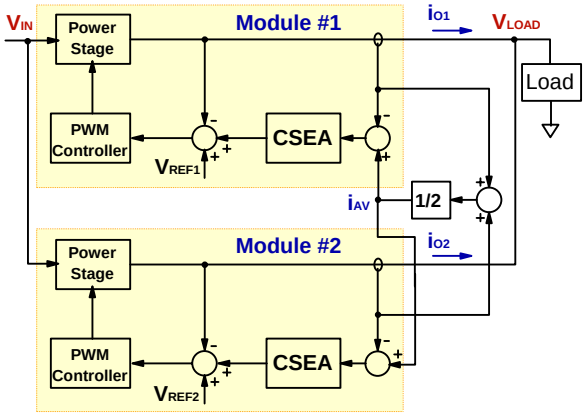

Fig. 1. Simplified block diagram of paralleled converters with average-current-sharing control.

The output currents are sensed and compared to average converter output current i_{AV}. The resulting current-sharing error signals are then processed by current-sharing-error amplifiers CSEA and injected in the voltage loops of paralleled modules. When the CSEA gain is high, the corresponding current-sharing error is low, and currents of the paralleled modules are essentially equal.

The steady-state performance of the average-current sharing control technique was analyzed in [5]. For paralleled converters delivering power to modern data processing equipment, the dynamic current-sharing performance during fast-slew-rate load transients becomes more and more important. To provide adequate transient current sharing, the high bandwidth of the current-sharing loop, as well as ample stability margins, are required. The dynamic modeling and analysis of average-current-sharing control can be found in [3], [7], [8], [9], and [10]. Perhaps the most general and systematic analysis was presented in [8] and [9]. Although the references contain dynamic modeling, analysis, and design of average-current-sharing control, none of them offer a method of measuring the current-sharing loop gain in the hardware setup. The purpose of this paper is to propose a practical technique for measurement of the average-current-sharing loop gain, to derive the theoretical loop gain, and to compare the measured and calculated results.

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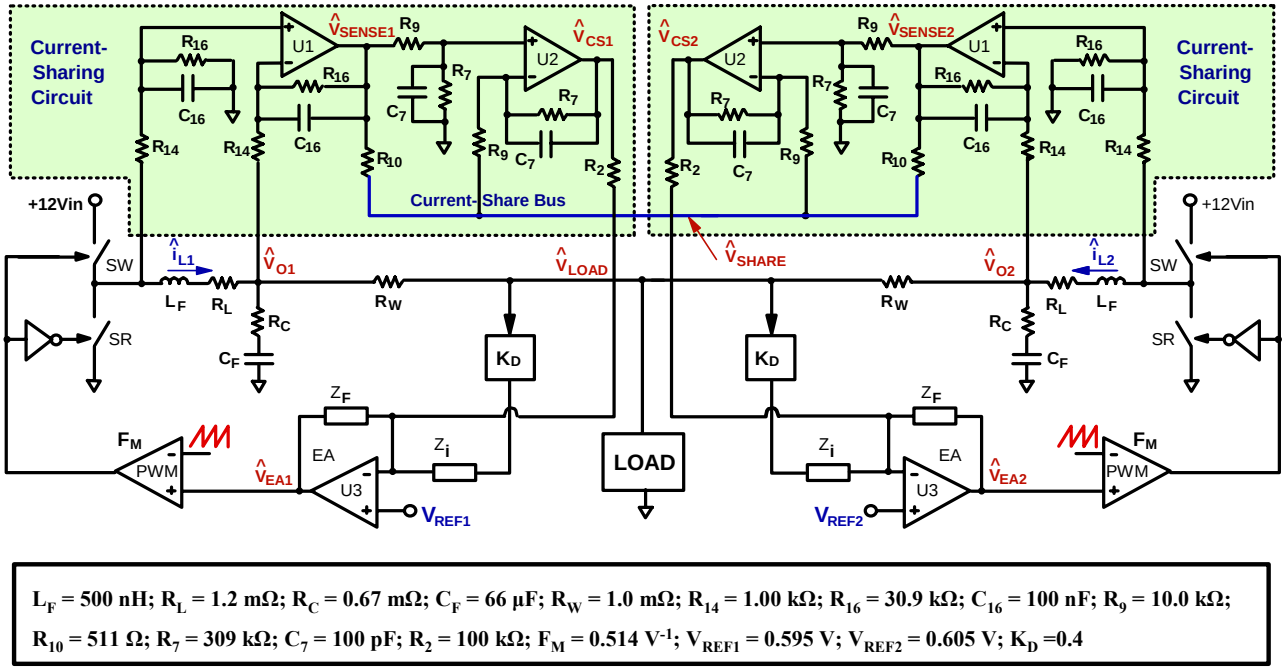

Fig. 2. Simplified circuit diagram of paralleled SR-buck converters and list of component values.

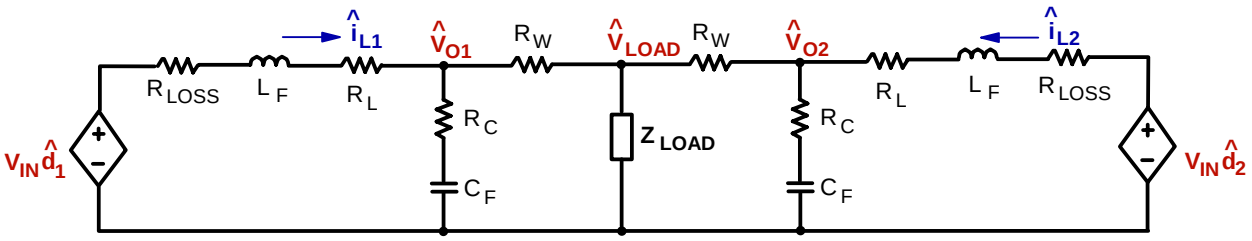

Fig. 3. Averaged model of merged power stages of two paralleled modules.

II. Current-Sharing Modeling and Calculated Loop Gain Of Paralleled Dc-Dc Converters

A detailed schematic of two paralleled SR-buck converter modules with average-current-sharing circuits and the list of component values are shown in Fig. 2. Blocks K_D represent the gain of load voltage resistive dividers and resistance R_W represents the interconnect impedance. The modules in Fig. 2 are identical except for mismatched reference voltages V_{REF1} and V_{REF2}. Current balancing of modules' output currents is achieved through balancing of their inductor currents i_{L1} and i_{L2}. Balancing of the inductor currents has the advantage of lossless current sensing. Namely, the module inductor current is sensed based on the voltage drop across ESR R_L of inductor L_F. The voltage across inductor L_F is amplified and averaged by differential amplifier U1, whose transfer function has a low-pass-filter property. Voltage $\hat{V}_{SENSE}$ at the output of amplifier U1 is related to inductor current $\hat{i}_L$ as

$$\hat{V}_{SENSE} = \hat{i}_L \cdot Z_X , \qquad (1)$$

where $Z_X = (R_L + s \cdot L_F) \cdot \dfrac{R_{16}/R_{14}}{1 + s \cdot R_{16} \cdot C_{16}}$.

Voltage $\hat{V}_{SHARE}$ on the current-share bus is the average of signals $\hat{V}_{SENSE1}$ and $\hat{V}_{SENSE2}$

$$\hat{V}_{SHARE} = 1/2 \cdot \left(\hat{V}_{SENSE1} + \hat{V}_{SENSE2}\right). \qquad (2)$$

The difference between sensed voltage $\hat{V}_{SENSE}$ and current-share bus voltage $\hat{V}_{SHARE}$ is proportional to the current-sharing error. This error is amplified by differential amplifier U2, which has transfer function $G_{CS} = \dfrac{R_7/R_9}{1 + s \cdot R_7 \cdot C_7}$.

Resistor R2 at the output of amplifier U2 converts voltage $\hat{V}_{CS}$ into current, which is injected into the voltage loop, as shown in Fig. 2. Current-sharing signals $\hat{V}_{CS1}$ and $\hat{V}_{CS2}$, which are injected in the voltage loops, are derived as

$$\hat{V}_{CS1} = G_{CS} \cdot \left(\hat{V}_{SENSE1} - \hat{V}_{SENSE2}\right)/2,$$
$$\hat{V}_{CS2} = G_{CS} \cdot \left(\hat{V}_{SENSE2} - \hat{V}_{SENSE1}\right)/2 = -\hat{V}_{CS1}. \quad (3)$$

Error amplifier U3 of the voltage feedback loop is described by equation

$$\hat{V}_{EA} = -G_{EA1} \cdot \hat{V}_{LOAD} - G_{EA2} \cdot \hat{V}_{CS}, \quad (4)$$

where $G_{EA1} = Z_F / Z_i$ and $G_{EA2} = Z_F / R_2$.

The averaged model of two combined power stages is shown in Fig. 3. Resistors R_{LOSS} in Fig. 3 model conduction losses of the switch and SR. The combined power stage is described by equations

$$\hat{V}_{O1} = G_{vd} \cdot \hat{d}_1 + G_{vd}^{cc} \cdot \hat{d}_2, \quad \hat{V}_{O2} = G_{vd}^{cc} \cdot \hat{d}_1 + G_{vd} \cdot \hat{d}_2 \quad (5)$$

$$\hat{i}_{L1} = G_{id} \cdot \hat{d}_1 + G_{id}^{cc} \cdot \hat{d}_2, \quad \hat{i}_{L2} = G_{id}^{cc} \cdot \hat{d}_1 + G_{id} \cdot \hat{d}_2, \quad (6)$$

$$\hat{V}_{LOAD} = \left[(G_{vd} + G_{vd}^{cc})/(2 + R_W / Z_{LOAD})\right] \cdot \left(\hat{d}_1 + \hat{d}_2\right), \quad (7)$$

where $G_{vd} = \hat{V}_{O1}/\hat{d}_1 = \hat{V}_{O2}/\hat{d}_2$, $G_{id} = \hat{i}_{L1}/\hat{d}_1 = \hat{i}_{L2}/\hat{d}_2$ are direct transfer functions, and $G_{vd}^{cc} = \hat{V}_{O2}/\hat{d}_1 = \hat{V}_{O1}/\hat{d}_2$, $G_{id}^{cc} = \hat{i}_{L1}/\hat{d}_2 = \hat{i}_{L2}/\hat{d}_1$ are cross-coupling transfer functions.

Based on equations (1)-(7), the control block diagram of paralleled modules with remote voltage sensing is shown in Fig. 4. Since the diagram is symmetrical and $\hat{V}_{CS1} = -\hat{V}_{CS2}$, duty cycles $\hat{d}_1$ and $\hat{d}_2$ are equal in magnitude and opposite in phase, namely, $\hat{d}_1 = -\hat{d}_2$. Based on equations (6) and (7),

$$\hat{V}_{LOAD} = 0 \text{ and } \hat{i}_{L1} = -\hat{i}_{L2}. \quad (8)$$

Relationships (8) allow reduction of the block diagram, as shown in Fig. 5. Since $\hat{V}_{LOAD} = 0$, signals excited by sources $V_{IN} \cdot \hat{d}_1$ and $V_{IN} \cdot \hat{d}_2$ cannot propagate to the power stages of the opposite modules and, therefore, $G_{id}^{cc} = 0$ and $G_{vd}^{cc} = 0$.

Based on the reduced block diagram in Fig. 5, the current-sharing loop gain is finally derived as

$$T_{CS} = G_{EA2} \cdot F_M \cdot G_{id} \cdot Z_X \cdot G_{CS}. \quad (9)$$

It should be noted that power stage transfer function $G_{id} = \hat{i}_{L1}/\hat{d}_1$ in equation (9) is calculated with the shorted load since $\hat{V}_{LOAD} = 0$. This condition also means that current-sharing loop gain T_{CS} is independent of the load.

Derived loop gain T_{CS} is practical since it provides the basis for conventional design of current-sharing error amplifier transfer function G_{CS} in the frequency domain.

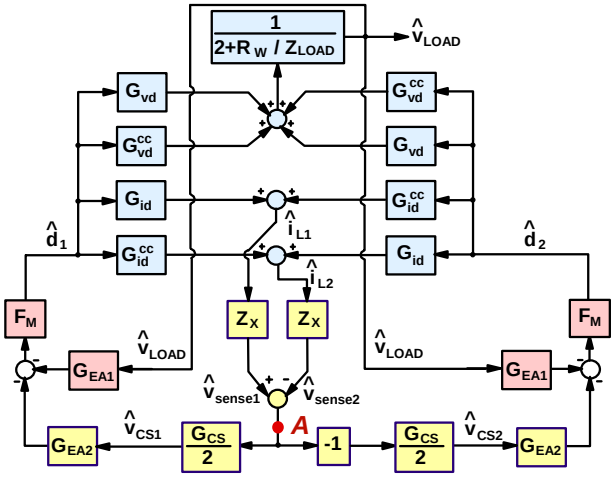

Fig. 4. Block diagram of two paralleled modules.

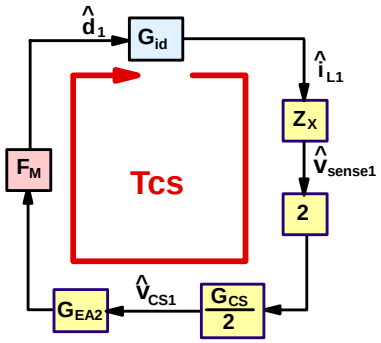

Fig. 5. Reduced block diagram for current-sharing loop gain derivation.

III. Proposed Current-Sharing Loop Gain Hardware Measurement

Generally, to measure a meaningful current-sharing loop gain, it is desirable to identify the location where breaking the loop interrupts the flow of current-sharing signals of both modules. At that location, the excitation signal is added and the loop gain is measured as the ratio of the test and reference signals. Observation of the diagram in Fig. 4 suggests that the only location that satisfies the indicated condition is location **A**. If the excitation signal is added at location **A**, then, $\hat{V}_{CS1} = -\hat{V}_{CS2}$, $\hat{d}_1 = -\hat{d}_2$, $\hat{V}_{LOAD} = 0$, $\hat{i}_{L1} = -\hat{i}_{L2}$, i.e., the signal relationships of the original circuit are observed. Unfortunately, point A exists only on the block diagram and not in the real circuit. Therefore, a different measurement

approach should be considered. To derive the desired measurement method, the block diagram in Fig. 6 is examined. The excitation source can be added at the output of amplifier U2 in Fig. 2 where the relationship between the input and output impedances is maintained [11]. Specifically, magnitude of U2 output impedance is much less than the value of resistor R2. If the single injection source $\hat{V}_{AC1}$ is added, as shown in Fig. 6, then $\hat{d}_1 \propto \hat{V}_{CS1} + \hat{V}_{AC1}$ and $\hat{d}_2 \propto \hat{V}_{CS2} \propto -\hat{V}_{CS1}$. Hence, $\hat{d}_2 \neq -\hat{d}_1$ and the signal balance of the original circuit is violated. To demonstrate the drawbacks of the single-injection-source measurement, corresponding loop gain T_{CS1} was simulated using SIMPLIS software for paralleled converters, shown in Fig. 2, and is plotted in Fig. 7. Loop gain T_{CS1} stays below 0-dB level at low frequencies, and goes above 0 dB in the frequency range from 5.3 to 7.6 kHz. The maximum value of this gain in this range is only 0.3 dB. After 7.6-kHz frequency loop gain T_{CS1} rapidly decreases with –40 dB/decade slope. This loop gain still carries information about the current-sharing loop stability. Namely, gain T_{CS1} indicates that the loop is stable with phase margin of 100º, which corresponds to 7.6-kHz crossover frequency, and the gain margin is above 20 dB. However, it is not possible to define a meaningful bandwidth for loop gain T_{CS1}. Also, the traditional design of current-sharing error amplifier compensation in the frequency domain is not possible since there are two current-sharing amplifiers in the circuit and relationship between loop gain T_{CS1} and the current-sharing amplifier transfer function G_{CS} is not straightforward. Hence, the single-source-injection measu-rement technique fails and a more sophisticated technique should be proposed.

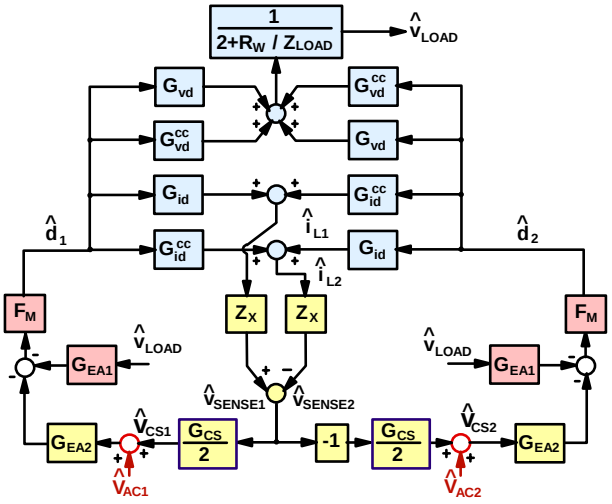

Fig. 6. Placement of excitation sources for loop gain measurement.

In order to keep the signal balance and measure a meaningful loop gain T_{CS}, two excitation sources $\hat{V}_{AC1}$ and $\hat{V}_{AC2}$ are added, as shown in Fig. 6. In this case, $\hat{d}_1 \propto \hat{V}_{CS1} + \hat{V}_{AC1}$ and $\hat{d}_2 \propto -\left(\hat{V}_{CS1} - \hat{V}_{AC2}\right)$. If excitation sources have the same magnitude and the opposite phase, i.e. $\hat{V}_{AC2} = -\hat{V}_{AC1}$, then $\hat{d}_2 = -\hat{d}_1$, $\hat{V}_{LOAD} = 0$, $\hat{i}_{L1} = -\hat{i}_{L2}$, and the signal balance of the original circuit is restored. It is easy to verify that with two excitation sources the loop gain is the same as the one given by equation (9). Therefore, the current-sharing loop gain measurement can be accomplished with two excitation sources $\hat{V}_{AC1}$ and $\hat{V}_{AC2} = -\hat{V}_{AC1}$. The two sources can be implemented as voltages of the opposite polarity on two secondary windings of a three-winding excitation transformer. The secondary windings should have the same number of turns $N_{S1} = N_{S2}$. A practical measurement setup is shown in Fig. 8. The current-sharing loop gain is then measured as the ratio $\hat{V}_{TEST} / \hat{V}_{REF}$. Since the paralleled modules are identical, pair of $\hat{V}_{REF}$ and $\hat{V}_{TEST}$ signals can be measured on either module.

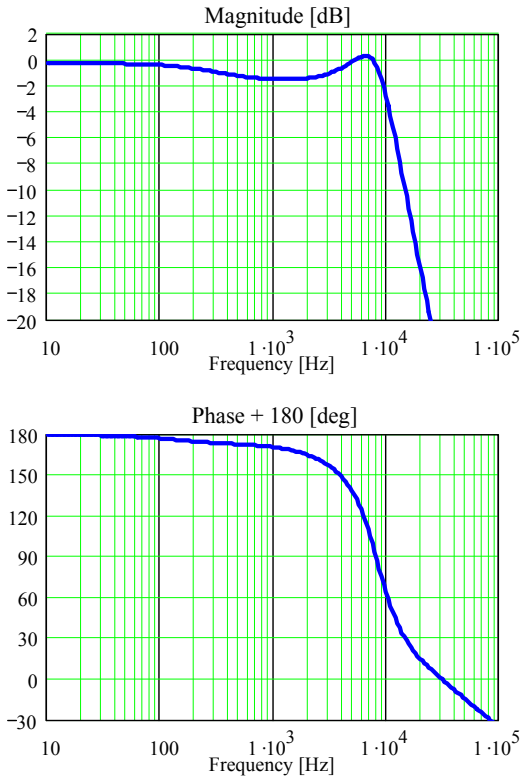

Fig. 7. Simulated Bode plots of current-sharing loop gain T_{CS1} with single injection source.

V. Experimental Results

To test the proposed measurement technique, two 330-kHz, 12-V input, 20-A output POL converters with adjustable

output voltage were paralleled. The simplified schematic and component values of the POL converters are shown in Fig. 2. Measurements of transfer functions were conducted at 1.5-V output voltage and 40-A load current. A three-winding transformer for the signal injection was implemented as follows. The transformer has Ferroxcube PTS30/19/I-3C90 ferrite core and three identical windings of 160 turns. Solid copper wire of AWG #30 is used for the windings, which are bifilar wound. The transformer has a high magnetizing inductance, 68 mH, and low leakage inductance, 23 µH, allowing measurement in a wide frequency range from 10 Hz up to several MHz.

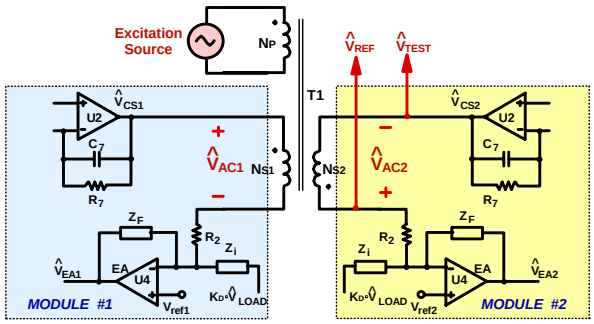

Fig. 8. Practical setup for current-sharing loop gain measurement.

Before measuring the loop gain, the assumption of zero perturbation of the load voltage, used in Sections II and III, has to be verified. Since the real modules are not identical due to component tolerances and asymmetrical layout of the system board, the load voltage perturbation cannot be exactly zero. To verify this assumption of the proposed measurement technique, transfer function $\hat{V}_{LOAD}/\hat{V}_{CS}$ was measured in setups with one and two excitation sources. The measured results for component values, shown in Fig. 2, can be seen in Fig. 9. The implementation of the voltage-loop error amplifier, which was used in the experimental setup, is shown in Fig. 10. The difference amplifier in Fig. 10 provides differential sensing of the remote load voltage. Figure 9 demonstrates that the two-source injection dramatically reduces ac component of V_{LOAD} and makes it practically zero in the frequency range of interest. The measured and calculated current-sharing loop gains are plotted in Fig. 11 and show good agreement. The measured loop gain has 10.4-kHz bandwidth, 51° phase margin, and 13-dB gain margin, whereas the calculated loop gain has 8.6-kHz bandwidth, 44° phase margin, and 21-dB gain margin. The measured and calculated loop gains start to diverge at high frequencies where the load voltage perturbation shows significant increase.

The measured voltage loop gain of stand-alone experimental module is plotted in Fig. 12. The measurement was conducted with five Panasonic polymer aluminum 150-µF, 12-mΩ ESR load capacitors. Since the voltage loop gain in Fig. 12 has 114-kHz bandwidth, there is sufficient separation between gain crossover frequencies of the voltage and current-sharing loops to prevent any undesirable interaction.

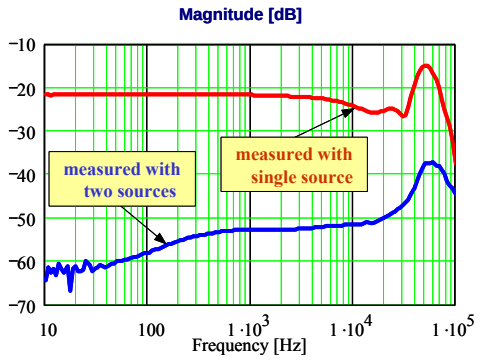

Fig. 9. Measured magnitude of transfer function V_{LOAD}/V_{CS}.

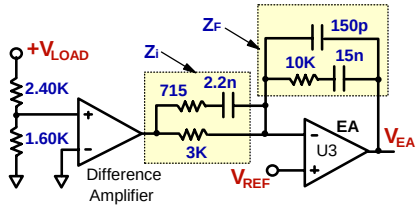

Fig. 10. Implementation of load voltage sensing circuit and voltage-loop error amplifier EA.

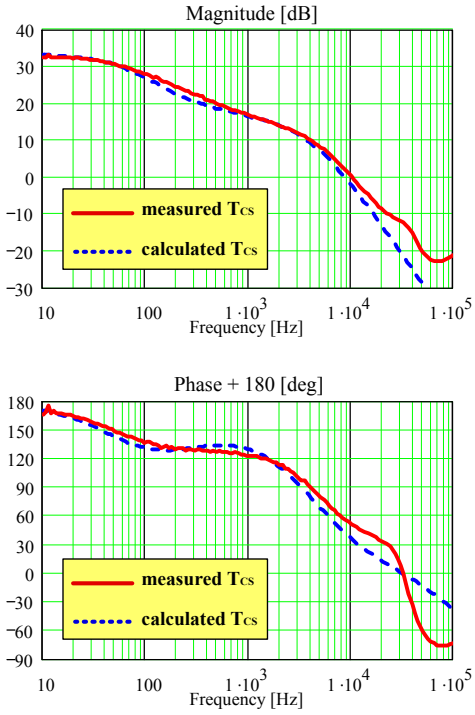

Fig. 11. Measured and calculated loop gain T_{CS}.

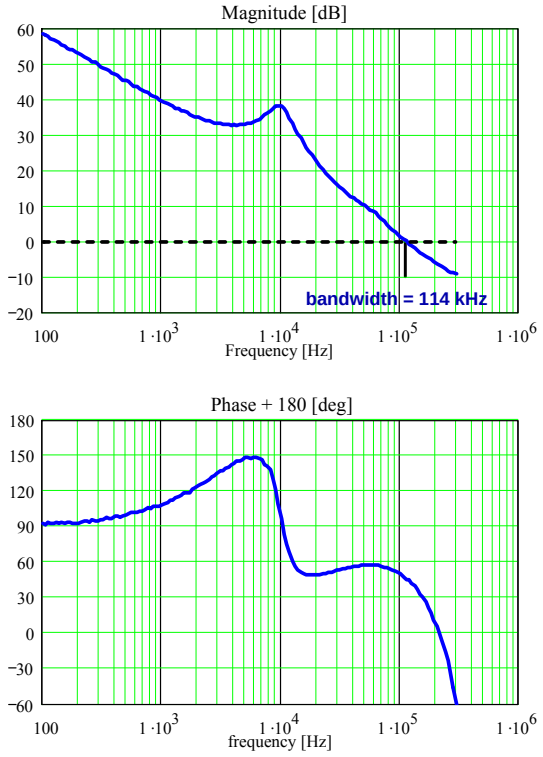

Fig. 12. Measured voltage loop gain of stand-alone module.

V. SUMMARY

Sufficient bandwidth and stability margins of the current-sharing loop are important for design of high-performance paralleled dc-dc converters. Measurement of a meaningful current-sharing loop gain cannot be accomplished with traditional single-injection-source approach. To measure the current-sharing loop gains, the setup with two injection sources of the same magnitude and opposite phase was proposed. Two-source injection is easily implemented by using an excitation transformer with two secondary windings which have the same number of turns. The current-sharing loop gain was derived for identical converters with mismatched references and was compared to the measured loop gain of two paralleled POL converters. Good agreement between the measured and calculated current-sharing loop gains verifies proposed measurement technique.

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