

# Analysis and Performance Evaluation of Interleaved DCM/CCM Boundary Boost PFC Converters Around Zero-Crossing of Line Voltage

Claudio Adragna<sup>1</sup>, Laszlo Huber<sup>2</sup>, Brian T. Irving<sup>2</sup>, and Milan M. Jovanović<sup>2</sup>

<sup>1</sup> STMicroelectronics  
Offline Power Supply Business Unit  
Application Laboratory  
20041 Agrate Brianza  
Via C. Olivetti, 2

<sup>2</sup> Delta Products Corporation  
Power Electronics Laboratory  
P.O. Box 12173  
5101 Davis Drive  
RTP, NC 27709, U.S.A.

**Abstract** – In this paper, causes of improper interleaving of two DCM/CCM boundary boost PFC converters around zero crossing of the line voltage are analyzed. The converters have a master-slave relationship. The slave is synchronized to the turn-on instant of the master by using an open-loop interleaving method. It is shown that phase shifting the gate drive signals of the two stages by 180° does not provide 180° phase-shift between the individual inductor currents, which is the real purpose of interleaving. Fortunately, the improper interleaving around zero crossing of the line voltage does not deteriorate the power factor (PF) and total harmonic distortion (THD). It is shown that although the interleaving method can be improved to achieve close to 180° phase shift between the master and slave currents even around zero crossing of the line voltage, the improved interleaving has only a minor effect on the PF and THD.

## I. INTRODUCTION

Interleaving techniques extend the usage of DCM/CCM boundary boost PFC converters (see Fig. 1) to power levels that are prohibitive for a single stage. Consequently, the benefits offered by these converters, such as the absence of issues related to the reverse-recovery of the boost diode and the possibility to achieve turn-on with zero-voltage switching (ZVS) can be extended to power levels where CCM operation would have been the only choice otherwise. There are additional benefits as well, resulting from the superposition of the individual inductor currents. Due to the lower ripple amplitude of both the input and the output currents, the differential-mode input EMI filter can be significantly reduced and the output bulk capacitor is much less stressed.

While interleaving can be easily achieved in fixed-frequency systems, in the PFC stages under consideration the switching frequency of each stage is variable and depends essentially on the inductance value of the respective boost inductors.

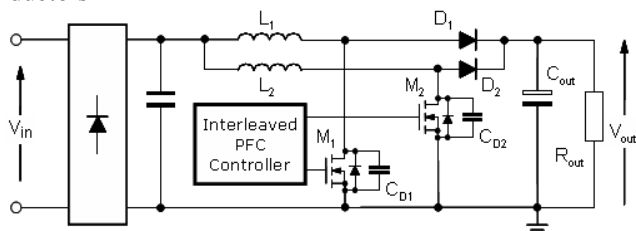


Fig. 1. Principle schematic of a system of two interleaved DCM/CCM boundary boost PFC converters

Though the nominal value of inductances is chosen to be the same for both, in mass production the actual inductance of each sample will randomly fall in a tolerance band around that nominal value. As a result, the two stages, if not properly controlled, will run at different frequencies with a continuously changing phase-shift and a combined input current ripple continuously oscillating from zero to twice the peak input current of each stage.

To synchronize the switching of the two stages, it is possible to use the master-slave approach [1]-[10], where the master operates as a free-running converter, while the slave is controlled so that its phase-shift is 180° with respect to the master, to minimize the combined input current ripple. Additionally, the two stages should share the total load as equally as possible. Lastly, CCM operation must be avoided.

Interleaving with master-slave approach can be achieved with either open-loop [1]-[7] or closed-loop methods [8]-[10]. In this paper, the focus is on open-loop methods, where the slave's switch is turned on after a delay equal to one half of the master's period, measured in the previous switching cycle. Among the open-loop methods, only the method when the slave is synchronized to the turn-on instant of the master with current-mode control can provide stable operation [7].

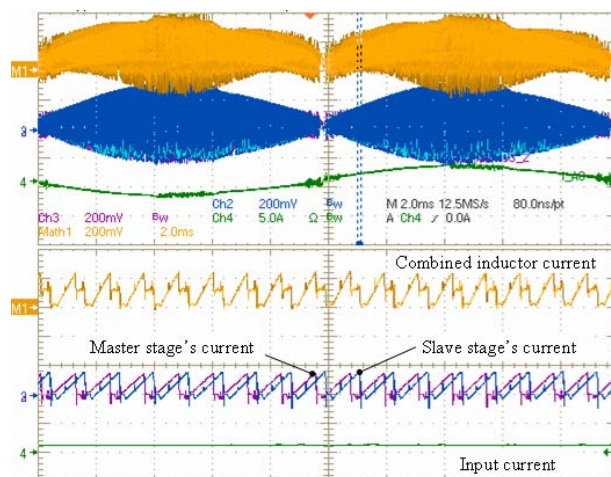


Fig. 2. Phase-shift error in the individual inductor currents around zero-crossing of line voltage (note: current ramps are not equally spaced) in a system designed for 400V/400W output, with  $L_1 = 175 \mu\text{H}$ ,  $L_2 = 167 \mu\text{H}$  at  $V_{in} = 115 \text{ Vac}$  and half load.

It should be noted that, generally, this control method ensures that the slave's gate drive signal is phase shifted by  $180^\circ$  with respect to the master's gate drive signal. However, the real purpose of interleaving is to phase shift the individual inductor currents by  $180^\circ$ .

Experimental results show that today's interleaving techniques do not provide individual inductor currents phase shifted by  $180^\circ$  and, additionally, interleaving can be almost completely lost around the zero-crossing of the line voltage, as illustrated in the oscilloscope picture in Fig. 2. The interleaving behavior around the zero-crossing of the line voltage has not been addressed in the literature yet.

In this paper, causes of improper interleaving around the zero crossing of the line voltage are analyzed in details. It is shown that the improper interleaving around zero crossing of the line voltage does not deteriorate the power factor (PF) and total harmonic distortion (THD). In fact, it is shown that although the interleaving method can be improved to achieve close to  $180^\circ$  phase shift between the master and slave currents even around zero crossing of the line voltage, the improved interleaving has minor effect on the PF and THD. A possible implementation of the improved interleaving circuit is also included.

## II. REVIEW OF OPEN-LOOP MASTER-SLAVE SYNCHRONIZATION

It is shown in [7] that among the open-loop interleaving methods for PFC boost converters operating at the DCM/CCM boundary with a master-slave approach, the only method resulting in a stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control. The basic control circuit and key waveforms are shown in Fig. 3.

The master is turned on by zero-current-detection pulse ZCD-M, while the slave is turned on after delay  $T_d$ , equal to half the switching period of the master determined from the master's previous switching cycle, with respect to the turn-on instant of the master. This provides  $180^\circ$  phase-shift in the gate-drive signals. The master and slave are turned off by their own PWM, by comparison of the corresponding inductor current  $i_{LM(S)}$ , used as a ramp signal, to the sinusoidal reference current  $I_{Lpk,ref}$  programmed by the voltage-loop.

If the two inductors perfectly match ( $L_S = L_M$ ), as shown in Fig. 3(b), both the master and slave are turned on with ZVS.

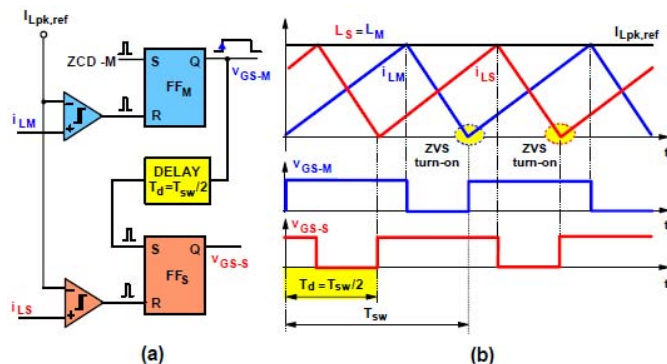


Fig. 3. (a) Basic control circuit and (b) key waveforms of two interleaved DCM/CCM boundary boost PFC converters operating with current-mode control, when the slave is synchronized to the turn-on instant of the master

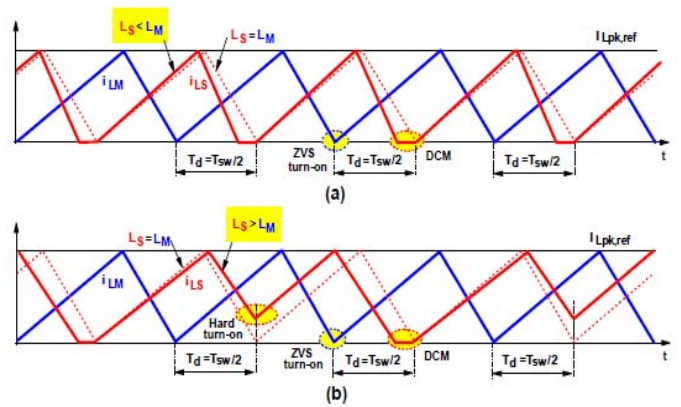


Fig. 4. Inductor current waveforms of the master and slave operating with current-mode control, when the slave is synchronized to the turn-on instant of the master: (a)  $L_S < L_M$ , and (b)  $L_S > L_M$ .

In the more realistic case of inductor mismatch, it is essential to ensure that the slave stage does not work in CCM, which would result in increased switching losses in the mosfet and issues related to the boost diode's reverse recovery. Therefore, the case shown in Fig. 4(b) ( $L_S > L_M$ ) should be prevented and the master inductance should be greater than the slave inductance. In this way, the master stage will still work in ZVS while the slave stage will work in DCM, as shown in Fig. 4(a). To meet this target with no negative impact on the current sharing between the two stages, a good approach is to identify the master and the slave during an initialization phase where the two stages work independently, self-synchronized to the demagnetization of their respective boost inductor. An observer detects which stage is working at the lower frequency and this will be designated as the "master" stage, while the other will be assigned the slave role.

## III. ANALYSIS OF IMPROPER INTERLEAVING

As mentioned in Section I, the real purpose of interleaving is to phase-shift the two individual inductor currents by  $180^\circ$  to minimize the combined current ripple at both the input and the output, with all the resulting benefits. However, all the known synchronization methods [1]-[10] aim to phase shift the gate-drive signals by  $180^\circ$  - not directly the individual inductor currents - assuming that this will indirectly phase shift the individual inductor currents by  $180^\circ$  as well.

In this section is shown that improper interleaving is originated by two major causes: (a) phase-shift  $\neq 180^\circ$  between the gate drive signals, and (b) improper phase shifting between the individual inductor currents even with the gate drive signals properly phase shifted by  $180^\circ$ . These phenomena are more pronounced around the zero crossing of the line voltage.

The following analysis is based on the fact that the switching frequency is much larger than the line frequency. Therefore, both the line voltage and the line current can be considered constant over a switching cycle (quasi-static approximation). As a result, it is possible to consider all the quantities defined on a cycle-by-cycle basis (e.g. the switching frequency, the peak inductor current, etc.), as continuous functions of time or, equivalently, of the instantaneous phase angle  $\theta \in \{0, 180^\circ\}$  of the line voltage.

### A. Interleaving errors due to improper phase-shift between gate-drive signals

One fundamental assumption for proper interleaving with the open-loop control methods is that the duration of two consecutive switching cycles does not change significantly, so that it is possible to use the information obtained in the previous switching cycle to determine the slave's turn-on delay in the present one.

In a line half-cycle, the switching frequency continuously changes, as shown in Fig. 5, at a rate depending on the instantaneous line voltage  $v_{in}$ , its rms value  $V_{in}$  and the load ( $P_{out}$ ). Around zero crossing of the line voltage the switching frequency changes with the fastest rate, dropping to very low values. This is essentially due to the use of correction circuits that reduce the crossover distortion in the line current [11]. In fact, to keep the reference current  $I_{Lpk,ref}$  around zero crossing of the line voltage at a finite value, an offset current:

$$I_o(\theta) = I_{o,pk} (1 - \sin \theta) \quad (1)$$

is added, where the peak amplitude,  $I_{o,pk}$ , is typically a few percent (in this paper, 2.5% is used) of the maximum value allowed for  $I_{Lpk,ref}$ . In this way, the capacitor after the bridge rectifier ( $C_{in}$  in Fig. 1) tends to be depleted almost completely, so that the boost inductor is charged to a finite current with a voltage approaching zero. In a current-mode controlled system, this considerably extends the ON-time of the power switch, sometimes to the point that it is possible to observe the boost inductor ringing with the input capacitor  $C_{in}$  (see the currents at the zero crossing shown on the upper side of Fig. 8). The resulting operating frequency can be very low.

In a line half-cycle, during the  $k$ -th switching cycle of the master stage, the  $k$ -th switching cycle of the slave stage is initiated after a delay  $T_{sw}(k-1)/2$  instead of  $T_{sw}(k)/2$ , resulting in an inherent gate-drive phase error,

$$\Delta\Phi_1(k) = 180 \frac{\frac{T_{sw}(k-1)}{2} - \frac{T_{sw}(k)}{2}}{\frac{T_{sw}(k)}{2}} = -180 \frac{\Delta T_{sw}(k)}{T_{sw}(k)} \quad (2)$$

where  $\Delta T_{sw}(k) = T_{sw}(k) - T_{sw}(k-1)$ . Equation (2) can be re-written in differential terms as:

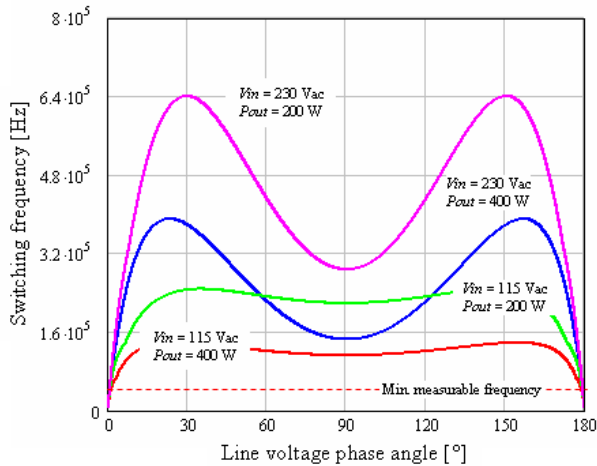


Fig. 5. Switching frequency vs. line voltage phase angle in the master stage of a DCM/CCM boundary boost PFC converter ( $V_{out} = 400$  V,  $L_M = 170$   $\mu$ H).

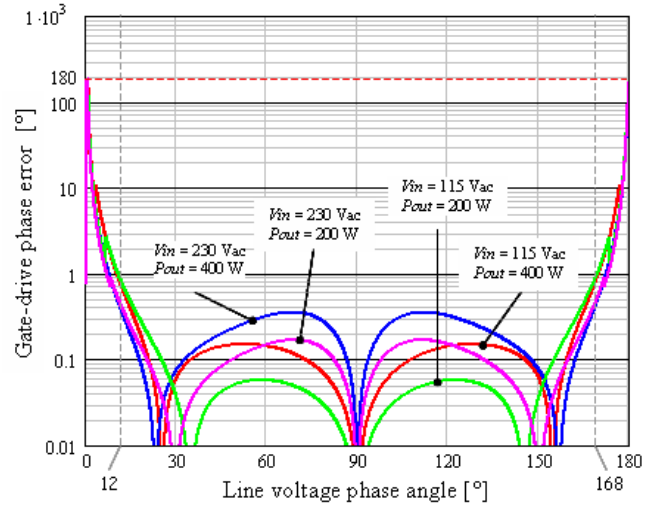


Fig. 6. Gate-drive phase error vs. line voltage phase angle in the slave stage of a DCM/CCM boundary boost PFC converter ( $V_{out} = 400$  V,  $L_M = 170$   $\mu$ H).

$$\Delta\Phi_1(\theta) = -180 \frac{dT_{sw}(\theta)}{T_{sw}(\theta)} \approx -180(2\pi f_L) \frac{dT_{sw}(\theta)}{d\theta} \quad (3)$$

Figure 6 shows how  $|\Delta\Phi_1(\theta)|$  changes over a line half-cycle for different input voltages and load levels. The sign of the phase error can be easily obtained from the slope of the curves in Fig. 5

The amplitude of the phase error is very small ( $< 1^\circ$ ) in the entire line half-cycle, except in a band of about  $\pm 12^\circ$  centered at zero-crossing of the line voltage, where it abruptly becomes very large, consistently with the faster change of the switching frequency, and approaches  $180^\circ$ . In that band, interleaving is completely lost.

All open-loop master-slave synchronization methods use a time measurement system to provide the desired  $180^\circ$  phase-shift between the gate-drive signals. There is an upper limit on the maximum switching period of the master stage that can be measured. For example, in case of analog implementation with a voltage ramp [7], the peak value of the voltage ramp cannot exceed the voltage that supplies the control circuit.

As shown in Fig. 5, around the zero crossing of the line voltage the switching frequency can drop to quite low values, i.e., the switching period can become extremely long. If the switching period exceeds the maximum measurable period  $T_{sw,max}$  (i.e. the switching frequency falls below the "Min. measurable frequency" dotted line in Fig. 5), the delay time of the slave's gate drive signal will be set at the maximum value  $T_{sw,max}/2$ . This delay is shorter than half the master's actual switching period and the resulting phase-shift is  $< 180^\circ$ . Assuming that  $T_{sw}(\theta) \geq T_{sw,max}$ ,

$$\Delta\Phi_2(\theta) = 180 \frac{\frac{T_{sw,max}}{2} - \frac{T_{sw}(\theta)}{2}}{\frac{T_{sw}(\theta)}{2}} = 180 \left( \frac{T_{sw,max}}{T_{sw}(\theta)} - 1 \right) \quad (4)$$

However, if  $T_{sw,max}$  is long enough, e.g. corresponding to a minimum measurable frequency just above the audible range, this error will affect only few switching cycles around the zero crossing.

B. Interleaving errors due to different gate-drive-to-inductor-current phase-shift in master and slave stages

Synchronizing the gate-drive signals with 180° phase-shift to achieve 180° phase-shift in the individual inductor currents relies on the implicit assumption that the same phase relationship exists between the gate-drive signal and the inductor current in both converters. However, this assumption is not exactly true for two reasons.

The first reason can be understood looking at the waveforms in Fig. 4(a), where it is possible to see that locking the turn-on instants in time provides inductor currents that are perfectly phase shifted by 180° in the case  $L_M = L_S$  (red dotted line): both the zeroes and the peaks of the two waveforms are equally spaced in time. In the real-world case  $L_M > L_S$ , the inductor current of the slave stage will reach the peak in a shorter time as compared to the master stage. Therefore, the peaks of the two current waveforms are no more equally spaced in time. This can be considered as a time (phase)-shift between the two waveforms. In fact, when their superposition is considered, it is intuitive that a shift in the individual peaks will affect the result much more than a shift in their zeroes and, therefore, the time (phase) displacement of the peaks can be assumed as a measure for the time (phase) displacement of the waveforms.

It can be concluded that, synchronizing the slave stage to the turn-on instant of the master introduces a leading phase-shift error due to the inductance mismatch of the two boost inductors.

To understand the second reason, we need to review the details of the DCM/CCM boundary mode operation. As the boost inductor demagnetizes, the resonant tank composed of the boost inductor and the total parasitic capacitance of the drain node ( $L_1, C_{D1}$  and  $L_2, C_{D2}$  in Fig. 1) starts oscillating as shown in the timing diagrams of Fig. 7.

Typically, the negative-going edge of the drain voltage is sensed to detect the boost inductor's demagnetization. There is a delay  $T_d$  between the demagnetization instant and the turn-on instant. If  $T_d$  is properly tuned, i.e. it equals half the drain ringing period, the power switch will be turned on with zero or with a minimum drain voltage, depending on whether the instantaneous line voltage  $v_{in}$  is greater or less than half the output voltage  $V_{out}$ .

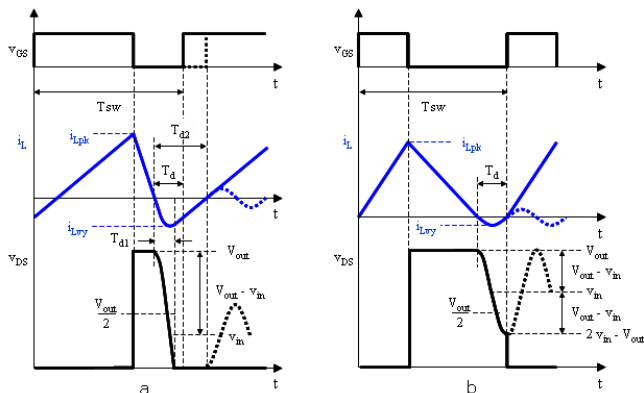


Fig. 7. Key switching waveforms of DCM/CCM boundary operation with valley switching: (a) with  $v_{in} \leq V_{out}/2$ , (b) with  $v_{in} > V_{out}/2$ .

In both cases, the boost inductor current  $i_L$  becomes negative after the demagnetization and has a sinusoidal shape. In case (a), i.e. when  $v_{in} \leq V_{out}/2$ , it is sinusoidal and flows through  $C_{D1,2}$  during time  $T_{d1} < T_d$  necessary for  $v_{DS}$  to decay to zero. Then, immediately after  $T_{d1}$ ,  $v_{DS}$  becomes slightly negative and the body diode of the power switch turns on, clamping  $v_{DS}$  to  $-V_F$ . From  $T_{d1}$  to  $T_d$ ,  $i_L$  flows through the body diode and the voltage across the boost inductor equals  $v_{in} + V_F$ . Therefore,  $i_L$  ramps up linearly as if the power switch were already turned on (at least as long as  $v_{in} \gg V_F$ ). It is possible to prove that  $i_L$  is still negative at  $t = T_d$ , when  $v_{GS}$  goes high and the switch turns on. Note that if  $v_{GS}$  goes high with a delay  $T_{d2}$  after demagnetization (see Fig. 7(a)), the operation and the timing of the circuit are essentially unaffected.

In case (b), i.e. when  $v_{in} > V_{out}/2$ , the negative portion of  $i_L$  after demagnetization is sinusoidal throughout the resonant time interval  $T_d$ , flowing through  $C_{D1,2}$  and becoming again zero at  $t = T_d$ ; the body diode is not turned on.

This negative current at turn-on when  $v_{in} \leq V_{out}/2$  is a key point in determining a different phase relationship between the gate-drive signal and the inductor current in the master and the slave stage around line voltage zero crossing.

In the master stage, where the turn-on instant is determined by the demagnetization sensing, the gate-drive signal  $v_{GS}$  always goes high with a delay  $T_d$  with respect to the instant the inductor current goes to zero and, therefore, the inductor current always starts from  $i_L(T_d)$ . In the slave stage, the turn-on instant is locked in time to that of the master stage but is unrelated to the value of the inductor current. Since in case  $v_{in} < V_{out}/2$  a time interval  $T_{d2} - T_{d1}$  exists where the inductor current  $i_L$  starts rising linearly regardless the gate drive  $v_{GS}$  is high or low, the current in the slave stage at the turn-on instant could assume any value between  $i_L(T_{d1})$  and  $i_L(T_{d2})$ . As the free-running switching frequency of the slave stage is higher, the slave tends to phase-lead the master stage.

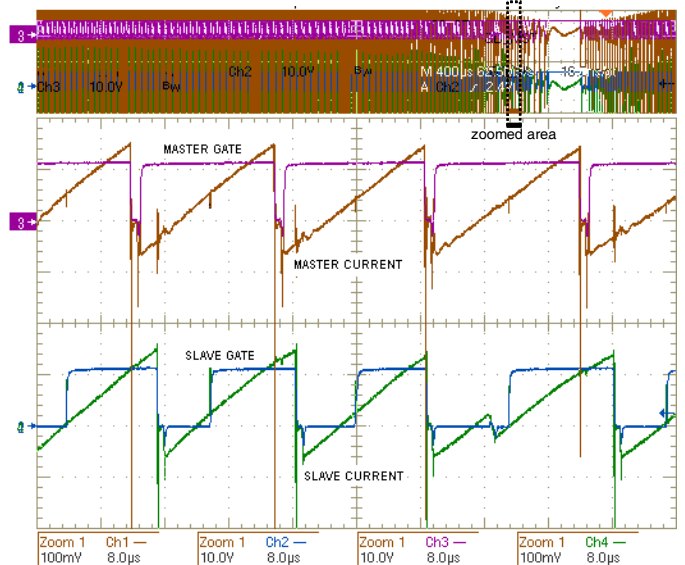


Fig. 8. Master's current and slave's current almost in-phase around zero-crossing of line voltage despite the gate drive signals (rising edges) are 180° out-of-phase. Note the phase mismatch between slave's gate-drive signal and inductor current and the difference in the ON-times of the two gate signals.

As a consequence, the inductor current waveform of the slave stage will be shifted ahead as long as it is allowed by a low gate-drive signal and, therefore, the current at the turn-on instant tends to be  $i_L(T_{d2})$ .

This is apparent in the oscilloscope picture in Fig. 8. Note that in some cycles the gate-drive of the slave stage goes high with a positive inductor current. Actually, if the gate-drive signal is kept low - and the power switch is kept in the OFF state - after  $T_{d2}$  in the case of Fig. 7(a) or after  $T_d$  in the case of Fig. 7(b),  $i_L$  will oscillate around zero and  $v_{DS}$  around  $v_{in}$ , as shown by the dotted lines. Therefore,  $i_L(T_{d2})$  can be greater than zero, and the oscillations of  $i_L$  cause a periodic change in  $i_L(T_{d2})$  and, then, in the phase-shift of the slave current.

The mosfet used as the power switch has a significant role. In fact, its  $C_{oss}$  is one of the components of  $C_{D1,2}$ , in addition to the junction capacitance of the boost diode and the parasitic capacitance of the boost inductor. The conduction of the body diode is also significant. Once it has been turned on at  $t = T_{di}$ , it will conduct until all the electrical charge in its junction capacitance (essentially, its reverse recovery charge  $Q_{rr}$ ) has been removed. This may considerably extend its ability to carry forward current beyond  $t = T_{d2}$ . Therefore, when using mosfets with a fast body diode, lower values of positive current can be observed at turn-on of the slave stage compared to their counterparts with a standard body diode.

As previously mentioned, the phase displacement of the peaks can be assumed as a measure for the phase displacement of the current waveforms. If  $t_{pk,M}(\theta)$  denotes the instant the peak of the master's inductor current occurs in its  $k$ -th cycle,  $t_{pk,S}(\theta)$  denotes the instant of the peak for the slave's inductor current, and  $T_{sw,M}(\theta)$  denotes the duration of the  $k$ -th cycle, the phase-shift of the two current waveforms can be expressed as

$$\Phi(\theta) = 360 \frac{t_{pk,S}(\theta) - t_{pk,M}(\theta)}{T_{sw,M}(\theta)} \quad (5)$$

Using a time scale where  $t = 0$  is the beginning of the  $k$ -th cycle, the instant the peak of the master occurs is

$$t_{pk,M}(\theta) = T_{ON,M}(\theta) \quad (6)$$

Neglecting the phase-shift errors  $\Delta\Phi_1(\theta)$  and  $\Delta\Phi_2(\theta)$  in the gate-drive signals, the instant the peak of the slave occurs is

$$t_{pk,S}(\theta) = \frac{1}{2}T_{sw,M}(\theta) + T_{ON,S}(\theta) \quad (7)$$

where  $T_{ON,M}(\theta)$  is the ON-time of the master stage and  $T_{ON,S}(\theta)$  is the ON-time of the slave stage. Substituting (6) and (7) in (5), it follows that

$$\Phi(\theta) = 360 \left( \frac{1}{2} - \frac{T_{ON,M}(\theta) - T_{ON,S}(\theta)}{T_{sw,M}(\theta)} \right) \quad (8)$$

Note in (8) that the second term in parentheses is the phase-shift error. Based on the previous considerations, it is always  $T_{ON,M}(\theta) > T_{ON,S}(\theta)$  and, therefore, the resulting phase-shift is always less than  $180^\circ$ .

Using an approximation, which is detailed in the Appendix, the phase-shift  $\Phi(\theta)$  given by (8) can be expressed in a way that highlights the origin of the phase-shift error:

$$\Phi(\theta) = 360 \cdot \left[ \frac{1}{2} - \left( 1 - \frac{v_{in}(\theta)}{V_{out}} \right) \cdot \left( 1 - \frac{i_{Lpk}(\theta) - i_{L0,S}(\theta)}{i_{Lpk}(\theta) - i_{L0,M}(\theta)} \cdot \frac{L_S}{L_M} \right) \right] \quad (9)$$

where  $L_S$  and  $L_M$  are the slave and master inductances, respectively;  $v_{in}(\theta) = \sqrt{2}V_{in} \sin \theta$  is the instantaneous rectified line voltage,  $V_{out}$  is the regulated output voltage,  $i_{Lpk}(\theta)$  is the peak inductor current, equal for both stages, whereas  $i_{L0,M}$  and  $i_{L0,S}$  are the values of the master and slave inductor currents at the beginning of their respective ON-times. Therefore,  $i_{L0,M} = i_L(T_d)$  and  $i_{L0,S} \approx i_L(T_{d2})$ , which is close to the worst case.

By setting  $i_{L0,S} = 0$  and  $i_{L0,M} = 0$  in (9), it is possible to find that a mismatch in the inductances inherently produces an improper phase-shift between the individual inductor currents. This phase-shift error increases as the instantaneous line voltage  $v_{in}$  approaches zero. In addition, the different initial inductor currents ( $i_{L0,M} < 0$ ,  $i_{L0,S} \geq 0$ ) further increase the phase-shift error.

The phase-shift between the two current waveforms over a half-line cycle at both  $V_{in} = 115$  Vac and  $V_{in} = 230$  Vac line voltages for the same 400V/400W system, with  $\pm 5\%$  inductance mismatch is shown in Fig. 9. This diagram is obtained by assuming that  $i_{L0,M}$  equals  $i_{Lvy}$  (see Fig. 7) and that  $i_{L0,S} = 0$ .

The phase-shift changes slightly for phase angles ranging from approximately  $30^\circ$  to  $150^\circ$ . At  $V_{in} = 230$  Vac, at portions of the line half cycle where  $v_{in} > V_{out}/2$ , the phase-shift is closer to  $180^\circ$  and is essentially due to the inductance mismatch because  $i_{L0,M}$  and  $i_{L0,S}$  are quite small. At  $V_{in} = 115$  Vac,  $v_{in}$  is always smaller than  $V_{out}/2$ ; therefore, the effect of the different initial currents,  $i_{L0,M} \neq i_{L0,S}$ , is significant and the phase-shift does not exceed  $150^\circ$ .

For phase angles  $< 30^\circ$  and  $> 150^\circ$ , the effect of  $i_{L0,M} \neq i_{L0,S}$  is fairly large and the phase-shift drops considerably, tending to zero at zero crossing.

#### IV. IMPROVED OPEN-LOOP CONTROL METHOD

As shown in (8), the phase-shift error between the master and slave inductor currents is proportional to the difference in the ON-times of the two stages. Therefore, to achieve  $180^\circ$  phase-shift between the individual inductor currents, the turn-on instant of the slave stage should be further delayed after the  $T_{sw,M}/2$  delay, by the difference between the ON-times of the master and the slave. The ON-times need to be measured with the same time scale as  $T_{sw,M}$ . To achieve this, any known technique can be used.

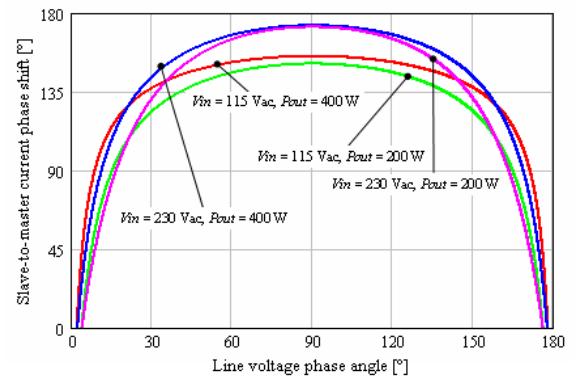


Fig. 9. Master-slave inductor current phase-shift over a half line cycle with a  $\pm 5\%$  inductance mismatch with respect to the nominal value ( $170 \mu\text{H}$ ) in a system designed for 400V/400W output.

An analog implementation with a single-ramp technique is illustrated in Fig. 10(a). Key waveforms are shown in Fig. 10(b). Time is measured by conversion to voltage using voltage ramps generated by capacitors charged with constant current sources. C1 and I1 are used to measure the switching cycle and the ON-time of the master; C2 and I2 are used to measure the ON-time of the slave. Capacitors are matched as well as the current sources, to ensure the same time-to-voltage conversion ratio.

The voltage across C1 is a ramp  $v_{r,M}$  whose peak is sampled and held across C3 at the end of each switching cycle. This voltage, proportional to  $T_{sw,M}$ , is buffered by B1. The value of  $v_{r,M}$  is sampled and held across C4 as  $v_{GS,M}$  goes low. This voltage, proportional to  $T_{ON,M}$ , is buffered by B2. Similarly, the voltage across C2 is a ramp  $v_{r,S}$  whose peak is sampled and held across C6 as  $v_{GS,S}$  goes low. This voltage, proportional to  $T_{ON,S}$ , is buffered by B3.

The block “Summer 1”, generates a voltage proportional to  $T_{ON,M} - T_{ON,S}$  at the output of OP1; the block “Summer 2” provides a voltage  $v_\phi$  proportional to  $T_{sw,M}/2 + (T_{ON,M} - T_{ON,S})$  at the output of OP2. This voltage is compared to the ramp  $v_{r,M}$  in COMP1 and, when they are equal to one another, a “Synch” pulse is generated that asserts  $v_{GS,S}$  high.

## V. SIMULATION RESULTS

To evaluate the effects of the improper interleaving of two DCM/CCM boundary boost PFC converters around zero crossing of the line voltage on the power factor (PF) and total harmonic distortion (THD) of the line current, PSIM simulations were performed on a 400-W/400-V output PFC system with  $\pm 5\%$  inductance mismatch, by using the interleaving circuit in Fig. 10(a).

Simulated individual inductor currents near zero crossing of the line voltage without and with the improved interleaving circuit are presented in Figs. 11(a) and 11(b), respectively.

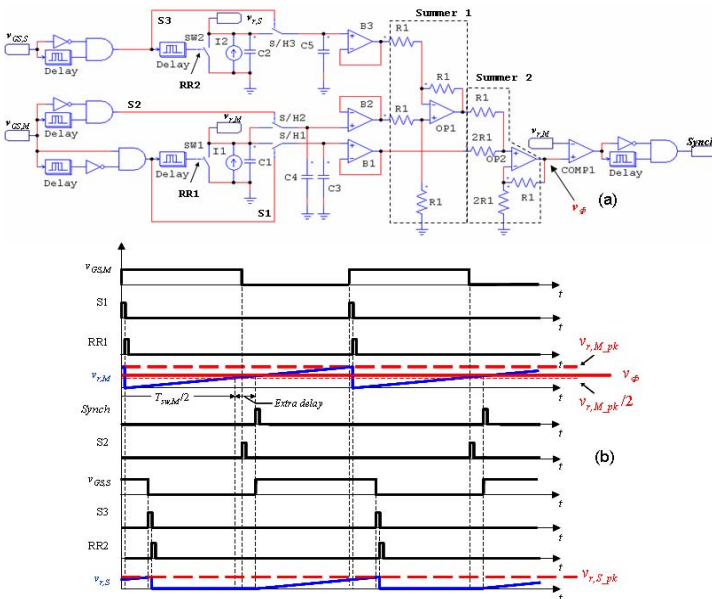


Fig. 10. Implementation of the improved interleaving circuit in analog technology with single-ramp technique: (a) circuit diagram, (b) key waveforms

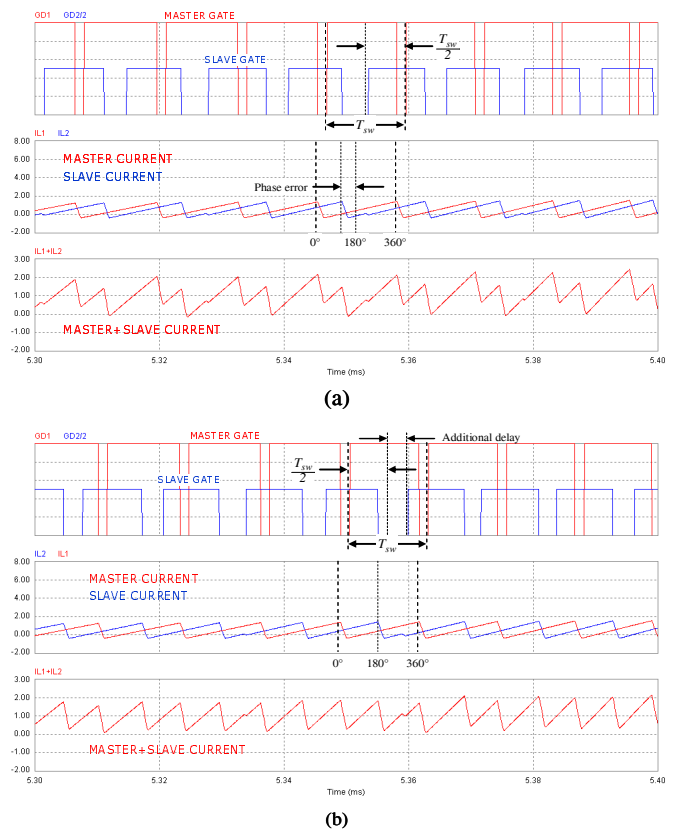


Fig. 11. Simulation results comparing the phase-shift of individual inductor currents around zero crossing of line voltage: (a) standard control method and (b) improved control method (400V/400W output,  $L1 = 178.5 \mu\text{H}$ ,  $L2 = 161.5 \mu\text{H}$ ,  $V_{in} = 115 \text{ Vac}$ ).

In Fig. 11 (a), the improper phase shift between the master and slave inductor currents is apparent, whereas, in Fig. 11(b), the peaks of the master and slave current are properly phase shifted close to  $180^\circ$  and their superposition has significantly lower ripple. Similar results were obtained at other operating conditions and at different phase angles.

PF and THD measurements obtained on the simulated circuit are presented in Table I. It follows from Table I that the PF and THD at nominal low line (115 Vac) and nominal high line (230 Vac) are almost the same with and without the improved interleaving circuit. In fact, the PF and THD with the improved control method are slightly degraded. Therefore, it can be concluded that the improper interleaving around zero crossing of the line voltage does not deteriorate the PF and THD.

TABLE I  
PERFORMANCE EVALUATION OF THE IMPROVED CONTROL METHOD

	Standard control method		Improved control method	
	PF	THD%	PF	THD%
$V_{in} = 115 \text{ Vac}$	0.9989	3.778	0.9987	3.867
$V_{in} = 230 \text{ Vac}$	0.9928	5.070	0.9923	5.129

## VI. SUMMARY

Causes of improper interleaving of two DCM/CCM boundary boost PFC converters around zero crossing of the line voltage are analyzed in details. The converters have a master-slave relationship. The slave is synchronized to the

turn-on instant of the master by using an open-loop interleaving method. It is shown that phase shifting the gate drive signals by 180°, such as in all today's open-loop interleaving methods, does not provide a 180° phase-shift between the individual inductor currents, which is the real objective of interleaving.

Fortunately, the improper interleaving around zero crossing of the line voltage does not deteriorate the power factor (PF) and total harmonic distortion (THD). It is shown that although the interleaving method can be improved to achieve close to 180° phase shift between the master and slave currents even around zero crossing of the line voltage, the improved interleaving has minor effect on the PF and THD. These results were obtained by PSIM simulations.

#### APPENDIX A

With reference to Fig. 12 and using the definitions given in Section III, the ON-time of the master stage is:

$$T_{ON,M}(\theta) = \frac{i_{Lpk}(\theta) - i_{LO,M}(\theta)}{v_{in}(\theta)} L_M \quad (A1)$$

while the ON-time of the slave stage is:

$$T_{ON,S}(\theta) = \frac{i_{Lpk}(\theta) - i_{LO,S}(\theta)}{v_{in}(\theta)} L_S. \quad (A2)$$

Assuming that during the OFF-time the inductor current linearly decreases from  $i_{Lpk,M}$  to  $i_{LO,M}$ , the OFF-time can be expressed as:

$$T_{OFF,M}(\theta) = \frac{i_{Lpk}(\theta) - i_{LO,M}(\theta)}{V_{out} - v_{in}(\theta)} L_M. \quad (A3)$$

This expression slightly underestimates  $T_{OFF,M}$ . By adding (A1) to (A3) the switching period of the master is found:

$$T_{sw,M}(\theta) = [i_{Lpk}(\theta) - i_{LO,M}(\theta)] \left( \frac{1}{V_{out} - v_{in}(\theta)} + \frac{1}{v_{in}(\theta)} \right) L_M \quad (A4)$$

Inserting (A1), (A2) and (A4) in (8), relationship (9) can be obtained after some algebraic manipulations.

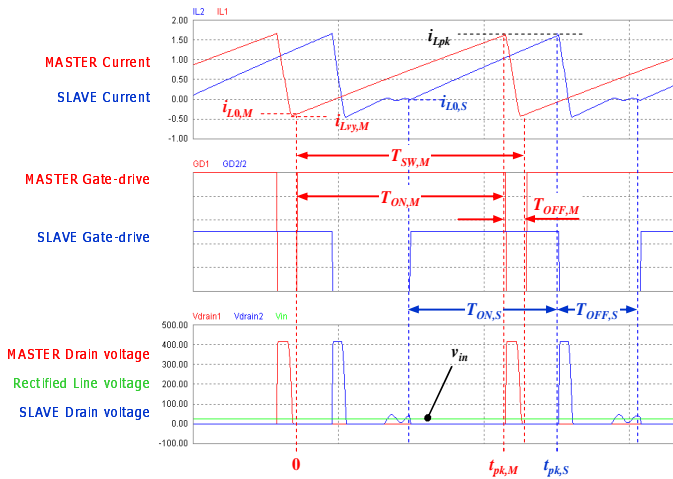


Fig. 12. Diagram showing the definition of the quantities used in the analysis in Section III.

If in (A4)  $i_{LO,M}$  is replaced with  $i_{Lvy,M}$  the approximation will improve: a slight overestimate of  $T_{ON,M}$  tends to compensate  $T_{OFF,M}$ , which becomes less underestimated as well.

The value  $i_{Lvy,M}$  can be easily calculated as:

$$i_{Lvy,M}(\theta) = \frac{v_{in}(\theta) - V_{out}}{Z_{L,M}} \quad (A5)$$

where  $Z_{L,M}$  is the characteristic impedance of the ringing circuit composed of  $L_M$  and the total parasitic capacitance associated to the drain of its mosfet  $C_{D,M}$  (corresponding to  $C_{D1}$  or  $C_{D2}$ , depending on which stage is the master):

$$Z_{L,M} = \sqrt{L_M / C_{D,M}} \quad (A6)$$

In this paper,  $C_{D1,2} = 200$  pF is used.

#### APPENDIX B

Equation (3) can be derived by using the chain rule,

$$\frac{dT_{sw}(\theta)}{T_{sw}(\theta)} = \frac{dT_{sw}(\theta)}{d\theta} \frac{d\theta}{T_{sw}(\theta)} \quad (A7)$$

and observing that between two consecutive switching cycles,  $\theta$  has a small finite change  $\Delta\theta$  proportional to the ratio of the switching cycle  $T_{sw}(\theta)$  and the line cycle  $1/f_L$ :

$$\frac{\Delta\theta}{2\pi} = T_{sw}(\theta) f_L. \quad (A8)$$

Since  $T_{sw}(\theta) f_L \ll 1$ , it is possible to assume  $d\theta \approx \Delta\theta$ .

#### REFERENCES

- [1] J. Zhang, J. Shao, F.C. Lee, and M.M. Jovanović, "Evaluation of input current in the critical mode boost PFC converter for distributed power systems," *IEEE Applied Power Electronics Conf. (APEC) Proc.*, pp. 130-136, Feb. 2001.
- [2] T. Ishii and Y. Mizutani, "Power factor correction using interleaving technique for critical mode switching converters," *IEEE Power Electronics Specialists Conf. (PESC) Proc.*, pp. 905-910, May 1998.
- [3] T. Ishii and Y. Mizutani, "Variable frequency switching of synchronized interleaved switching converters," U.S. Patent 5,905,369, May 18, 1999.
- [4] B.T. Irving, Y. Jang, and M.M. Jovanović, "A comparative study of soft-switched CCM boost rectifiers and interleaved variable-frequency DCM boost rectifier," *IEEE Applied Power Electronics Conf. (APEC) Proc.*, pp. 171-177, Feb. 2000.
- [5] C.M. de Oliveira Stein, J.R. Pinheiro, and H.L. Hey, "A ZCT auxiliary commutation circuit for interleaved boost converters operating in critical conduction mode," *IEEE Trans. Power Electronics*, vol. 17, no. 6, pp. 954-962, Nov. 2002.
- [6] T.F. Wu, J.R. Tsai, Y.M. Chen, and Z.H. Tsai, "Integrated circuits of a PFC controller for interleaved critical-mode boost converters," *IEEE Applied Power Electronics Conf. (APEC) Proc.*, pp. 1347-1350, Feb. 2007.
- [7] L. Huber, B.T. Irving, C. Adragna, and M.M. Jovanović, "Implementation of Open-Loop Control for Interleaved DCM/CCM Boundary Boost PFC Converters," *IEEE Applied Power Electronics Conf. (APEC) Proc.*, pp. 1010-1016, Feb. 2008.
- [8] M.S. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters," *IEEE Applied Power Electronics Conf. (APEC) Proc.*, pp. 152-158, Mar. 1996.
- [9] M.S. Elmore and K.A. Wallace, "Zero voltage switching supplies connected in parallel," U.S. Patent 5,793,191, Aug. 11, 1998.
- [10] A. Jansen, "Master-slave critical conduction mode power converter," U.S. Patent Application 2006/0077604, Apr. 13, 2006.
- [11] C. Adragna, "THD Optimizer Circuits for PFC Pre-regulators," AN1616 STMicroelectronics, Nov. 2002.