

A Comparative Study of a Class of Full Bridge Zero-Voltage-Switched PWM Converters

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Abstract: Four implementations of the full-bridge zero-voltage-switched PWM converter are discussed. The merits and limitations of each implementation are reviewed and their key features and characteristics are compared. In addition, experimental performance comparisons of the four converters were performed on the 1-KW/400-V laboratory prototypes.

I. INTRODUCTION

The phase-shifted PWM full bridge (FB) converter incorporates the leakage inductance of the transformer to achieve zero-voltage switching (ZVS) of the primary switches [1], [2]. The elimination of the need for the primary side snubbers enables high frequency power conversion for high input voltage and high power applications. As a result, the power density and the efficiency of the converter can be improved. However, when ZVS is required over a wide load and/or line range, the leakage inductance is deliberately increased and/or a large external resonant inductor is added, resulting in an excessive duty cycle loss and very severe secondary side parasitic oscillations. These increase primary side conduction losses and the secondary side snubber losses, and therefore decrease the efficiency of the converter.

An improvement can be made by replacing the linear resonant inductor with the saturable inductor and by minimizing the leakage inductance of the transformer [3]. In this implementation, the resonant inductor only stores the necessary energy required for ZVS. Since the duty cycle loss and the ringings on the secondary rectifiers are reduced, the efficiency of the converter can be improved.

Instead of using the energy in the leakage inductance, the magnetizing energy of the power transformer can be utilized to achieve ZVS [4], [5]. Since the leakage inductance can be minimized, the duty cycle loss is negligible, and the parasitic ringing on the rectifiers is very small. Also, ZVS range can be extended to no load.

All of the mentioned methods require an additional energy storage element in the circuit. However, the energy stored in the output inductor can be directly utilized to achieve ZVS by employing two saturable reactors as the secondary side complementary switches [6]-[8]. Because the energy stored in the output inductor is substantial, the ZVS range is widely extended. Also, the secondary parasitic ringing is virtually eliminated because of the use of a very small leakage inductance and because of the damping effect of the saturable reactors.

This paper reviews the operation principles of these four ZVS techniques for implementing FB PWM converters. The characteristics of each method are studied and compared in detail. Finally, the experimental results are presented.

II. REVIEW OF OPERATION PRINCIPLES

Since in the phase-shifted PWM full bridge converter the load current reflected to the primary side is used to achieve the zero-voltage turn on of the leading switches, the realization of ZVS for the leading switches is easy to obtain. Therefore, the discussion in this paper is focused on the realization of the ZVS for the lagging switches. To simplify the discussion, the winding capacitance of the transformer is neglected. The following definitions are used throughout the text:

V_{in} :	input voltage,
N :	transformer turn ratio,
L_{lk} :	leakage inductance of the transformer,
L_m :	magnetizing inductance of the transformer,
L_r :	resonant inductor,
L_{r0} :	unsaturated value of the saturable inductor,
L_f :	output filter inductor,
C_{oss} :	drain-to-source capacitance of one MOSFET at the input voltage,
I_o :	full load current,
I_{ZVS} :	critical output inductor current required by ZVS,
ΔD :	duty cycle loss,
τ_1 :	dead time for the leading leg,
τ_2 :	dead time for the lagging leg,
T_s :	switching period.

A. Basic FB-ZVS-PWM Converter [2]

Figure 1 shows the schematic circuit of the basic FB-ZVS-PWM converter and its theoretical waveforms. S1 and S3 are the leading switches, while S2 and S4 are the lagging switches. D1, D2, D3, and D4 are the body diodes of the MOSFET switches. L_{lk} is the leakage inductance of the transformer, and L_r is the external inductor added to ensure ZVS in a certain minimum load range. In Fig. 1(b), the communication of the lagging switches S2 and S4 occurs at t_3 . Before t_3 , D3 and S2 are on, freewheeling the reflected load current. At t_3 , S2 turns off, enabling $L_r + L_{lk}$ to resonate with the output capacitances C_o of S2 and S4. If the energy stored in L_r and L_{lk} is large enough, the output capacitance of S4 is completely discharged at t_4 , forcing D4 to conduct. Then S4 can be turned on with zero voltage. The same is true for S2 before it is turned on. To ensure ZVS, L_r should satisfy Eq.(1) [2]:

$$\frac{1}{2}(L_{lk} + L_r) \left(\frac{I_{ZVS}}{N} \right)^2 \geq E_{min} = \frac{4}{3} C_{oss} V_{in}^2 \quad (1)$$

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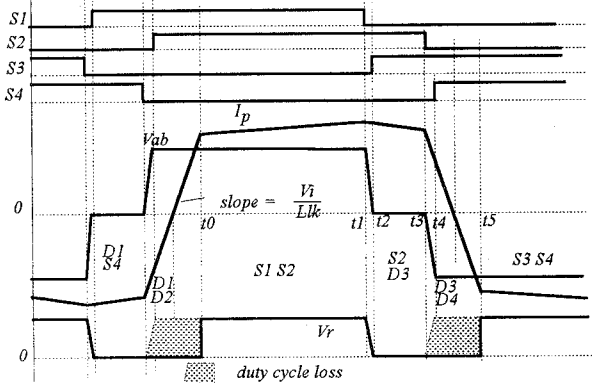
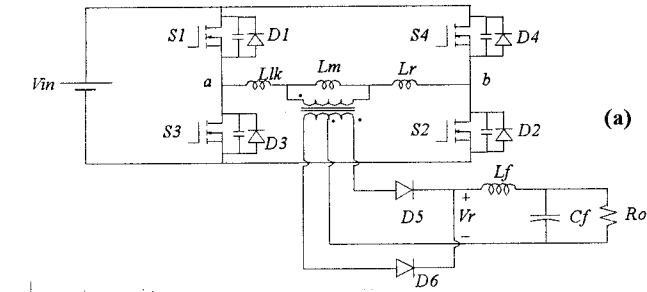


Fig. 1 Basic FB-ZVS-PWM converter: (a) circuit diagram; (b) gate timing and typical waveforms

This circuit absorbs the parasitic inductance to achieve ZVS for the primary switches and requires no additional active devices. Moreover, the presence of the resonant inductor, L_r , reduces the peak reverse recovery current of the secondary rectifiers. The operating frequency can potentially be much higher than that of the conventional hard-switching PWM converter. However, after S2 turns off, the magnitude of the primary current is less than the magnitude of the current through the output inductor. As a result, during the interval $[t_3, t_5]$, both rectifiers D5 and D6 are on, shorting the secondary winding of the transformer. The interval $[t_3, t_5]$ decreases the effective duty cycle on the secondary side (the duty cycle loss is marked by the shadowed area in Fig. 1). To get the same output voltage, the turn ratio of the transformer must be decreased. This increases the primary side conduction loss and the voltage stress on the secondary side rectifiers. In addition, the ripples on the secondary rectifiers become more severe because of the increased energy in the leakage inductance and the external resonant inductor. Damping of this ringing increases the power loss in the circuit.

B. Reducing Duty Cycle Loss by Using Saturable Resonant Inductor [3]

To improve the commutation of the lagging switches in the above discussed circuit, a saturable inductor is employed as the resonant inductor, and the leakage inductance of the transformer is minimized [2]. The circuit diagram and the theoretical waveforms are shown in Fig. 2. The ideal saturable inductance value becomes zero when the current is larger than the critical point, I_{crit} . When S2 turns off at t_3 , the primary current drops to I_{crit} very quickly, and the saturable inductor starts to resonate with the output capacitances of S2 and S4. In the ideal case (where I_{crit} equals I_{zvs}/N), the primary current crosses zero (at t_4) when the output capacitance of S4 has been completely

discharged. Then S4 can be turned on with zero voltage. The primary current continues to decrease until t_5 , when it reaches I_{crit} . At t_5 , the primary current will almost instantly increase to reach the reflected load current, due to the small leakage inductance of the transformer. S2 and S4 then conduct, starting the next half cycle. To guarantee ZVS of the lagging switches, L_{r0} should meet the following requirement:

$$\frac{1}{2}(L_{r0} + L_{lk}) \left(\frac{I_{zvs}}{N} \right)^2 \approx \frac{1}{2} L_{r0} I_{crit}^2 \geq \frac{4}{3} C_{oss} V_{in}^2 \quad (2)$$

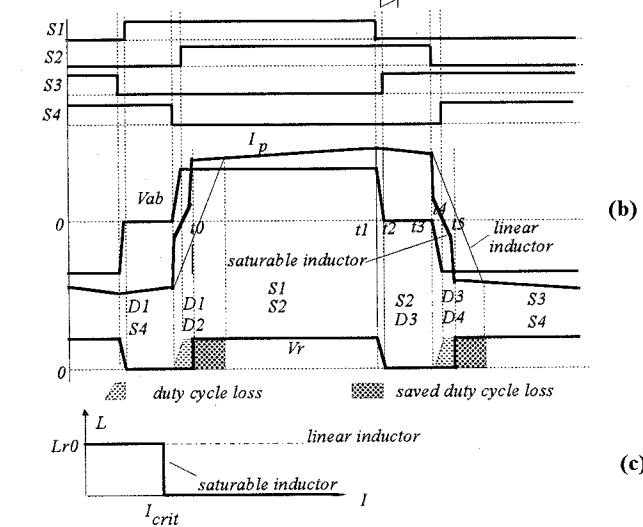
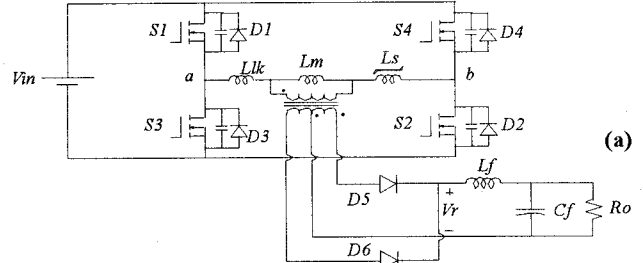


Fig. 2 FB-ZVS-PWM converter employing saturable resonant inductor: (a) circuit diagram, (b) gate timing and typical waveforms, (c) characteristics of ideal saturable inductor

The above expression takes into account the nonlinearity of the drain-to-source capacitance of MOSFET (C_{oss}), as described in [2]. Figure 2 also shows the comparison of the primary current waveforms between the linear resonant inductor case and the saturable inductor case. The duty cycle loss of the circuit with the saturable resonant inductor is much less than that with the linear inductor. Hence the efficiency can be improved, and the ZVS range can be extended by employing the saturable inductor. However, the saturable core placed on the primary side has a thermal problem at high frequency since the flux swings between the positive and negative saturation levels. A possible solution is to place two saturable inductors in series with the secondary rectifiers and to add an additional freewheeling diode [3]. The circuit schematic is similar to that shown in Fig. 3.

C. Full Load Range ZVS by Utilizing the Magnetizing Inductance of the Transformer [5]

Figure 3 shows the schematic circuit of the converter employing the magnetizing inductance and its ideal waveforms. Two saturable reactors are employed as the complementary

switches to utilize the magnetizing current. If the saturable reactors were not employed, the magnetizing current could be used to charge and discharge the output capacitances of the MOSFETs only when it is larger than the reflected load current. However, if the magnetizing current were increased to meet this requirement, it would substantially increase the primary side conduction loss. With the saturable reactors, the magnetizing current does not need to be larger than the reflected load current to achieve ZVS in the full load range. Since there is a dead time between these two magnetic switches, a freewheeling diode must be added. Before t_3 , the primary current freewheels through S2 and D3, while the load current flows through D5 and S5. After S2 turns off at t_3 , the primary current decreases quickly due to the small leakage inductance. On the secondary side, the current flowing through D5 and S5 also decreases, and the freewheeling diode starts conducting. After the primary current decreases to the magnetizing current, the current through the S5 and D5 becomes zero, i.e., S5 turns off. Because S5 and S6 are simultaneously off, L_m can resonate with the output capacitances of S2 and S4. The voltage on S4 decreases to zero at t_4 , forcing D4 to conduct. S4 can then be turned on with zero voltage. The same sequence takes place before S2 is turned on.

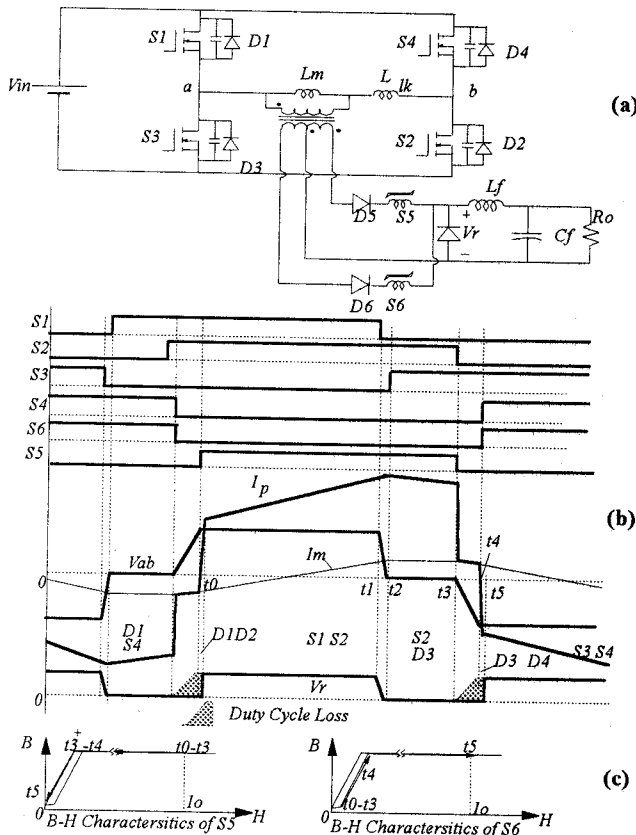


Fig. 3 FB-ZVS-PWM converter employing magnetizing inductance: (a) circuit Diagram, (b) gate timing and typical waveforms, (c) B-H characteristics of saturable reactors

After t_4 , the primary current decreases to the negative reflected load current quickly because L_{lk} is very small. Consequently, the duty cycle loss is very small. The saturable reactors can be implemented on ferrite cores, and they are reset automatically by the circuit itself. Their B-H characteristics are described in Fig. 3(c). The major advantage of this circuit is that ZVS can be achieved at no load. Also, the secondary parasitic

oscillations are greatly reduced because of the very small leakage inductance and the damping effect of the saturable reactors. The potential drawback of this approach is that the deliberately increased magnetizing energy circulates in the primary, resulting in an increased conduction loss.

D. Wide Load Range ZVS by Using Energy in the Output Inductor [6]

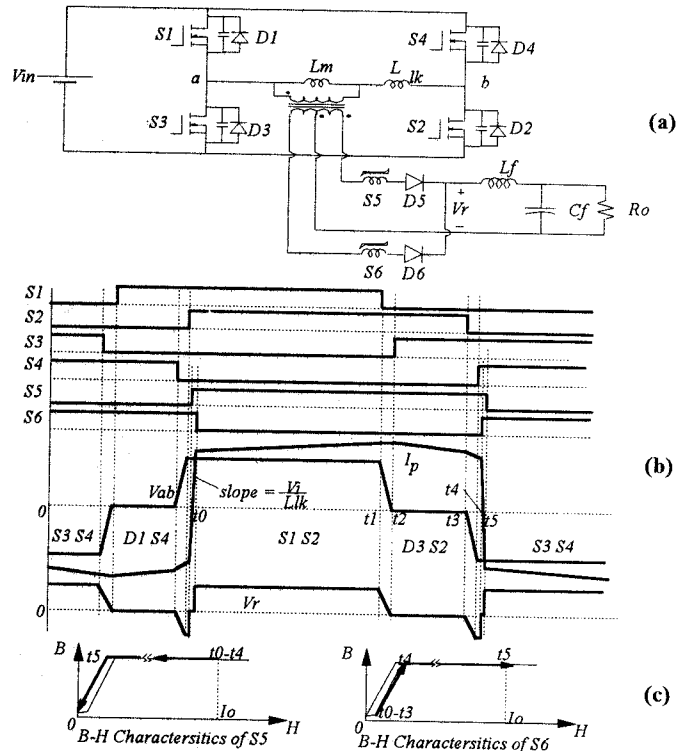


Fig. 4 FB-ZVS-PWM converter employing output inductor: (a) circuit diagram, (b) gate timing and typical waveforms, (c) B-H characteristics of saturable reactors

Instead of using the energy stored in the magnetizing inductance to achieve ZVS, the saturable reactors can be arranged to utilize the energy of the output filter inductor to obtain ZVS. Figure 4 shows the circuit topology and operation waveforms. Before t_3 , on the primary side, S2 and D3 freewheel the reflected load current. On the secondary side, D5 and S5 are on, conducting the load current. At t_3 , the lagging switch S2 turns off. Because of the blocking of S6, the output inductor current has to flow through S5 and D5 branch. This current is reflected to the primary side, charges and discharges the output capacitances of S2 and S4. At some instant between t_3 and t_4 , the voltage across S4 decreases to zero, forcing D4 to conduct. Then S4 can be turned on with zero voltage. After t_4 , S6 becomes on. The load current will commute from the S5 D5 branch to the S6 D6 branch almost instantly because L_{lk} is very small, forcing the primary current to decrease instantly to approximately the negative reflected load current. At t_5 , S5 turns off, starting the next half cycle.

Since in this circuit, there is an overlapping interval when both S5 and S6 are on, no freewheeling diode is needed. The ferrite cores can be used to implement the saturable reactors without any resetting circuit. The B-H characteristics of the cores

are shown in Fig. 4(c). The secondary-side ringings in this circuit are negligible. Consequently, no secondary side snubber is necessary. During [t3, t4], the voltage polarity on the transformer primary winding reverses, and the secondary voltage V_r becomes negative. Therefore, the duty cycle loss is slightly larger than that of the approach employing the magnetizing inductance. But its total duty cycle loss is still small compared to that of the basic FB-ZVS-PWM converter. Because the energy stored in the output choke is substantial, ZVS of the lagging switches is easy to achieve, and the ZVS range can be extended down to very light loads.

III. COMPARISONS OF CHARACTERISTICS

Every ZVS approach reviewed in the previous section has its advantages and disadvantages. Since ZVS range, dead time, and duty cycle loss are the main criteria in the design trade-off of the FB-ZVS-PWM converter, they will be discussed in detail further in this section. In addition, because the circulating energy and the secondary parasitic ringing are directly related to the performance of the circuits, their comparisons are also given. The following discussion is based on the assumption that the same switches, rectifiers, and output filters are used, and that the same maximum duty cycle is adopted. The leakage inductance of the transformer is assumed to be zero, and the winding capacitance is neglected to simplify the discussion. Finally, to make the discussion more convenient, the basic ZVS approach employing the linear resonant inductor will be referred to as approach A, the method employing the saturable resonant inductor as approach B, the ZVS approach employing the magnetizing inductance as approach C, and the method using the output inductor as approach D. However, the nonlinear nature of the drain-to-source capacitance of MOSFET is taken into account.

A. Required Dead Time

In order to achieve ZVS of the primary switches, dead times have to be introduced between the turn on and the turn off of the switches on the same leg. These are shown in Fig. 1 as the time intervals [t1, t2] and [t3, t4]. These two intervals reduce the maximum effective duty cycle available for the power conversion.

In all four approaches, before the leading switch is turned on, its output capacitance is discharged almost linearly by the reflected load current plus the magnetizing current. Because the magnetizing currents in approaches A, B, and D are negligible, the dead times for the leading switches in these three approaches can be determined from Eq. 3 [2]:

$$\tau_1 = \frac{4C_{oss}V_{in}}{I_p/N + I_m} \approx \frac{4NC_{oss}V_{in}}{I_{ZVS}} \quad (3)$$

where I_p corresponds to the minimum peak current of the output inductor and is approximately equal to I_{ZVS} if the ripple of the output inductor current is small enough. For approach C, if ZVS range is required over the whole load range, I_m dominates at no load condition. Then, the dead time for the lagging switch in approach C is determined from

$$\tau_1 = \frac{4NC_{oss}V_{in}}{I_m} \quad (4)$$

The dead times for the lagging switches vary for the different ZVS approaches. For approaches A and B, the output capacitances of the lagging switches are discharged in a resonant

manner. The dead times can be estimated as one fourth of the resonant period [2]:

$$\tau_2 = \frac{\pi}{2} \sqrt{\frac{8}{3} L_r C_{oss}} \quad (5)$$

By applying Eq. (1), Eq. (5) can be written as:

$$\tau_2 = \frac{4\pi NC_{oss}V_{in}}{3 I_{ZVS}} \quad (6)$$

In approach C, which employs the magnetizing inductance, the output capacitance is discharged approximately with constant current, and the dead time for the lagging switches can be estimated as:

$$\tau_2 = \frac{4NC_{oss}V_{in}}{I_m} \quad (7)$$

Similarly, for approach D, the dead time for the lagging switches is determined from

$$\tau_2 = \frac{4NC_{oss}V_{in}}{I_{ZVS}} \quad (8)$$

Though the dead times in approach C are independent of the ZVS range, they may be large because I_m cannot be very large considering the primary-side conduction loss. However, the dead times in the other three approaches are all inversely proportional to I_{ZVS} . When the required ZVS range is wide, the dead times will contribute to a large amount of duty cycle loss, which must be taken into account in the design.

B. Duty Cycle Loss

Compared to the primary side duty cycle, the secondary side effective duty cycle in the phase-shifted FB-ZVS-PWM converter is reduced. In approach A, the difference between the two, referred to as the duty cycle loss, may become significant due to the longer commutation times, [t1, t2] and [t3, t4], for wide ZVS range, and the longer resetting time, [t4, t5], for a large resonant inductor at heavy load. Assuming that the ripple of the output inductor current is negligible, and that I_{ZVS} is much smaller than the full load current, I_o , the duty cycle loss can be estimated from Eqs. (1) and (6) as:

$$\Delta D \approx \frac{2L_r I_o}{NV_{in} T_s / 2} + \frac{\tau_2}{T_s / 2} = \frac{32NC_{oss}V_{in} I_o}{3T_s I_{ZVS}^2} + \frac{8\pi \cdot NC_{oss}V_{in}}{3T_s I_{ZVS}} \propto \frac{I_o}{I_{ZVS}^2} \quad (9)$$

Since in approach B the saturable resonant inductance value becomes zero when the current exceeds the critical point, I_{crit} , the resetting time for the resonant inductor at heavy load is same as that at light loads. Assuming $I_{crit} = I_{ZVS}/N$, the duty cycle loss can be estimated as:

$$\Delta D \approx \frac{L_r I_{crit}}{NV_{in} T_s / 2} + \frac{\tau_2}{T_s / 2} = \frac{16NC_{oss}V_{in}}{3T_s I_{ZVS}} + \frac{8\pi \cdot NC_{oss}V_{in}}{3T_s I_{ZVS}} \propto \frac{1}{I_{ZVS}} \quad (10)$$

Since the duty cycle loss of approach B is only inversely proportional to I_{ZVS} instead of I_{ZVS}^2 , approach B greatly reduces the duty cycle loss compared to approach A.

In approach C, the duty cycle loss caused by the resetting time of the leakage inductance is small because L_{lk} can be very small. When this occurs, the duty cycle loss is dominated by the dead time of the lagging switches and can be estimated as:

$$\Delta D \approx \frac{\tau_2}{T_s / 2} = \frac{8NC_{oss}V_{in}}{T_s I_m} \propto \frac{1}{I_m} \quad (11)$$

Similarly, the duty cycle loss caused by the leakage inductance in approach D is negligible, and the duty cycle loss is

dominated by the dead time of the lagging switches. However, during the switching transient of the lagging switches, the secondary rectified voltage, V_r , is negative. An additional duty cycle loss results. At heavy load (which is the worst case), the duty cycle loss of approach D can be estimated from

$$\Delta D \cong \frac{2\tau_2}{T_s/2} = \frac{16NC_{oss}V_{in}}{T_s I_{zvs}} \propto \frac{1}{I_{zvs}} \quad (12)$$

It can then be seen that the duty cycle loss of approach A is heavily dependent on the ZVS range, while those of approaches B and D are less dependent on the ZVS range, implying that approaches B and D can have higher turn ratios of the transformer and less primary side conduction loss when the ZVS range is wide. The duty cycle loss of approach C is independent of the ZVS range and can be small if I_m is large enough.

C. ZVS Range

As has been discussed previously, different approaches have different duty cycle loss if ZVS ranges are same. Under wide ZVS range, the duty cycle loss of approach A becomes very large, resulting in large primary side conduction loss. So, approach A is not capable of achieving wide ZVS range. On the contrary, approaches B and D have much smaller duty cycle loss, so they can extend ZVS range to light load without increasing the primary conduction loss dramatically. Approach C is the only approach that can achieve ZVS at no load condition. To minimize the primary side conduction loss, the design trade-off between the duty cycle loss and the magnitude of the magnetizing current must be carefully made.

D. Circulating Energy

Referring to the waveforms in Fig. 1, it can be seen that after S3 turns off, the energy stored in the leakage inductance and/or the resonant inductor will flow back to the source. Since it does not contribute to the power conversion, it is referred to as the circulating energy. Though the circulating energy helps soft switching, it also increases the conduction loss in the circuit. In addition, as has been discussed before, the time interval $[t_3, t_5]$ shown in Fig. 1, during which the circulating energy flows back to the source, contributes to the duty cycle loss.

For approach A, the linear resonant inductor stores much more energy than is required for ZVS. This is shown in Fig. 5(a). E_{min} represents the minimum energy required for ZVS. Then the circulating energy of this converter can be estimated as:

$$E_{circ} \cong E_{max} = E_{min} \cdot \left(\frac{I_o}{I_{zvs}}\right)^2 \quad (12)$$

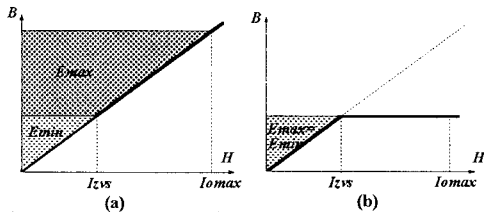


Fig. 5 Stored energy: (a) linear inductor, (b) saturable inductor

On the other hand, an ideal saturable inductor does not store more energy after it is saturated (see Fig. 5(b)). Therefore the circulating energy of approach B is:

$$E_{circ} \cong E_{min} \quad (13)$$

The energy in the magnetizing inductance in approach C is deliberately increased. This energy flows only through the primary winding, never contributing to the power conversion process. The circulating energy of approach C is approximately:

$$E_{circ} \cong \frac{1}{2} L_m I_m^2 \gg E_{min} \quad (14)$$

In approach D, at heavy load, the output capacitance of the lagging switch, S4, is discharged very quickly to zero. However, the saturable reactor S6 still blocks voltage even after D4 is forced on, because S4 is not turned on at this instant. As a result, the energy in the output inductor continues to flow back to the input source. The circulating energy of this converter is estimated as:

$$E_{circ} \cong V_{in} \frac{I_o}{N} \tau_2 = \frac{4I_o C_{oss} V_{in}^2}{I_{zvs}} = E_{min} \cdot 3 \left(\frac{I_o}{I_{zvs}}\right) \quad (15)$$

Approach B has the minimum circulating energy, as can be seen from Eqs. (12) ~ (14). Since the dead time for the lagging leg cannot be too large because of the duty cycle loss, the magnetizing current in approach C should be increased considerably. The circulating energy of this approach is then relatively large. Even though the circulating energy of approach D is more than that required to achieve ZVS, it is still much smaller than that of approach A, if implemented with wide ZVS range. This implies that approach D is more suitable for wide ZVS range applications than approach A.

E. Secondary Parasitic Ringing

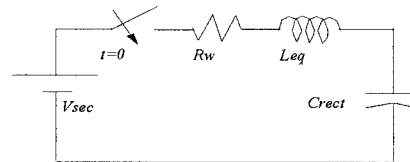


Fig. 6 Equivalent circuit of secondary-side parasitic ringing

In the full bridge converter with an isolation transformer, the junction capacitance of the secondary rectifiers oscillates with the leakage inductance or the resonant inductor in series with the transformer. The equivalent circuit is shown in Fig. 6: R_w is the parasitic resistance; L_{eq} is the equivalent inductor in series with the rectifier; and C_{rect} is the junction capacitance of rectifiers. The amplitude of voltage overshoot on the rectifier increases when the Q factor of the LCR resonant circuit increases. In approach A, the converter employs the large linear resonant inductor; therefore, Q is large. Because of this, a more dissipative snubber is needed to damp out the ringing. To reduce the snubbing power loss, the RCD clamp [9], the primary diode clamp [10] and the active snubber [11] have been implemented. However, if L_{eq} is nonlinear, the maximum energy of the parasitic oscillation is limited by the saturation level of the core. Then the secondary parasitic ringing of approach B is much smaller than that of approach A.

For approaches C and D, two saturable reactors are placed in series with the rectifiers and employed as the complementary switches. Since these saturable reactors do not store any energy, the ringing energy is almost zero. Also, the saturable reactors exhibit high impedance in the "off" state. As a result, the reverse recovery current of the rectifier is not allowed to flow, and the initial current in the LCR circuit shown in Fig. 6 is close to zero. The secondary ringings in approaches C and D are very small.

TABLE 1: SUMMARY OF THE CHARACTERISTICS OF THE DISCUSSED ZVS-PWM FB CONVERTERS

		Basic ZVS	ZVS employing saturable inductor	ZVS employing magnetizing inductance	ZVS employing output inductor
Dead times	τ_1	$\frac{4NC_{oss}V_{in}}{I_{zvs}}$	$\frac{4NC_{oss}V_{in}}{I_{zvs}}$	$\frac{4NC_{oss}V_{in}}{I_m}$	$\frac{4NC_{oss}V_{in}}{I_{zvs}}$
	τ_2	$\frac{4\pi}{3} \frac{NC_{oss}V_{in}}{I_{zvs}}$	$\frac{4\pi}{3} \frac{NC_{oss}V_{in}}{I_{zvs}}$	$\frac{4NC_{oss}V_{in}}{I_m}$	$\frac{4NC_{oss}V_{in}}{I_{zvs}}$
ZVS Range		narrow	wide	from no load to full load	wide
ΔD		$\propto \frac{I_o}{I_{zvs}^2}$	$\propto \frac{1}{I_{zvs}}$	$\propto \frac{1}{I_m}$	$\propto \frac{1}{I_{zvs}}$
Circulating Energy		$E_{min} \cdot \left(\frac{I_o}{I_{zvs}}\right)^2$	E_{min}	$\frac{1}{2} L_m I_m^2 \gg E_{min}$	$E_{min} \cdot 3 \left(\frac{I_o}{I_{zvs}}\right)$
Secondary Ringing		large	smaller	very small	very small
Secondary Side Control		N/A	N/A	Available	Available

F. Secondary Side Control

Approaches C and D employ the secondary side complementary switches, and therefore provide another means of control: secondary side control [4], [5], [7], [8]. If the secondary side switches are implemented on the saturable reactors, magamp control becomes available for approaches C and D. On the contrary, for approaches A and B, only primary side control is available. This implies that approaches C and D are suitable for the multi-output applications.

IV. EXPERIMENTAL COMPARISONS

A. Specifications and Power Stage Design

To experimentally verify and compare the discussed FB-ZVS-PWM implementations, four 1 KW converters were constructed to the following specifications: $V_{in} = 320\text{-}400\text{Vdc}$, $V_o = 48\text{ Vdc}$, $F_s = 100\text{ KHz}$, $D_{max} = 0.95$, and 50% - 100% of full load ZVS range.

Based on the specifications, the power stage components were conservatively chosen: IRFP460 for the power switches, BYV54V200 for the rectifiers, and TDK 3C85-E55 for the transformer cores. The output choke was measured about $17\ \mu\text{H}$ and the output capacitor about $6\ \mu\text{F}$.

In approach A, a linear resonant inductor with the value of $29\ \mu\text{H}$ was employed to achieve ZVS from a 50% load to a full load. Since L_r is fairly large, a very lossy rectifier snubber had to be used: $C_{snub} = 3.9\text{nF}$ and $R_{snub} = 75\ \Omega$.

In approach B, two saturable resonant inductors were placed in series with the secondary rectifiers and a freewheeling diode was added. The PC50 EPC17Z was chosen for the saturable core. A 2-mil air gap was inserted into only one side leg, and a 5 turns winding were placed on the center leg. A smaller snubber was used: $C_{snub} = 680\text{pF}$ and $R_{snub} = 150\ \Omega$.

In approach C, 3-mil air gaps were inserted into the side legs and the center leg of the transformer core. The magnetizing current was not increased dramatically because the critical ZVS current was only 50% of the full load, and the energy in the leakage inductance was utilized. Two saturable reactors were placed in series with the rectifiers, and a freewheeling diode was also added. The saturable reactors were designed by using PC30 T12-3-6 core with 7 turns, and a small RCD clamp was placed across the freewheeling diode.

In approach D, the output inductor was employed to achieve ZVS. Only two saturable reactors were added. They were made

of TDK H5B T14-3.5-7 cores with 8 turns. No snubber was used.

B. Results , Explanations and Comparisons

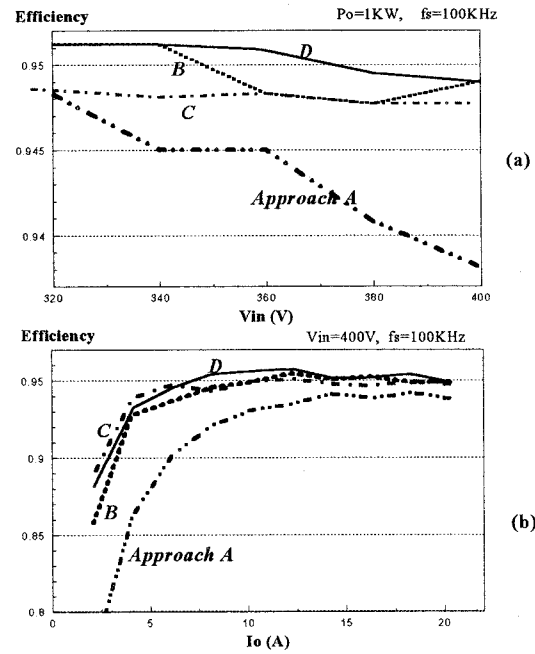


Fig. 7 Measured efficiencies of various implementations of PWM-ZVS-FB converters

- (a) efficiencies vs. input voltage at full power ($P_o=1\text{KW}$)
- (b) efficiencies vs. load current at high line ($V_{in}=400\text{V}$)

Figure 7 shows the measured efficiency of the experimental converters as the functions of the input voltage (Fig. 7(a)) and the load current (Fig. 7(b)). The measurements were done with the same measurement setup to achieve a high accuracy of relative measurements. The efficiency of the basic FB-ZVS-PWM converter is the lowest and decreases at high line or light load. The other three approaches improve the efficiency and keep the efficiency curve flat over a wide line and load range. The efficiency of the converter employing the magnetizing inductance (approach C) is slightly lower, due to its increased rms value of the primary current.

SUMMARY

Four FB-ZVS-PWM converters are reviewed and compared theoretically and experimentally. The basic FB-ZVS-PWM converter is not suitable for applications with wide ZVS range. The other three ZVS techniques improve the circuit performance by reducing duty cycle loss and alleviating secondary side ringing problem without increasing the circuit complexity. Moreover, approaches C and D can implement the secondary-side control, and are therefore suitable for multi-output converter applications.

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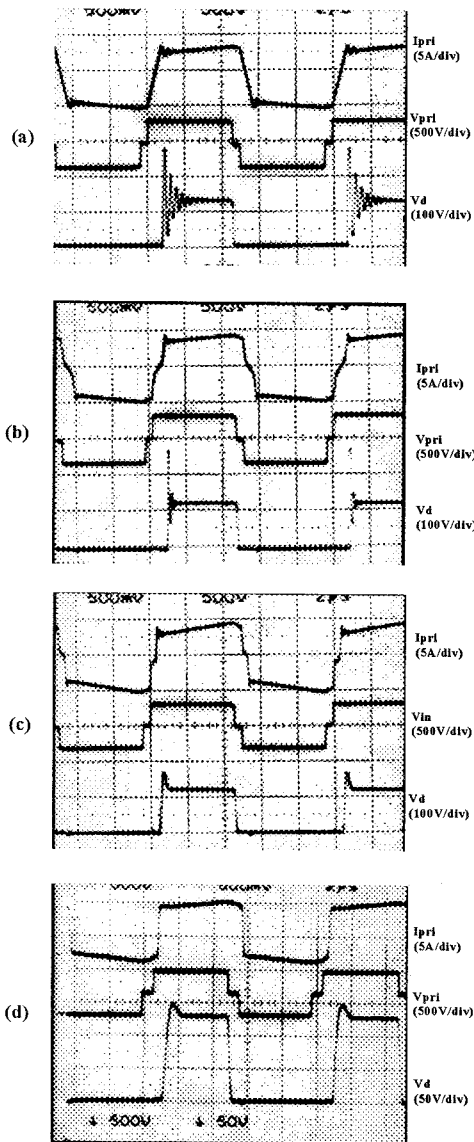


Fig. 8: Key waveforms of various implementations of ZVS-FB-PWM converters. From top to bottom: transformer primary current (I_{pri}), transformer primary voltage (V_{pri}), voltage on the rectifier (V_d)
 (a) ZVS by linear resonant inductor
 (b) ZVS by saturable resonant inductor
 (c) ZVS by magnetizing inductance
 (d) ZVS by reflected output inductor

Figure 8 shows the waveforms of the four converters without the secondary snubbers. However, to prevent a rectifier failure, high voltage rectifiers, BYT230PIV400, were used in these measurements. For the converter using the linear resonant inductor, the ringing on the secondary rectifiers is very severe. However, the ringing on the rectifiers in the circuit using the saturable inductor is much smaller. In the converters employing the magnetizing inductance or the output inductor to achieve ZVS, the secondary ringings are almost eliminated, which verifies the previous theoretical analysis. Comparing the primary currents, we can see that the slope of the primary current of approach C is larger than those of the other three cases because the magnetizing current in approach C is deliberately increased.