Performance Evaluation of Synchronous Rectification in Front-End Full-Bridge Rectifiers

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***Abstract* - In this paper, performance evaluation of synchronous rectification in front-end full-bridge rectifiers is presented. Specifically, the implementation of the full-bridge rectifier with the two diode rectifiers connected to the negative output terminal replaced by two synchronous rectifiers (SRs) and the implementation with all four diode rectifiers replaced by four SRs are considered. In both implementations, the SRs are N-channel MOSFETs controlled by sensing the line voltage. Two methods of line-voltage sensing are presented. First, direct line-voltage sensing, and second, indirect line-voltage sensing, i.e., sensing the line voltage between an input terminal and the negative output terminal. The proposed implementations also include a protection method of preventing accidental short circuit between the input or output terminals. In addition, SR power-management methods such as turning off the SRs at light loads and at no load are provided. The protection of SRs at large inrush currents is also discussed. Experimental results obtained on a 90-W (19.5-V/4.6-A) laptop adapter for the universal line voltage range (90-264 Vrms) are given. In the experimental circuit with four SRs, the efficiency improvement at 90-Vrms line voltage and full load is 1.31%.**

I. INTRODUCTION

Since the turn of the millennium, continuous advancements of power supply technology has enabled remarkable improvements of power densities and efficiencies of ac/dc power supplies for server, networking, and telecom equipment. While a decade ago a typical power density of computer power supplies was around 5 W/in^3 and efficiency in the 75% range, today's state-of-the-art power supplies offer power densities in the 25-35 W/in^3 range and maximum efficiencies in the 94-96 % range. The major driving force behind this extraordinary efficiency improvements have been the 80Plus program [1] and Climate Savers Computing Initiative (CSCI) [2]. The 80Plus program was instrumental in nudging power supply manufacturers to deliver power supplies with efficiencies over 80% in the entire load range from 20% to 100%, whereas CSCI has been essential in pushing power supply efficiencies over 90%.

While initial efficiency improvements have been achieved primarily through topology refinements, advancements in components and materials, as well as better understanding of design optimization trade-offs, more recent efficiency gains has been primarily brought about by improvements in semiconductor components and the employment of power management that has been enabled by digital technology. In fact, further advancements in semiconductor devices, digital control and power management, and packaging techniques will be the key technology areas for achieving efficiencies beyond 94-96% range [3]

In retrospective, the introduction of super junction MOSFETs and SiC rectifiers, as well as the employment of low-voltage MOSFETs with extremely low on-resistances as synchronous rectifiers (SRs) have been the most vital in making possible to achieve efficiencies over 90%. The most significant future incremental efficiency gains in ac/dc power supplies are expected from the introduction of switches made with wide-bandgap materials such as SiC and GaN, in particular, with the introduction of 600-V GaN MOSFETs [4].

Currently, the primary design optimization focus in ac/dc power supplies is on the front-end PFC converter including its EMI filter and energy-storage (bulk) capacitor. With the availability of SiC rectifiers that virtually eliminate the reverse-recovery-related switching losses, the major R&D effort has been directed to further minimization of the conduction losses by integrating the rectifier and PFC functions and minimizing the number of semiconductors in the power processing path. These so-called "bridgeless" PFC boost converters are slowly finding applications in high-end single-phase, ac/dc power supplies, primarily those that need to meet efficiencies above 95% [5].

Because "bridgeless" PFC circuits are implemented with at least two switches, they are more suitable for higher-power applications where multiple switches needs to be also used in the implementation of a conventional PFC front end. At lower power levels, i.e., around 500-600-W and below, where a single switch is typically used, the "bridgeless" technology is less appealing since its implementation requires more components and volume compared to the conventional approach.

Another approach to improve the efficiency of ac/dc power supplies by reducing the conduction loss of the front end is to replace the line-voltage full-bridge rectifier diodes with SRs [6]-[11]. The attractiveness of this approach, in which line-frequency diode rectifiers are replaced by SRs, is in the simplicity of its implementation. Namely, this approach requires minimal modifications of existing designs that should not have any adverse impact on the EMI performance.

The control of the front-end SRs should be as simple as possible yet reliable to prevent accidental short circuit between

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the input or output terminals. Generally, the front-end SRs can be controlled by sensing the line voltage [8] or by sensing the voltage across the SRs [6], [7]. Another control method is by sensing the current through the SRs [10], though, this method is more appropriate for SRs in the output dc-dc converters because of the higher current levels.

In this paper, performance evaluation of synchronous rectification in the front-end full-bridge rectifiers is presented. Specifically, the implementation of the full-bridge rectifier with the two diode rectifiers connected to the negative output terminal replaced by two SRs and the implementation with all four diode rectifiers replaced by four SRs are considered. In addition, two implementations of the control and protection circuit, including a method of preventing accidental short circuit between the input or output of the rectifier and power management of SRs at light loads and no load, are described. The protection of SRs at large inrush currents is also discussed. Finally, the results of experimental performance evaluations obtained on a 90-W (19.5-V/4.6-A) laptop adapter for the universal line voltage range (90-264 Vrms) are given.

II. Review of Existing Implementations of Front-End Synchronous Rectification

The literature on front-end synchronous rectification in switch-mode converters is very scarce [6]-[11]. It is primarily focused on describing SR control implementations and do not offer any systematic assessment of performance improvement. The proposed SR control methods are implemented by considering only operation in steady state. They do not address start-up and transient conditions, power-line disturbances, and operation at light loads and no load.

The control of full-bridge SRs proposed in [6] and [7] is achieved by sensing the voltage across the SRs. All SRs are N-channel MOSFETs, as shown in Fig. 1. The SRs are turned on after their body diode starts to conduct, whereas, the SRs are turned off when the voltage across the SR decreases close to zero. In [6], the control circuit consists of four comparators and three charge-pump circuits for biasing the comparators. Each comparator has a positive bias voltage and operates with a zero threshold voltage (referenced to its bias voltage) at its non-inverting input. During a half-line cycle when a synchronous rectifier is supposed to conduct, the sensed voltage at the inverted input of its comparator is negative, making the output voltage level of the comparator high and the SR is turned on. It should be noted that comparators operating with a positive bias voltage have a very limited range of negative input voltage (typically less than 0.3 V). As a result, the proposed control circuit in [6] is extremely noise sensitive. Another drawback of the proposed control circuit in [6] is that the charge pump circuits for biasing the comparators are linear voltage regulators, which have low efficiency.

In [7], the four SRs are controlled by four SR controller ICs, originally dedicated to control secondary-side SRs such as in flyback and resonant half-bridge topologies. Using secondary-side SR controllers to control front-end SRs requires additional components to accommodate the different operating conditions at the front-end compared to those at the secondary side. In fact, operating at line frequency, the slope of the current through the SR at the zero-crossings of the line voltage is very small, resulting in oscillation of the gate-drive circuit (oscillation between the turn-on and turn-off threshold levels), until the current reaches a decent level, which is sufficient to keep the sensed source-drain voltage above the turn-off threshold level. Another limitation is the maximum value of the sensed drain-source voltage (typically, 200 V). Finally, it should be noted that using two independent controller ICs for each pair of simultaneously conducting SRs is not an optimal approach. Therefore, it can be concluded that the control circuit for the front-end SRs proposed in [7] is not cost effective.

The control of full-bridge SRs proposed in [8], where all SRs are N-channel MOSFETs (as shown in Fig. 1), is achieved by sensing the line voltage indirectly, i.e., by sensing the voltage between an input terminal and the negative output terminal. For example, during a positive half-line cycle, when SRs SR_1 and SR_4 are supposed to conduct, the negative input terminal is connected to the negative output terminal through the conducting SR_4 and the line voltage is sensed by sensing the voltage across SR_2. In [8], only the basic concept is provided, without implementation details.

In [9] and [10], full-bridge SRs, which consist of two N-channel and two P-channel MOSFETs are considered. The two MOSFETs connected to the negative output terminal are N-channel MOSFETs, whereas, the two MOSFETs connected to the positive output terminal are P-channel MOSFETs. It should be noted that by using P-channel MOSFETs as SRs connected to the positive output terminal, the implementation of the gate drive circuit is significantly simpler than by using N-channel MOSFETs. However, P-channel MOSFETs have larger on-resistance compared to the N-channel counterparts. The control of the SRs proposed in [9] is achieved by sensing the line voltage. The control circuit consists of one

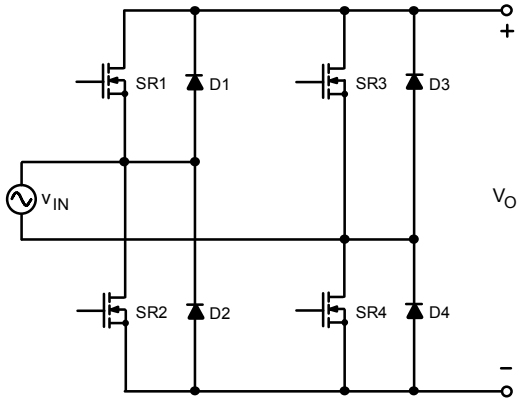

Fig. 1 Circuit diagram of front-end full-bridge rectifier with SRs

comparator and three inverters. Similarly as in [6], the comparator is noise sensitive because it operates with a positive bias voltage and one input voltage is always negative. The bias voltage is equal to the output voltage. It should be noted that the main purpose of the full-bridge SR proposed in [9] is to provide a constant polarity voltage to an electric load from either ac or dc power sources and protect the electric load from an inappropriately applied voltage by switching the applied voltage's polarity. The input voltage of the full-bridge SR proposed in [9] is either a low dc voltage or a low ac voltage obtained from the line voltage through a transformer. Therefore, it can be concluded that the full-bridge SR proposed in [9] is more suitable for low-voltage applications.

The control of the SRs proposed in [10] is achieved by sensing the current through the SRs. In fact, the N-channel MOSFETs are controlled by sensing the current through the body diode or the channel, whereas, the P-channel MOSFETs are directly driven from the ac line by connecting their gates to the appropriate ac input terminal. Therefore, the full-bridge SR proposed in [10] is also more suitable for low-voltage applications.

Finally, the full-bridge rectifier circuit proposed in [11] consists of two rectifier diodes connected to the positive output terminal and two N-channel MOSFETs connected to the negative output terminal. The MOSFETs operate as active switches in the first quadrant of the drain-current – drain-source-voltage plane. Therefore, the full-bridge rectifier circuit proposed in [11] cannot be considered as front-end SR circuit.

III. Efficiency Improvement with SRs

When the front-end diode rectifiers are replaced with SRs, the highest efficiency improvement is obtained at the minimum rms line voltage, V_{INmin}, where the line current has maximum rms value. The loss of the full bridge diode rectifier can be expressed as

$$P_{LossD} = \frac{P_O}{\eta_D \cdot V_{IN\,min}} \cdot \frac{2\sqrt{2}}{\pi} \cdot 2V_D \quad , \qquad (1)$$

where, P_O is the output power, η_D is the efficiency of the converter with front-end diode rectifiers, and V_D is the rectifier-diode forward-voltage drop, which can be approximated as

$$V_D = V_{Dth} + r_D \cdot I_D \quad , \qquad (2)$$

where, V_{Dth} is the threshold of the forward-voltage drop, and r_D is the dynamic forward resistance of the diode rectifier.

When all four rectifier diodes are replaced with SRs, the loss of the SRs can be expressed as

$$P_{LossSR} = \left(\frac{P_O}{\eta_{SR} \cdot V_{IN\,min}} \right)^2 \cdot 2R_{DSon} \quad , \qquad (3)$$

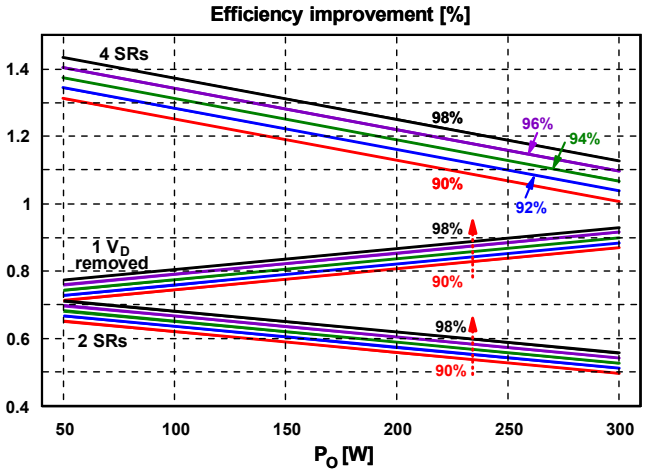

Fig. 2 Calculated efficiency improvements versus output power, at minimum rms line voltage $V_{INmin} = 90\ V_{RMS}$, for five efficiency values of the converter with front-end diode rectifiers

where, R_{DSon} is the drain-source on-resistance of the SR and η_{SR} is the efficiency of the converter with front-end SRs. The efficiency improvement can be obtained as

$$\Delta\eta = \eta_{SR} - \eta_D = \frac{P_O}{\frac{P_O}{\eta_D} - \Delta P_{Loss}} - \eta_D = \frac{\eta_D^2 \cdot \frac{\Delta P_{Loss}}{P_O}}{1 - \eta_D \cdot \frac{\Delta P_{Loss}}{P_O}}, \quad (4)$$

where

$$\Delta P_{Loss} = P_{LossD} - P_{LossSR} \qquad (5)$$

is the loss reduction.

Calculated efficiency improvements versus output power, at minimum rms line voltage $V_{INmin} = 90\ V_{RMS}$, for five efficiency values of the converter with front-end diode rectifiers are presented in Fig. 2. The following parameters of the rectifier diodes and SRs are used: $V_{Dth} = 0.75$ V, $r_D = 50$ mΩ, $R_{DSon} = 0.1$ Ω. The top five lines are for the implementation when all four diode rectifiers are replaced by SRs, whereas, the bottom five lines are for the implementation when only two diodes (connected to the negative output terminal) are replaced by SRs. As can be seen from Fig. 2, with increasing output power the efficiency improvement linearly decreases; and with higher efficiency of the converter with front-end diode rectifiers, the efficiency improvement increases. For example, the efficiency of a 90-W power supply with $\eta_D = 90\%$, can be improved by 1.26% when all four diodes are replaced by SRs.

Fig. 2 also includes the calculated efficiency improvement diagrams in the case when one front-end diode forward-voltage drop is completely removed such as in the case of bridgeless PFC circuits (middle five lines). As can be seen in Fig. 2, with increasing output power, the efficiency improvement linearly increases, which is opposite to the case when the diodes are replaced with SRs. For example, the efficiency of

a 300-W power supply with $\eta_D = 94\%$, can be improved by 0.9% when one front-end diode forward-voltage drop is completely removed. This efficiency improvement is better than the corresponding efficiency improvement when two front-side diodes are replaced by SRs ($\Delta\eta = 0.53\%$). However, it is lower than the corresponding efficiency improvement when all four front-side diodes are replaced by SRs ($\Delta\eta = 1.07\%$).

IV. Implementation

In the circuit diagram of the front-end full bridge rectifier with four SRs (N-channel MOSFETs) shown in Fig. 1, diodes D_1-D_4 represent the body diodes of the MOSFETs or the diodes of the full-bridge diode rectifier. External diode rectifiers should be connected in parallel to SRs in applications with large inrush currents because diode rectifiers can withstand significantly higher surge currents than the body diodes of SRs.

In this paper, the SRs are controlled by sensing the line voltage. Two methods of the line-voltage sensing are presented in Figs. 3 and 5.

In Fig. 3, the block diagram of the SR control circuit with direct line-voltage sensing is shown. The direct line-voltage sensing circuit includes a differential amplifier with level shifting and two comparators (detectors). By using level shifting, the SR control circuit is implemented with only a positive bias voltage. The output voltage of the differential amplifier with level shifting is determined as

$$v_{DIFF} = K_S \cdot v_{IN} + V_{SHIFT} \quad , \qquad (6)$$

where, K_S is the scaling coefficient. It should be noted that by using level shifting, the zero crossings of the line voltage can be very accurately detected. The SRs connected to the negative output terminal are driven by low-side driver circuits, whereas, the SRs connected to the positive output terminal are driven by high-side driver circuit. Key waveforms that illustrate the operation of the circuit in Fig. 3 are presented in Fig. 4.

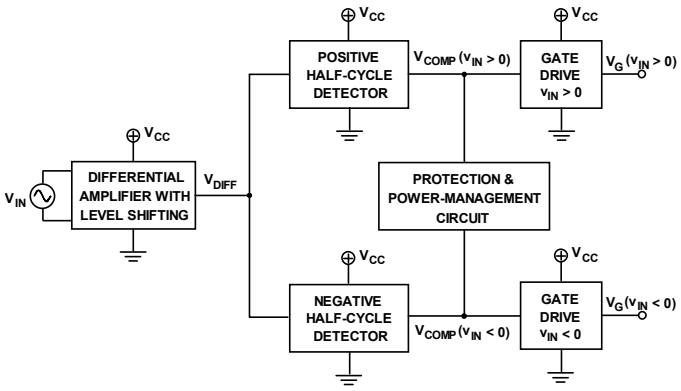

Fig. 3 Block diagram of SR control circuit with direct line-voltage sensing

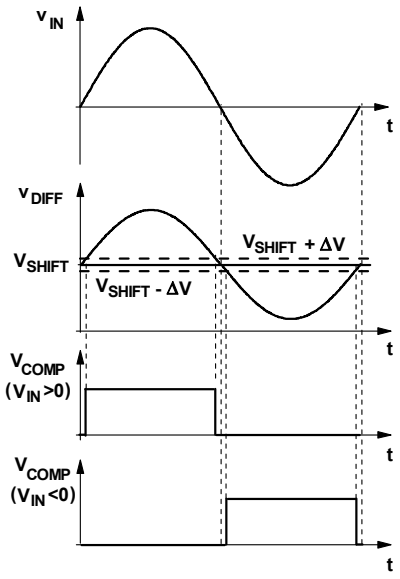

Fig. 4 Key waveforms that illustrate operation of circuit in Fig. 3

The SR control circuit in Fig. 3 also contains a protection and power-management block. The protection circuit prevents improper operation of SRs, i.e., accidental short circuit between the input or output terminals, especially during line and load transients. The power-management circuit is used to improve the efficiency of the power supplies at light loads and no load (when the control loss becomes dominant) by turning off the SRs. Details about the implementation of the protection and power-management block are shown in Figs. 7 and 8.

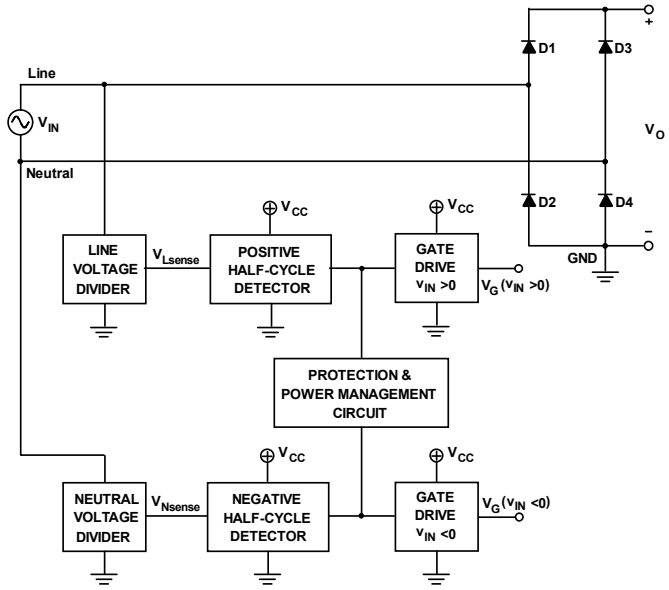

Fig. 5 Block diagram of SR control circuit with indirect line-voltage sensing

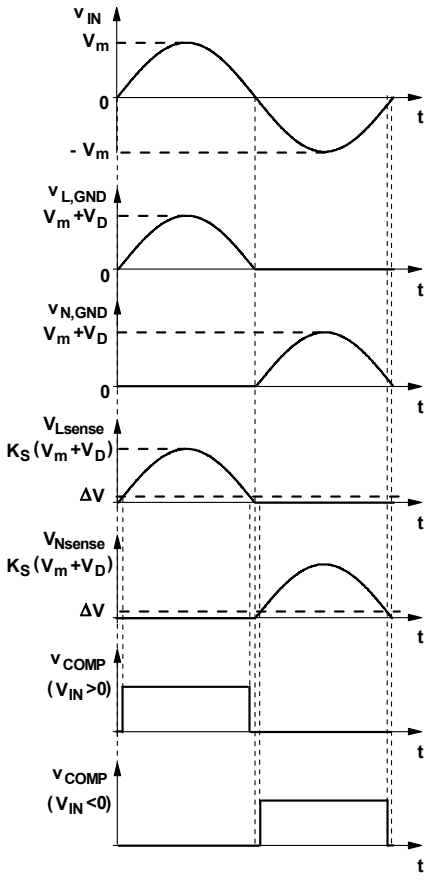

Fig. 6 Key waveforms that illustrate operation of circuit in Fig. 5

The block diagram of the SR control circuit with indirect line-voltage sensing is shown in Fig. 5. Key waveforms that illustrate the operation of the circuit in Fig. 5 are presented in Fig. 6. The indirect line-voltage sensing circuit in Fig. 5 includes two high-voltage dividers and two comparators (detectors). Diodes D_1-D_4 in Fig. 5 represent the body diodes of the SRs or the diodes of the full-bridge diode rectifier. The line voltage sensing is achieved indirectly, i.e., by sensing the voltage between an input terminal (Line or Neutral) and the negative output terminal (GND). For example, during a positive half line cycle, when diodes D_1 and D_4 are supposed to conduct, the Neutral input terminal is connected to the negative output terminal through the conducting diode D_4 and the Line-Neutral voltage is sensed by sensing the voltage across the Line voltage divider. The SR control circuit in Fig. 5 also includes the protection and power-management block, similarly as the SR control circuit in Fig. 3.

An implementation of the SR control circuit in Fig. 5 with two SRs is presented in Fig. 7. The Line-voltage divider consists of resistors R_1 and R_2. When the sensed voltage on resistor R_2 at the non-inverting input of the comparator U_1 becomes greater than the threshold voltage determined by the forward voltage drop of diode D_1, synchronous rectifier SR_1 will be turned on. In order to ensure proper operation around the zero crossings of the line voltage, when the corresponding rectifier diodes are conducting close-to-zero currents, a capacitor is connected in parallel to each SR.

The protection circuit includes MOSFETs Q_3 and Q_4, which are used to cross couple the outputs of the two comparators. Cross coupling the outputs of the two comparators prevents improper operation of the SRs, i.e., accidental short circuit between the input or output terminals.

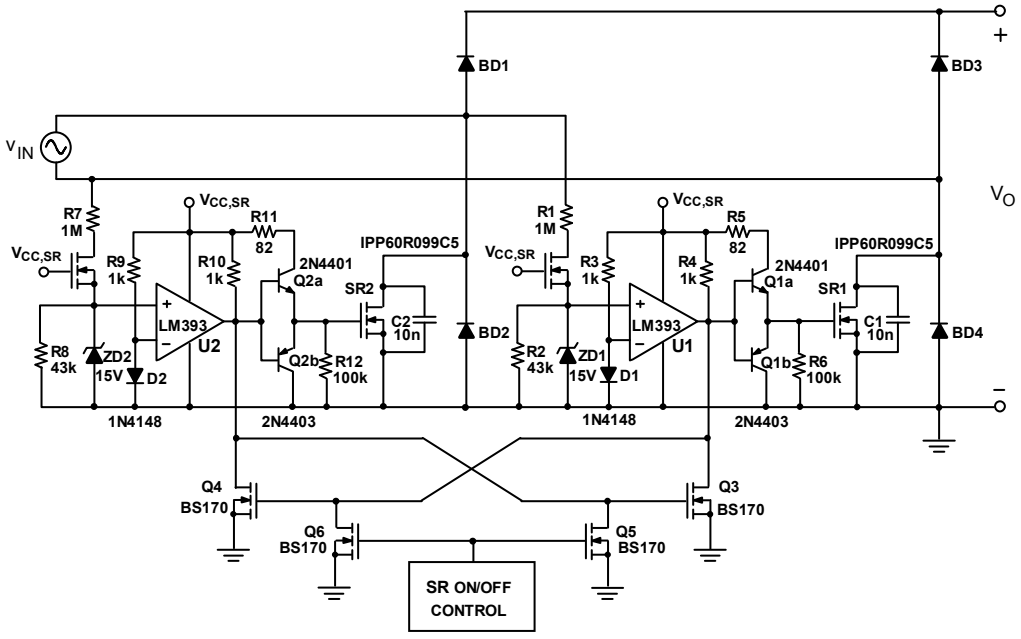

Fig. 7 Implementation of SR control circuit in Fig. 5 with two SRs

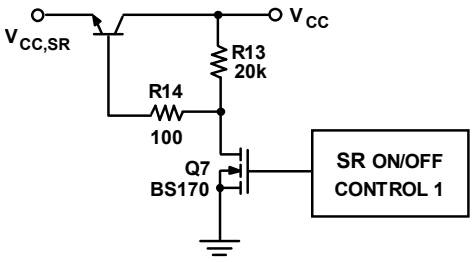

Fig. 8 ON/OFF control of SRs in Fig. 7 by turning ON and OFF the bias voltage of the SR's control circuit

The power-management circuit includes MOSFETs Q_5 and Q_6, which are used to turn off the SRs at light loads and at no load (if necessary) by forcing the output voltage of both comparators to LOW level. In addition, the SRs can be disabled by turning off the bias voltage $V_{CC,SR}$ of the SR's control circuit, as shown in Fig. 8. In order to further reduce the loss of the SR's control circuit when the SRs are disabled, the high-voltage resistive dividers R_1-R_2 and R_7-R_8 can be deactivated through the bias voltage $V_{CC,SR}$, as shown in Fig. 7.

It should be noted that in some low-power, low-cost applications, where inrush-current limiting is not employed, e.g., low-cost laptop adapters, connecting external diode rectifiers in parallel to SRs as shown in Fig. 1 will not be able to protect the SRs. In fact, even if the forward voltage drop of the SR's body diode is greater than the forward voltage drop of the diode rectifier, at large surge currents the forward voltage drop of the diode rectifier will increase above the threshold voltage of the SR's body diode and the SR's body diode will start to conduct and it will take over part of the surge current from the diode rectifier.

In order to protect the SRs without introducing an excessive loss, an active inrush current limiting as shown in Fig. 9 can be employed. During the start-up of the power supply, switch Q_X is open and inrush-current limiting resistor R_X is connected in series with the output capacitor. After the output voltage reaches a predetermined level, switch Q_X turns on. The additional conduction loss of switch Q_X is negligible because the rms current of the output capacitor is small during the steady-state operation.

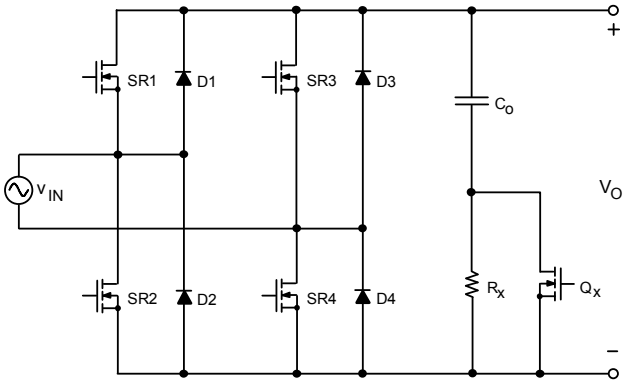

Fig. 9 Protection of SRs with active inrush-current limiting circuit

Finally, it should be noted that the proposed control methods for front-end SRs can be also applied to more advanced PFC circuits such as the bridgeless PFC [5] and the single-stage PFC [12]. For example, the circuit diagram of the bridgeless PFC circuit with return diodes, where SRs are added in parallel to the return diodes is presented in Fig. 10. It follows from Fig. 2, that the efficiency improvement of a, for example, 300-W bridgeless PFC with return diodes and with an efficiency between 96% and 98%, is between 0.54% and 0.56%.

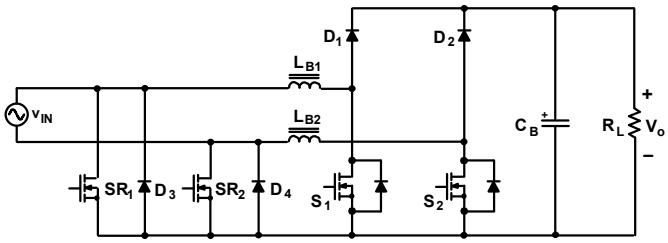

Fig. 10 Circuit diagram of bridgeless PFC with return diodes, where SRs are added in parallel to return diodes

I. Experimental Results

The proposed front-end synchronous rectifiers are experimentally verified on a 90-W (19.5-V/4.6-A) laptop adapter for the universal line voltage range (90-264 Vrms). The front stage of the experimental circuit is a DCM/CCM boundary boost PFC circuit with a full-bridge diode rectifier. The SRs are connected in parallel to the diode rectifiers. Both implementations, with two SRs and with four SRs, were tested.

Efficiency measurements obtained on the experimental circuit with four SRs (IPP60R099C5) controlled by the direct line-voltage-sensing circuit in Fig. 3 are summarized in Table I. The SRs were driven by employing the IR2110 high and low side drivers. As can be seen in Table I, the efficiency improvement at 90-Vrms line voltage and full load is 1.31%, which is in good agreement with the calculated efficiency improvement in Section III.

TABLE I
EFFICIENCY MEASUREMENTS WITH FOUR SRS

V_{in} [V_{rms}]	η_D [%]	η_{SR} [%]	$\Delta\eta$ [%]
90	88.78	90.09	1.31
100	89.44	90.59	1.15
115	90.07	91.05	0.98
132	90.42	91.32	0.90
180	90.68	91.38	0.70
200	90.61	91.25	0.64
230	90.30	90.90	0.60
264	90.10	90.70	0.60

Efficiency measurements obtained on another sample of the 90-W adapter with two SRs (IPP60R099C5) controlled by the indirect line-voltage-sensing circuit in Fig. 7 are summarized in Table II. As can be seen in Table I, the efficiency improvement at 90-Vrms line voltage and full load is 0.5%, which is slightly less than ½ of the corresponding efficiency improvement with four SRs in Table I. Table II also shows the delay time between the SR gate drives. Experimental waveforms of the line-to-ground voltage, neutral-to-ground voltage, and the SR gate drive voltages at 90-Vrms line voltage and full load are presented in Fig. 11.

TABLE II
EFFICIENCY MEASUREMENTS WITH TWO SRS

V_{in} [Vrms]	η_D [%]	η_{SR} [%]	Δη [%]	T_d [µsec]
90	89.07	89.57	0.5	827
100	89.651	90.105	0.454	667
115	90.261	90.666	0.405	627
132	90.657	91.01	0.353	547
180	90.736	90.988	0.252	443
200	90.625	90.858	0.233	391
230	90.43	90.625	0.195	347
264	90.108	90.301	0.193	303

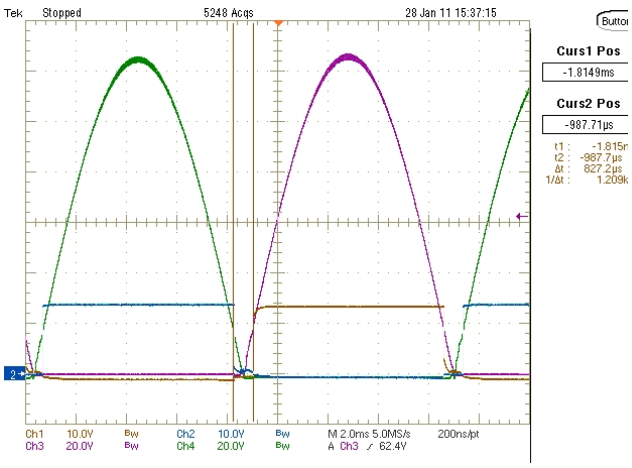

Fig. 11 Experimental waveforms of line-to-ground voltage, neutral-to-ground voltage, and SR gate drive voltages at 90-Vrms line voltage and full load obtained on the experimental adapter with two SRs (IPP60R099C5) controlled by the indirect line-voltage-sensing circuit in Fig. 7

II. SUMMARY

Two implementations of the front-end full-bridge rectifier with synchronous rectifiers (SRs) are presented. In one implementation, four SRs are employed, while in the other implementation, two SRs, which are connected to the negative output terminal, are used. In both implementations, the SRs are N-channel MOSFETs controlled by sensing the line voltage. Two methods of line-voltage sensing are presented. First, direct line-voltage sensing, and second, indirect line-voltage sensing, i.e., sensing the voltage between an input terminal and the negative output terminal. The proposed implementations also include a method of preventing accidental short circuit between the input or output terminals. In addition, SR power management methods such as turning off the SRs at light loads and at no load are provided. The protection of SRs at large inrush currents is also discussed. Experimental results obtained on a 90-W (19.5-V/4.6-A) laptop adapter for the universal line voltage range (90-264 Vrms) are given. In the experimental circuit with four SRs, the efficiency improvement at 90-Vrms line voltage and full load is 1.31% which is in good agreement with the calculated efficiency improvement.

The proposed control methods for front-end SRs can be also applied to other PFC circuits such as bridgeless PFC and single-stage PFC.

REFERENCES

[1] 80 Plus specification (available at http://www.80plus.org/80what.htm)

[2] Climate Savers Computing Initiative, White Paper (available at http://www.climatesaverscomputing.org/docs/20655_Green_Whitepaper_060 1307_ry.pdf)

[3] M. M. Jovanović, "Power conversion technologies for computer, networking, and telecom power systems – past, present, and future," *Proc. Int'l Power Conversion and Drive Conf. (IPCDC)*, St. Petersburg, Russia, June 8-9, 2011, pp. 5-18. (available at http://www.deltartp.com)

[4] Efficient Power Conversion (EPC) http://epc-co.com/epc/DesignSupportbr/TechnicalArchives/Articles.aspx

[5] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electronics*, vol. 23, no 3, pp.1381-1390, May 2008

[6] B. M. Hirst, "Synchronous bridge rectifier," U.S. Patent 6563726, May 13, 2003.

[7] D. Giancomini and L. Chine, "A novel high-efficiency approach to input bridge," *Proc. PCIM Europe Conf.*, 2008.

[8] X. Liu, C. Hu, H. Yue, P. Lin, D. Xu, and H. Pan, "High-efficiency PFC with enabling window control and active input bridge," *Proc. Applied Power Electronics Conf. (APEC)*, pp. 119-124, Mar. 2011

[9] B. K. Kates and J. A. Cummings, "Constant polarity input device including synchronous bridge rectifier," U.S. Patent 6181588, Jan. 30, 2001.

[10] A. Leibovitz, "Bridge synchronous rectifier," U.S. Patent Application 2009/0257259, Oct. 15, 2009.

[11] S. Wong, "Bridge rectifier circuit having active switches and an active control circuit," U.S. Patent 5510972, Apr. 23, 1996.

[12] L. Huber, M. M. Jovanović, and C.C. Chang, "AC/DC flyback converter," U.S. Patent 6950319, Sep. 27, 2005.