A New Three-Phase Two-Switch ZVS PFC DCM Boost Rectifier

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***Abstract*— A new, three-phase, two-switch, power-factor-correction (PFC) rectifier that can achieve less than 5% input-current total harmonic distortion (THD) and features zero-voltage switching (ZVS) of all the switches over the entire input-voltage and load ranges is introduced. The proposed rectifier also offers automatic voltage balancing across the two output capacitors connected in series, which makes it possible to use downstream converters designed with lower-voltage-rated component that offer better performance and are less expensive than their high-voltage-rated counterparts. In addition, the proposed rectifier also exhibits low common-mode EMI noise. The performance of the proposed rectifier was evaluated on a 2.8-kW prototype with a 780-V output that was designed to operate in 340-520-$V_{L-L,\ RMS}$ input-voltage range.**

I. INTRODUCTION

It is well established that three-phase power-factor-correction (PFC) rectifiers with three or more active switches exhibit superior power factor and input-current total harmonic distortion (THD) compared with those implemented with a fewer number of switches, [1]-[15]. However, because the simplicity and low cost of single- and two-switch rectifiers are so attractive, they are increasingly employed in cost-sensitive applications such as, for example, three-phase battery chargers.

Major concerns in three-phase single- and two-switch rectifiers is their relatively low efficiency due to "hard" switching and a relatively high input-current THD because of their inability to actively shape each phase current independently. To address the efficiency issue, various implementations of the three-phase single-switch rectifiers with reduced switching losses were proposed, [2], [5], [6]. Specifically, in the circuits proposed in [2] and [5] resonant techniques are employed to achieve zero-current switching (ZCS) of the switch, whereas in [6], ZCS is achieved by using an active snubber. Generally, all these techniques require additional circuitry that increases their complexity and cost. In addition, the implementations employing resonant techniques suffer from high voltage and/or current stresses.

To improve the input-current THD of the three-phase single- and two-switch rectifiers, a number of harmonic-injection techniques were introduced in [3], [8]-[10]. In [3], a third-harmonic injection technique for two-switch rectifiers was proposed that can reduce line-current THD below 5%, which is a typical requirement for today's rectifiers. However, this technique and its refinements are not quite suitable for implementation in state-of-the-art, high-power density, high-efficiency rectifiers since they require additional components such as low-frequency harmonic filters, or zig-zag autotransformers that have adverse effects on the efficiency, size, weight, and cost. The harmonic-injection techniques for single-switch rectifiers introduced in [8]-[10] do not require additional components since the harmonic injection is solely performed at the control level. While all these techniques are proven to reduce THD without penalizing efficiency, they are not capable of reducing the THD below 5%

Another major concern in the application of three-phase front-end PFC rectifiers that employ the boost topology is the adverse effect of their high output voltage on the cost and performance of downstream converter(s). Namely, for rectifiers operating with a nominal three-phase line-to-line voltage 380/480 V, the output voltage is typically in the 800-V range. Because the majority of high-performance low-cost silicon devices are rated below 650 V and the majority of high-energy-density low-cost aluminum capacitors are rated below 450 V, the high output voltage of the front-stage rectifier dictates the use of relatively inefficient and expensive components in downstream converters, unless the output voltage is divided by two capacitors in series so that low-voltage-rated components in downstream converters can be used. While the split capacitor approach may seem attractive since it eliminates a need for high-voltage-rated components, it is not preferred because it suffers from a voltage imbalance of the split output capacitors. Although there are many techniques that can actively balance the voltages across the split capacitors, those techniques typically require additional sensing components and control loops, which increases the cost and the complexity of their control, [16]-[18].

In this paper, a new, three-phase, two-switch, zero-voltage-switching (ZVS), discontinuous-current-mode

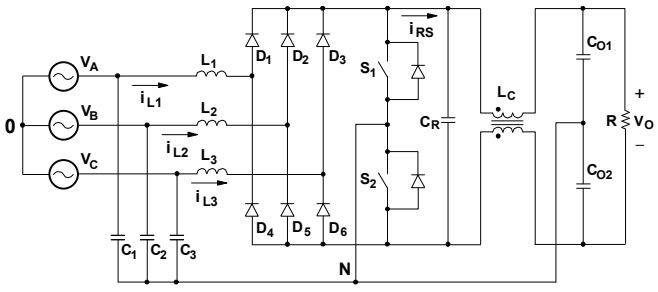


Fig. 1. Proposed three-phase two-switch ZVS PFC DCM boost rectifier.

(DCM), PFC boost rectifier is introduced. The proposed rectifier achieves less than 5% input-current THD over the entire input range and above 20% load and features ZVS of all the switches without any additional soft-switching circuitry. Moreover, the proposed rectifier has automatic voltage balancing across the two output capacitors connected in series. As a result, the voltage across the two output capacitors can be used either as a single high-voltage output or two identical low-voltage outputs, where series connected downstream converters with low-cost high-performance components are employed. In addition, the common-mode electro-magnetic interference (EMI) of the proposed rectifier is quite low. The evaluation of the proposed rectifier was performed on a three-phase 2.8-kW prototype operating in the 340-520-$V_{L\text{-}L,\,RMS}$ line-voltage range.

II. Three-Phase Two-Switch ZVS PFC DCM Boost Rectifier

Figure 1 shows the proposed three-phase two-switch ZVS PFC DCM boost rectifier. In the proposed circuit, the three Y-connected capacitors, C_1, C_2, and C_3, are used to create virtual neutral N, *i.e.,* a node with the same potential as power source neutral 0 that is not physically available or connected in three-wire power systems. Since the virtual neutral is connected to the mid-point between two switches S_1 and S_2 and also to the mid-point of two output capacitors C_{O1} and C_{O2}, the potentials of these two mid-points are the same as the potential of neutral 0 of the balanced three-phase power source.

In addition, by connecting virtual neutral N directly to the mid-point between switches S_1 and S_2, decoupling of the three input currents is achieved. In such a decoupled circuit, the current in each of the three inductors is dependent only on the corresponding phase voltage, which reduces the THD and increases the PF, [11]. Specifically, in the circuit in Fig. 1, bridge diodes D_1-D_6 allow only the phases with positive phase voltages to deliver currents through switch S_1 when it is turned on and allow only the phases with negative phase voltages to deliver currents through switch S_2 when switch S_2 is on. Therefore, the boost inductor in the phase in a positive voltage half-line cycle carries positive current when switch S_1 is on, while the boost inductor in the phase in a negative voltage half-line cycle carries negative current when switch S_2 is on. During the time when switch S_1 is off, the stored energy in the inductor connected to the positive phase voltage is delivered to capacitor C_R, whereas the stored energy in the inductor connected to the negative phase voltage is delivered to capacitor C_R during the time when switch S_2 is off. Because every switching cycle the voltage of each terminal of capacitor C_R changes with a high dV/dt, coupled inductor L_C is connected between "flying" capacitor C_R and output to isolate the output from these fast high-voltage transitions that usually produce unacceptable common-mode EMI noise. With coupled inductor L_C, the output common-mode noise is very low since it is contained in a relatively small area consisting of the S_1-S_2-C_R loop. Moreover, because of the presence of coupled inductor L_C, a parallel operation of multiple rectifiers is also possible.

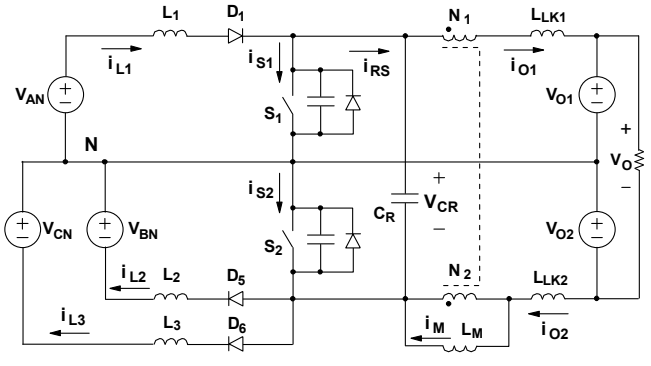


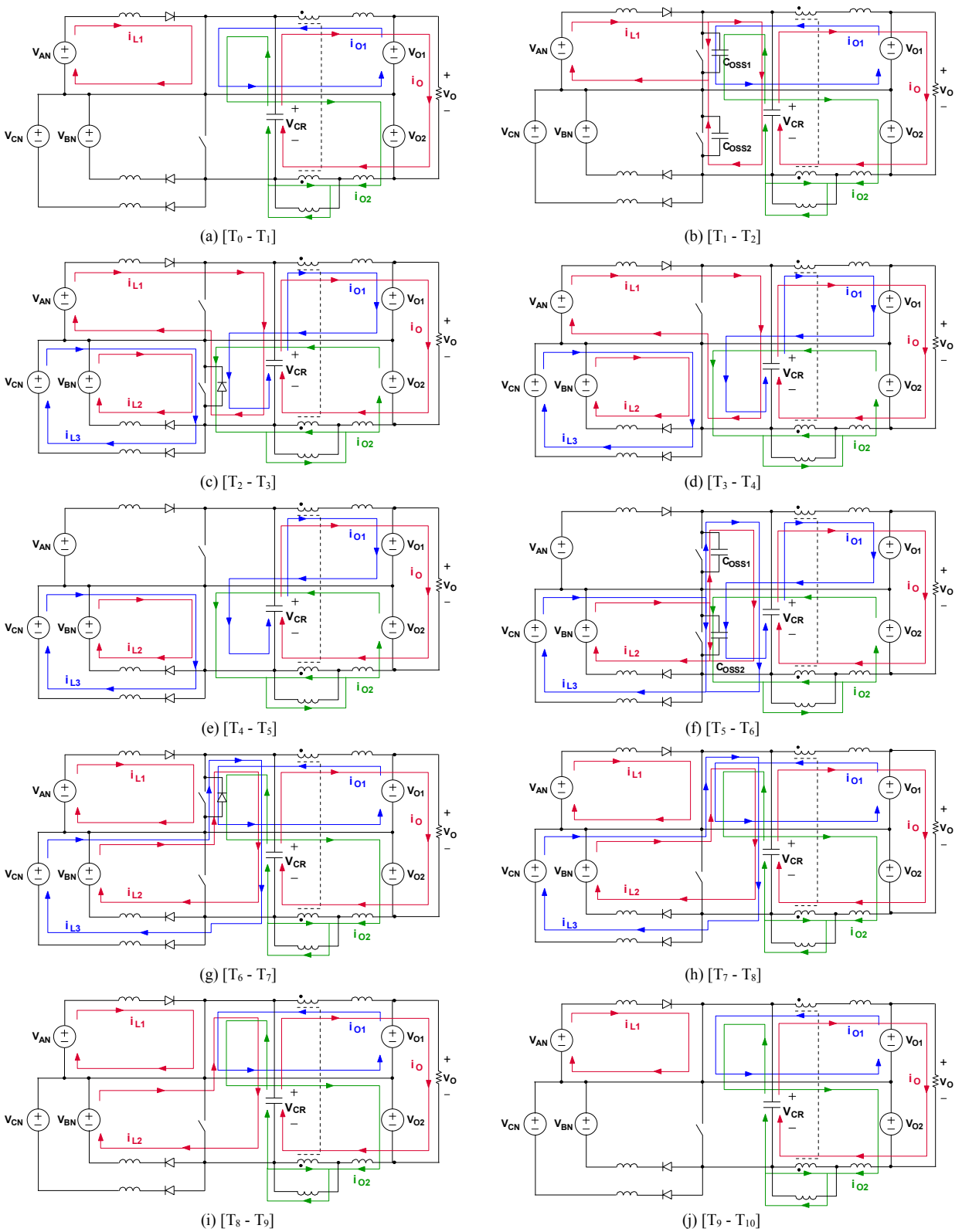
Fig. 2. Simplified circuit diagram of proposed three-phase boost power stage showing reference directions of currents and voltages in 60^0-segment where $V_{AN} > 0$, $V_{BN} < 0$, and $V_{CN} < 0$.

III. Analysis of Operation

To simplify the analysis of operation, it is assumed that ripple voltages of the input and output filter capacitors shown in Fig. 1 are negligible so that their voltages can be represented by constant-voltage source V_{AN}, V_{BN}, V_{CN}, V_{O1}, and V_{O2} as shown in Fig. 2. Also, it is assumed that in the on state, semiconductors exhibit zero resistance, *i.e.*, they are short circuits. However, the output capacitances of the switches are not neglected in this analysis. Coupled inductor L_C in Fig. 1 is modeled as a two-winding ideal transformer with magnetizing inductance L_M and leakage inductances L_{LK1} and L_{LK2}. It should be noted that the average voltage across capacitor C_R is equal to output voltage $V_O = V_{O1}+V_{O2}$. Since in a properly designed rectifier the ripple voltage of capacitor C_R is much smaller than output voltage V_O, voltage V_{CR} across capacitor C_R can be consider constant and equal to V_O.

The circuit diagram of the simplified rectifier along with the reference directions of currents and voltages is shown in Fig. 2. It should be noted that the input model in Fig. 2 is only valid in a 60-degree segment of the line cycle where $V_{AN} > 0$, $V_{BN}<0$, and $V_{CN} <0$. However, the same model is applicable to any other 60-degree segment with a corresponding change of polarities of voltage sources V_{AN}, V_{BN}, and V_{CN}.

To further facilitate the explanation of the operation, Fig. 3 shows topological stages of the circuit in Fig. 2 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams for switches S_1 and S_2 in Fig. 4, the switches operate in a complementary fashion with approximately 50% duty cycle and with a short dead time between the turn-off of switch S_1 and the turn-on of switch S_2, and vice versa. Because of this gating strategy, both switches can achieve ZVS. However, to maintain ZVS for a varying input voltage and/or output load, the proposed rectifier must employ a variable switching frequency control. The minimum frequency is set at full load and minimum input voltage,



(a) [T_0 - T_1] (b) [T_1 - T_2]

(c) [T_2 - T_3] (d) [T_3 - T_4]

(e) [T_4 - T_5] (f) [T_5 - T_6]

(g) [T_6 - T_7] (h) [T_7 - T_8]

(i) [T_8 - T_9] (j) [T_9 - T_{10}]

Fig. 3. Topological stages of proposed boost power stage when $V_{AN} > 0$ and $V_{CN} < V_{BN} < 0$.

whereas the maximum frequency is set at light load and maximum input voltage. The rectifier operates in controlled burst mode at no load or at a very light load to avoid unnecessarily high switching frequency. It should be noted

that other control strategies could also be applied to this circuit, including constant-frequency PWM control. However, with PWM control, ZVS cannot be maintained.

As shown in Figs. 3(a) and 4, before switch S_1 is turned off at $t=T_1$, inductor current i_{L1} flows through switch S_1. The slope of inductor current i_{L1} is equal to V_{AN}/L_1 and the peak of the inductor current at $t=T_1$ is approximately

$$I_{L1(PK)} = \frac{V_{AN}}{L_1} \times \frac{T_S}{2}, \qquad (1)$$

where V_{AN} is line-to-neutral voltage and T_S is the switching period. Because the dead time between turn-off of switch S_1 and turn-on of switch S_2 is very small in comparison with switching period T_S, the effect of the dead time is neglected in Eq. (1), *i.e.,* it is assumed that the duty cycle of switch S_1 is exactly 50%. During the period between T_0 and T_1, current

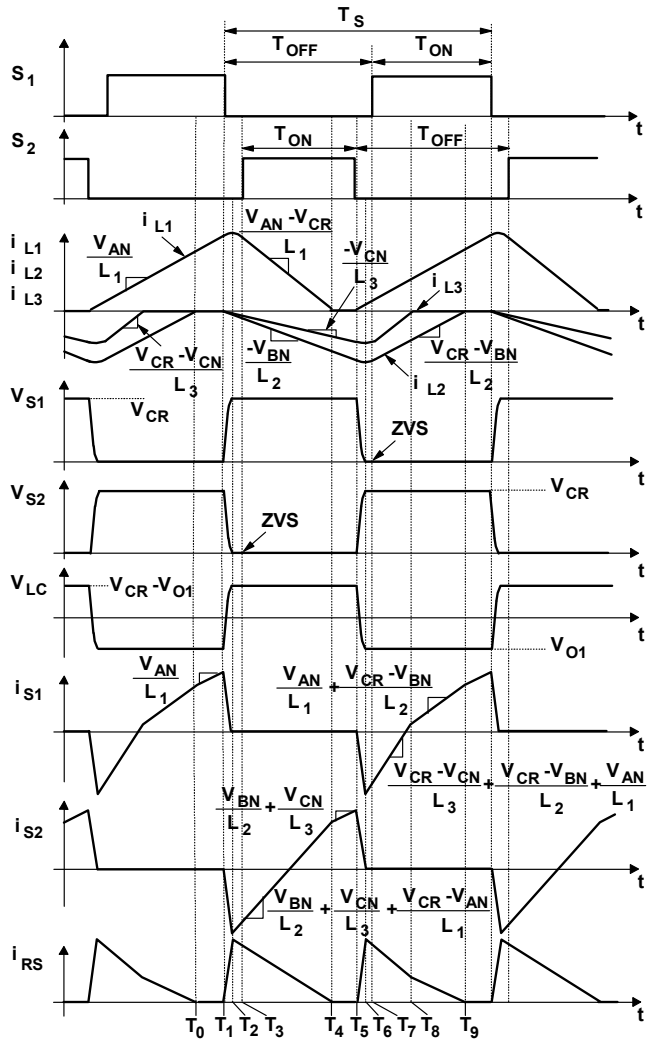


Fig. 4. Key waveforms of proposed boost power stage when $V_{AN} > 0$ and $V_{CN} < V_{BN} < 0$.

i_{O1} decreases with the rate $-V_{O1}/(L_M+L_{LK1})$ while current i_{O2} increases with the rate $(V_{CR}-V_{O1})/(L_M+L_{LK2})$. It should be noted that the magnetizing inductance value of coupled inductor L_C is designed to be sufficiently large so that the ripple current in the coupled inductor does not significantly affect rectifier operation. As shown in Fig. 1 by the "dot" convention, the two windings of inductor L_C are coupled in such a way as to cancel the magnetic fluxes from the differential current of the two windings so that the large magnetizing inductance can be obtained by a small gap in the core without saturation.

At $t=T_1$, when switch S_1 is turned off, inductor current i_{L1} starts charging the output capacitance of switch S_1, Fig. 3(b). Because the sum of the voltages across switch S_1 and switch S_2 is clamped to the "flying" capacitor voltage V_{CR}, the output capacitance of switch S_2 discharges at the same rate as the charging rate of the output capacitance of switch S_1. This period ends when the output capacitance of switch S_2 is fully discharged and the anti-parallel body diode of switch S_2 starts conducting at $t=T_2$, as shown in Fig. 3(c) and Fig. 4. Because the body diode of switch S_2 is forward biased, inductor currents i_{L2} and i_{L3} begin to increase linearly. At $t=T_3$, switch S_2 is turned on with ZVS and inductor currents i_{L2} and i_{L3} are commutated from the antiparallel diode of switch S_2 to the switch, Fig. 3(d). This period ends when inductor current i_{L1} decreases to zero at $t=T_4$. To maintain DCM operation, the time period between $t=T_3$ and $t=T_4$ must be less than one-half of switching period T_S which means that the rising slope of inductor current i_{L1} should be smaller than its falling slope. As illustrated in Fig. 4, the rising and falling slopes of i_{L1} are V_{AN}/L_1 and $(V_{AN}-V_O)/L_1$, respectively. As a result, minimum voltage $V_{CR\,(MIN)}$ across "flying" capacitor C_R, whose average is equal to output voltage $V_{O,}$ is

$$V_{CR(MIN)} = 2 \times V_{AN(PK)} = \frac{2\sqrt{2}}{\sqrt{3}} \times V_{L-L,\,RMS}\,, \qquad (2)$$

where $V_{AN\text{-}PK}$ is the peak line-to-neutral voltage.

It should also be noted that because during the T_2-T_4 interval inductor currents i_{L2} and i_{L3} flow in the opposite direction from inductor current i_{L1}, the average current through switch S_2 is reduced so that the switches in the proposed rectifier exhibit reduced power losses.

During the period between $t=T_4$ and $t=T_5$, inductor currents i_{L2} and i_{L3} continue to flow through switch S_2, Fig. 3(e). The slopes of inductor currents i_{L2} and i_{L3} during this period are equal to V_{BN}/L_2 and V_{CN}/L_3, respectively. The peaks of the inductor currents at the moment when switch S_2 turns off at $t=T_5$ are approximately

$$I_{L2(PK)} = \frac{V_{BN}}{L_2} \times \frac{T_S}{2} \quad \text{and} \qquad (3)$$

$$I_{L3(PK)} = \frac{V_{CN}}{L_3} \times \frac{T_S}{2}. \quad (4)$$

As it can be seen in Eqs. (1), (3), and (4), the peak of each inductor current is proportional to its corresponding input voltage.

After switch S_2 is turned off at $t=T_5$, inductor currents i_{L2} and i_{L3} start to simultaneously charge the output capacitance of switch S_2 and discharge the output capacitance of switch S_1, Fig. 3(f). This period ends at $t=T_6$ when the output capacitance of switch S_1 is fully discharged and its anti-parallel diode starts conducting, Fig. 3(g) and Fig. 4. After $t=T_6$, switch S_1 can be turned on with ZVS. In Fig. 4, switch S_1 is turned on at $t=T_7$. As shown in Fig. 3(h), once switch S_1 is on, increasing inductor current i_{L1} flows in the opposite direction from inductor currents i_{L2} and i_{L3} through switch S_1 so that switch S_1 carries only the difference of current i_{L1} and the sum of currents i_{L2} and i_{L3}. This period ends when inductor current i_{L3} decreases to zero at $t=T_8$. During period T_8-T_9, decreasing inductor current i_{L2} continues to flow through switch S_1, Fig. 3(i). Finally, after inductor current i_{L2} reaches zero at $t=T_9$, a new switching cycle begins, Fig. 3(j).

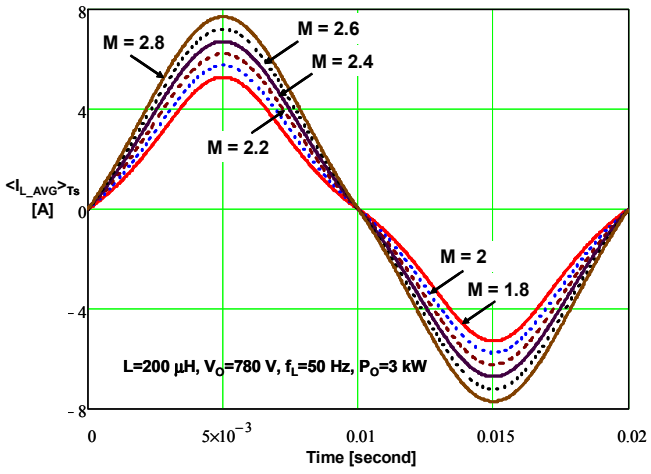


Fig. 5. Calculated average boost inductor current $<I_{L\text{-}AVG}>_{Ts}$ for various input-to-output voltage conversion ratios M.

TABLE I

THD and harmonics of average boost inductor currents shown in Fig. 5.

M	PF	THD [%]	3rd [%]	sum of other harmonics 5th - 99th [%]
1.8	0.989	14.93	14.75	1.14
2	0.992	12.64	12.53	0.67
2.2	0.994	10.97	10.9	0.6
2.4	0.995	9.7	9.65	0.72
2.6	0.996	8.7	8.66	0.78
2.8	0.997	7.89	7.85	0.81

Since in the proposed circuit the charging current of each boost inductor during the time when the related switch is on is proportional to its corresponding phase voltage and its discharging current is proportional to the difference of "flying" capacitor voltage V_{CR} and the corresponding phase voltage, as illustrated in the inductor-current waveforms in Fig. 4, average inductor current $<I_{L\ (AVG)}>_{Ts}$ of each boost inductor during a switching cycle is

$$\left\langle I_{L(AVG)} \right\rangle_{Ts} = \frac{T_S}{8L}\left(\frac{V_{CR} \times \sqrt{2} V_{L-N,\,RMS} \sin \omega t}{V_{CR} - \sqrt{2} V_{L-N,\,RMS} \sin \omega t} \right), \quad (5)$$

where $L= L_1=L_2=L_3$, and ω is the angular frequency of the line voltage.

By defining input-to-output voltage conversion ratio M as

$$M = \frac{V_O}{\sqrt{2} V_{L-N,\,RMS}} \quad (6)$$

and recalling that the average voltage across flying capacitor C_R is equal to output voltage V_O, *i.e.,* $V_{CR} = V_O$, average inductor current $<I_{L\ (AVG)}>_{Ts}$ in Eq. (5) can be rewritten as

$$\left\langle I_{L(AVG)} \right\rangle_{Ts} = \frac{V_O T_S}{8L}\left(\frac{\sin \omega t}{M - \sin \omega t} \right). \quad (7)$$

It should be noted that the expression for average inductor current $I_{L(AVG)}$ in Eq. (7) is exactly the same as that for the average inductor current of the single-phase constant-frequency boost PFC operating in DCM. The current distortion of the average inductor current in Eq. (7) is brought about by the denominator term ($M - \sin\omega t$) and it is dependant on voltage-conversion ratio M. Figure 5 shows calculated average inductor currents $<I_{L\text{-}AVG}>_{Ts}$ for various M, whereas Table I summarizes their harmonic content. As can be seen from Table I, the 3rd harmonic is the dominant distortion component. However, since in the three-wire power systems, the neutral wire is not available (or not connected) the line currents cannot contain the triplen harmonics (the 3rd harmonic and the odd multiples of the 3rd harmonic). Because in the proposed rectifier the triplen harmonics of the inductor currents flow through capacitors C_1-C_3, the proposed circuit exhibits a very low THD and high PF since according to Table I the remaining harmonics contribute less than 1% of total current distortion if M is equal or greater than 2.

Finally, it should be noted that the proposed rectifier automatically balances the voltages across the two output capacitors, *i.e.,* no additional voltage-balancing circuit is

required. Natural voltage-balancing is achieved because in the circuit in Fig. 1 the average voltages across switches S_1 and S_2 are equal to average voltages V_{O1} and V_{O2} across capacitors C_{O1} and C_{O2}, respectively, since the average voltages across the windings of inductor L_C are zero. Because the switches are operated with approximately 50% duty cycle, their average voltages are equal to $V_{CR}/2$ so that $V_{O1} = V_{O2} = V_{CR}/2$.

IV. Experimental Results

The performance of the proposed rectifier was evaluated on a 2.8-kW prototype circuit that was designed to operate from a 340-520 $V_{L\text{-}L,\ RMS}$ three-phase input and with a 780-V output. Figures 6 and 7 show the schematic diagrams and components of the prototype circuit's power stage and EMI filter, respectively.

Because the voltage stress of switches S_1 and S_2 is approximately equal to output voltage V_O, *i.e.,* it is around 780 V, in this wide input-voltage design it is necessary to use switches that are rated at least 950-V to maintain desirable design margin of 20%. As result, in the prototype circuit a CMF20120D SiC MOSFET (V_{DSS} = 1.2 kV, R_{DS} = 0.075 Ω) from Cree was used for each switch. Since input diodes D_1 - D_6 must block the same peak voltage stress and conduct the same peak current (approximately 15 A) as the switches, an

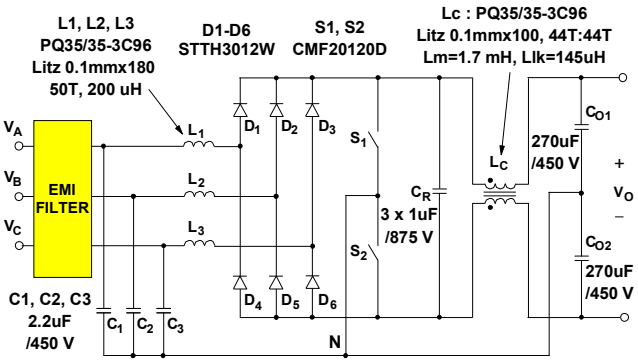


Fig. 6. Experimental prototype circuit of proposed three-phase two-switch ZVS PFC DCM boost rectifier.

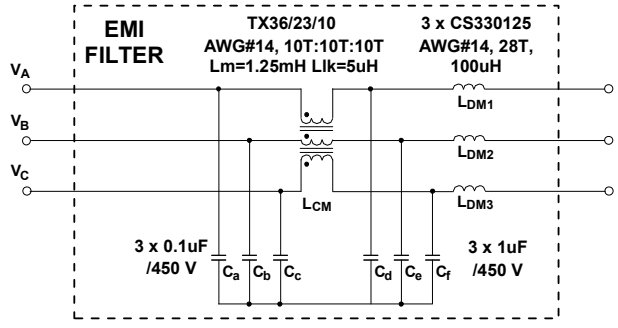
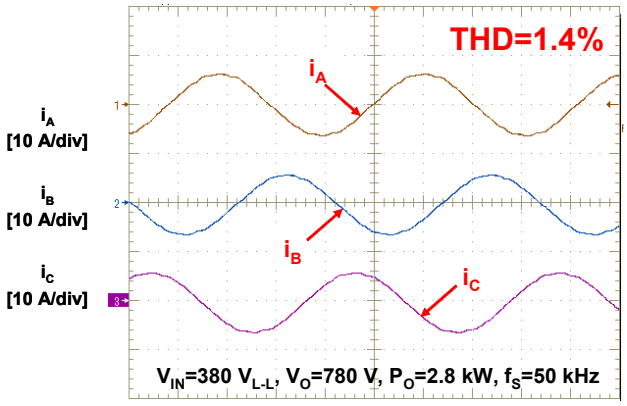
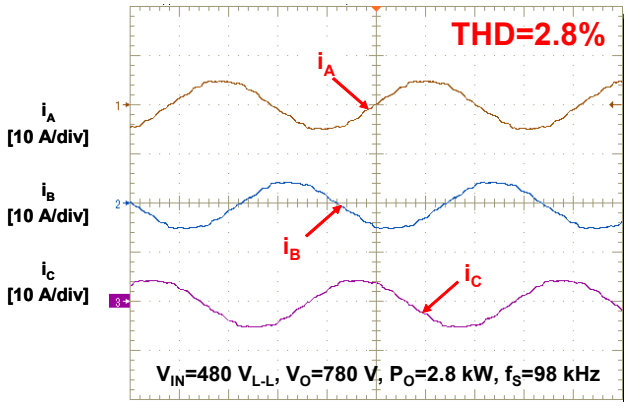


Fig. 7. EMI filter circuit of experimental prototype in Fig. 6.



(a)



(b)

Fig. 8. Measured input current waveforms at full power for input voltages: (a) 380 $V_{L\text{-}L,\ RMS}$; (b) 480 $V_{L\text{-}L,\ RMS}$. Time scale is 4 mS/div.

STTH3012W diode (V_{RRM} = 1.2 kV, I_{FAVM} = 30 A) from ST was used for each diode. To obtain the desired inductance of boost inductors L_1, L_2, and L_3 of approximately 200 µH and also to achieve high efficiency at light-load, each inductor was built using a pair of ferrite cores (PQ-35/35, 3C96) with 50 turns of Litz wire (Φ 0.1mm, 180 strands) and 6.2 mm gap. The Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor core. Coupled inductor L_C was built using a pair of ferrite cores (PQ-35/35, 3C96) with 44 turns of Litz wire (Φ 0.1mm, 100 strands) for each winding and 0.2 mm gap. The measured magnetizing and leakage inductances are 1.7 mH and 145 µH, respectively.

Three parallel connected film capacitors (1 µF, 875 VDC) were used for flying capacitor C_R and a film capacitor (2.2 µF, 450 VDC) was used for each input filter capacitor C_1, C_2, and C_3. Two aluminum capacitors (270 µF, 450 VDC) were used for output capacitors C_{O1} and C_{O2}. Because of additional filtering by the leakage inductance of coupled inductor L_C and capacitor C_R, the RMS current through output capacitors C_{O1} and C_{O2} is quite small. The output voltage across series-connected output capacitors C_{O1}

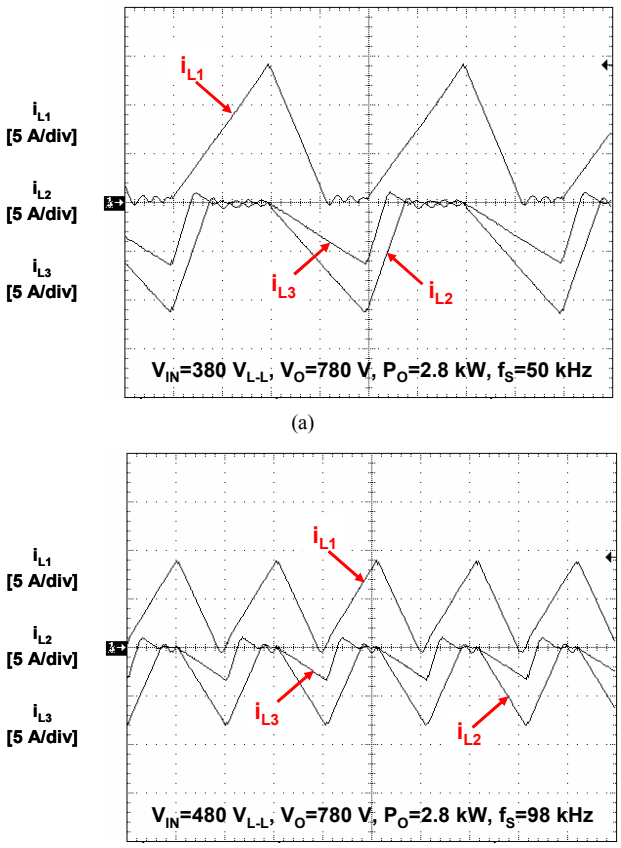


Fig. 9. Measured waveforms of inductor currents i_{L1}, i_{L2}, and i_{L3} at full power for input voltage: (a) 380 $V_{L-L, RMS}$; (b) 480 $V_{L-L, RMS}$. Time scale: 5 µS/div.

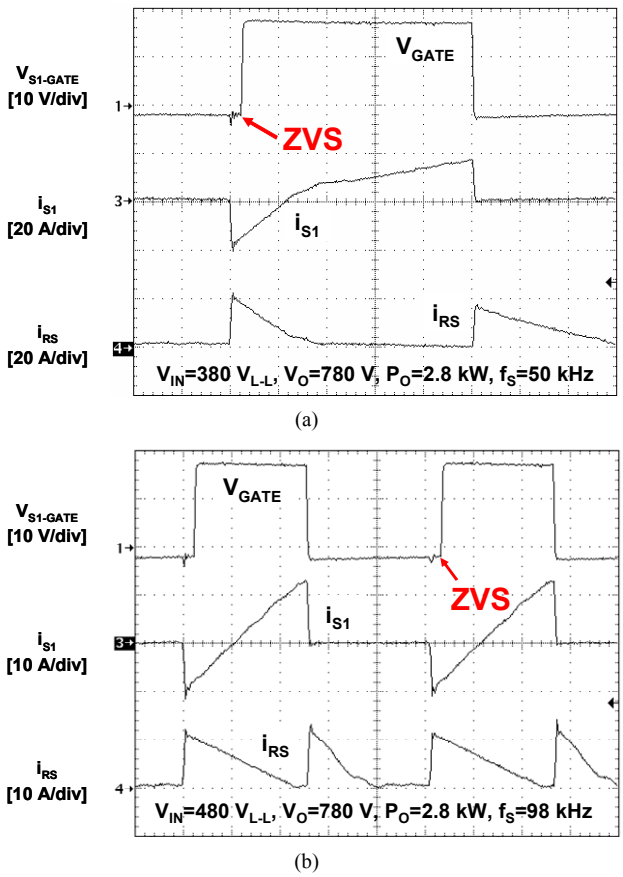


Fig. 10. Measured waveforms of gate voltage V_{GS1} and drain current i_{S1} of switch S_1 and current i_{RS} at full power and input voltage: (a) 380 $V_{L-L, RMS}$; (b) 480 $V_{L-L, RMS}$. Time scale: 2 µS/div.

and C_{O2} was regulated by an L6599 analog LLC controller from ST.

Figure 8 shows the measured full-power input-current waveforms of the experimental circuit at 380 $V_{L-L, RMS}$ and 480 $V_{L-L, RMS}$. The measured THDs of the input currents are approximately 1.4% and 2.8% at 380-$V_{L-L, RMS}$ and 480-$V_{L-L, RMS}$, respectively. Figure 9 shows the measured current waveforms of boost inductors L_1, L_2, and L_3 of the experimental circuit. The measured waveforms and the ideal waveforms in Fig. 4 are in a very good agreement except during the time when the inductor currents are supposed to be zero. The current ringing in the experimental waveforms is caused by the resonance of the boost inductors with the junction capacitance of the non-conducting (reverse-biased) bridge diodes. Although this current ringing adversely affects the THD of the input current, the measured THD was well below 5% over the entire input voltage range and above 20% load. By selecting diodes with smaller junction capacitances, the quality of the input currents can be improved even further. From Fig. 9 it can also be seen that the switching frequencies at full load at 380 $V_{L\_L, RMS}$ and 480 $V_{L\_L, RMS}$ are 50 kHz and 98 kHz, respectively.

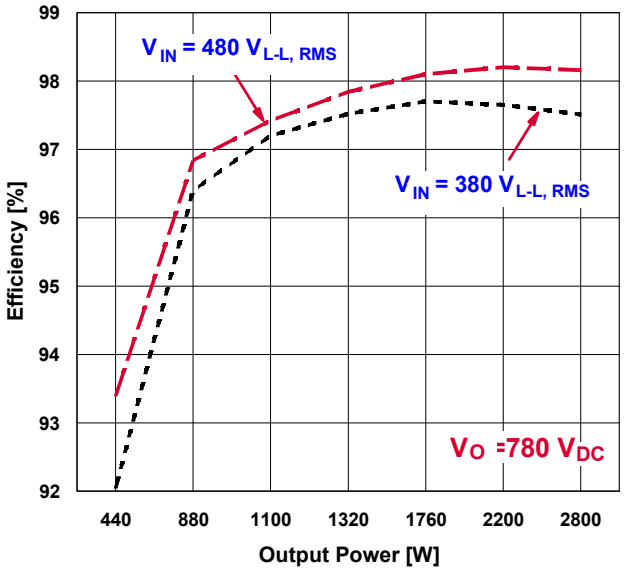


Fig. 11. Measured efficiencies of experimental prototype at nominal voltages as functions of output power.

Figure 10 shows gate-drive voltage V_{GS1} and drain current i_{DS} waveforms of switch S_1 along with the waveform of current i_{RS}. As it can be seen, boost switch S_1 turns on with ZVS because it turns on when the drain current is negative, *i.e.,* while the body diode of switch S_1 is conducting. It was measured that the ZVS of the switches in the experimental circuit maintains over the entire line and load ranges.

Finally, the measured efficiencies of the proposed rectifier at 380 $V_{L\text{-}L,\ RMS}$ and 480 $V_{L\_L,\ RMS}$ as functions of output power are shown in Fig. 11. The measured full-load efficiencies of the rectifier at 380 $V_{L\text{-}L,\ RMS}$ and 480 $V_{L\text{-}L,\ RMS}$ are 97.6% and 98.2%, respectively. It should be noted that the rectifier maintains high efficiency (>97.5%) even at half load.

V. SUMMARY

In this paper, a new three-phase two-switch ZVS PFC DCM boost rectifier has been introduced. The proposed rectifier achieves less than 5% input-current THD over the entire input range and above 20% load and features complete ZVS of the switches. In addition, the proposed rectifier has automatic voltage balancing across the two split output capacitors, which simplifies the implementation of downstream power processing with low-voltage-rated, low-cost, high-performance converters connected across the split capacitors. The performance evaluation was performed on a three-phase 2.8-kW prototype operating in the line voltage range of 340-520-$V_{L\text{-}L,\ RMS}$. The measured input-current THD at 380 $V_{L\_L,\ RMS}$ and 480 $V_{L\_L,\ RMS}$ were 1.4% and 2.8%, respectively. The measured full-load efficiency was in the 97.6-98.2% range.

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