A Novel Active-Current-Sharing Method for Interleaved Resonant Converters

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Abstract—This paper presents a novel active load-current-sharing control of paralleled or interleaved isolated series-resonant converters. In the proposed control method, the output voltage is regulated by variable-frequency control of the converters’ primary switches, while a delay-time control is used to control secondary-side switches provided in place of diode rectifiers to correct load-current imbalance between the converters that is caused by their mismatched components. By independently controlling the turn-off delay time of the secondary switches of each individual converter with respect to the zero-crossing instants of the corresponding resonant-tank current, excellent current balancing can be achieved. The evaluation of the proposed control method was performed on a 1.8-kW prototype that was implemented by two interleaved 900-W series-resonant LLC converters operating from a 240-450-V input-voltage range and providing a 13.8-V output.

I. INTRODUCTION

In series-resonant converters (SRCs), including LLC-resonant converters, the output voltage ripple is determined by the ac-component of the secondary-side rectified resonant current flowing through the output-filter capacitor. As a result, to achieve a low output-voltage ripple in high-current applications, a large output-filter capacitance is required. The output capacitor is typically implemented by paralleling electrolytic capacitors and/or ceramic capacitors. For converter applications that require a relatively long life time such as for example automotive on-board chargers and DC/DC converters, as well as solar inverters and LED drivers, it is not desirable to use electrolytic capacitors because of their relatively short life time [1], [2].

As well known, the output filter capacitance of a converter can be significantly reduced by interleaving, i.e., by paralleling converters and providing a phase shift between their gate-drive signals so that their current ripples at the input and output are greatly reduced. By employing interleaving, resonant converters with a C-type output filter can be designed for high-output-current applications with a reasonable small output filter capacitance. However, interleaving of these variable-frequency controlled resonant converters requires that their switching frequencies are synchronized, i.e., that the converters operate at the same (variable) frequency. However, even with identical input and output voltage and switching frequency, the interleaved resonant converters will not equally share the load current (power) because of inevitable mismatching of their resonant-tank components. Therefore to achieve acceptable current sharing between the interleaved resonant converters with mismatched components, an additional control means independent of switching-frequency control is required.

So far, a number of approaches for interleaved resonant converters have been introduced, [3]-[7]. Specifically, in [3] and [4], the input of each interleaved converter is connected to a separate dc power source (typically the output of the front-end PFC) and the power source voltages, which are the input voltages of the LLC converters, are controlled to achieve and maintain current balance between the interleaved converters. However, this method cannot be applied in applications where only one dc power source is available. The major drawback of the current-balancing methods based on multiphase resonant-converter approaches introduced in [5] and [6] is that they cannot implement phase shedding to maximize light-load conversion efficiency. The current sharing method in [7] employs additional switches to implement a variable resonant capacitor or inductor that can be controlled to compensate for mismatching of components and equalize the resonant frequencies of the interleaved modules. While the current-sharing performance of this approach has been verified, its major drawback is increased complexity and additional cost.

Recently, a new control method of SRCs that regulates the output voltage with a combination of variable-frequency and delay-time control has been introduced [8]. In this method, the variable-frequency control is used to control the primary switches, while delay-time control is employed to control secondary-side switches provided in place of diode rectifiers. Generally, the major feature of the delay-time control is that it alters the dc-conversion ratio of the SRC by giving it boost characteristics. In this paper, the ability of the delay-time control to modify the converter’s characteristic’s is employed to provide active-current-sharing control of interleaved SRCs that allows phase shedding, does not require any additional power-stage components, and is also applicable to a single DC power source input. In the proposed active current-sharing control, the output voltage is regulated by variable-frequency control of the primary switches of paralleled or interleaved converters, while the delay-time control is used to control secondary-side rectifier switches to correct current imbalance between the two resonant converters. By independently controlling the turn-off delay time of the secondary switches of each individual converter with respect to the zero-crossing instants of the
corresponding resonant-tank current, an excellent current balancing can be achieved. The performance evaluation of the proposed active-current-sharing method was done on a 1.8-kW prototype that was implemented by two interleaved 900-W LLC converters operating from the 240-450-V input-voltage range and providing a 13.8-V output.

II. PROPOSED ACTIVE-CURRENT-SHARING METHOD

Figure 1(a) shows two interleaved SRCs with the block diagram of the proposed active-current-sharing control. As shown in Fig. 1(a), the interleaved converters operate with the same switching frequency $f_s$, which is set by the output-voltage controller that includes the output-voltage error amplifier with the compensation circuit and the voltage controlled oscillator (VCO). Frequency $f_s$ at VCO is determined by the output-voltage error amplifier based on the voltage difference between scaled sensed output voltage $V_{O\text{scld}}$ and reference voltage $V_{REF}$. Interleaving is implemented by phase shifting of the control signals of the corresponding primary switches of the two converters by 90°, i.e., by one-quarter of the switching period $T_s/4$, as shown in Figure 1(b).

In the implementation example in Fig. 1(a), the output currents of the paralleled converters are not sensed directly. Instead, the output currents are obtained indirectly from sensed secondary currents $i_{S1}$ and $i_{S2}$. In Fig. 1(a), secondary currents $i_{S1}$ and $i_{S2}$ are rectified and filtered to provide currents $<|i_{S1}|>$ and $<|i_{S2}|>$ which are proportional to corresponding output currents. The differences between currents $<|i_{S1}|>$ and $<|i_{S2}|>$ are processed by the respective current-sharing error amplifier that sets the delay time of the corresponding secondary switches relative to the secondary current zero crossings. Since a typical current mismatch between parallel converters is relatively small, the delay times required for current balancing are also relatively short.

As shown in Fig. 1(b), switches in the same leg of the primary sides of the converters operate in a complementary fashion with a small dead time between their commutations to achieve ZVS. The delay-time control is implemented by delaying the turn-off of switches $S_{S11}$ and $S_{S21}$ of CONVERTER 1 with respect to the corresponding zero crossings of secondary-side resonant current $i_{S1}$ so that both switches $S_{S11}$ and $S_{S21}$ are turned on during delay-time interval $[T_0-T_1]$ shorting the secondary of transformer TR1. Similarly, the turn-off of switches $S_{S12}$ and $S_{S22}$ of CONVERTER 2 is delayed with respect to the corresponding zero crossings of secondary-side resonant current $i_{S2}$ so that both switches $S_{S12}$ and $S_{S22}$ are turned on during delay-time interval $[T_2-T_3]$. Because the secondary of the transformers is shorted during delay-time intervals $[T_0-T_1]$ and $[T_2-T_3]$, the voltage across resonant tank $L_R-C_R$ during delay-time intervals is $V_{in}$ instead of $V_{in}-nVO$ which is the case with no delay-time control. Therefore, with the delay-time control, a higher voltage is applied across the resonant tank and, consequently, a higher amount of energy is stored in resonant inductor $L_R$. Therefore, for the same input voltage and switching frequency, secondary-side delay-
time control provides a higher output voltage compared to the conventional frequency control.

Figure 2 shows the calculated dc conversion ratio $M = \frac{nV_D}{V_{IN}}$ of the SRC with delay-time control as a function of normalized switching frequency $f_S = f_S/f_0$ and with Q-factor $Q = \sqrt{L_R/C_R/(n^2R_{LOAD})}$ and normalized delay time $T_{D,N} = T_D/T_S$ as parameters. It should be noted that control characteristics with delay time $T_D = 0$ are those of the conventional SRC. Derivations of the dc-conversion ratio characteristics shown in Fig. 2 are given in [8].

To illustrate how the proposed delay-time control achieves active balancing of the output currents of two interleaved converters, Fig. 3 shows the dc characteristics of two converters with mismatched components. The characteristics of the reference converter, CONVERTER 1, without delay-time control ($T_D = 0$) for $Q = 1$ is shown with the solid red line. The corresponding characteristics of the mismatched converter, CONVERTER 2, is shown with the solid blue line. Because of the mismatching, the converters have different resonant frequencies, i.e., the resonant frequency of CONVERTER 1 is $f_0$ while that of CONVERTER 2 is assumed to be $1.1f_0$. Because the characteristics are shifted from each other, to regulate the same output voltage they require different frequencies, as illustrated in Fig. 3 by operating points A and B on the constant-gain line ($M = 0.92$). As also can be seen in Fig. 3, for the same input voltage and switching frequency the output voltage of CONVERTER 2 is higher than that of CONVERTER 1, as illustrated with operating points B and C on the constant-frequency line ($f_N = 1.24$) in Fig. 3. Therefore, if the two interleaved converters were driven by the same switching frequency, CONVERTER 2 would process the entire output power, while CONVERTER 1 would be practically off. However, because of the boost characteristics of the delay-time control, the output voltage (gain) of CONVERTER 1 can be increased, as shown in Fig. 3 with dashed red lines that correspond to normalized delay time $T_{D,N} = 0.05$ and $T_{D,N} = 0.1$. As can be seen from Fig. 3, for $D = 0.05$ the gain of CONVERTER 1 at normalized frequency $f_N = 1.24$ is increased to the level of CONVERTER 2 gain, i.e., both converter can control the specified output voltage at the same frequency enabling interleaved operation with current (power) sharing.

The proposed control can be implemented by either

![Fig. 2](image_url)

![Fig. 3](image_url)
challenge is to provide the balance of input (capacitor) voltages $V_{\text{IN1}}$ and $V_{\text{IN2}}$. Generally, the balance of the capacitor voltages can only be achieved and maintained if the converters are identical and draw equal energy. Otherwise, the input voltages of the two converters will be different depending on the mismatching of the two converters. To prevent the input-voltage imbalance from exceeding a permissible range, a passive or active voltage-balancing control must be implemented.

The proposed delay-time control can also be employed to balance the capacitor voltages. In this active input-capacitor voltage-balancing control, the output of the two interleaved converters is regulated by frequency control of the primary switches, while the delay-time is used to regulate the input voltage of each converter, i.e., input-capacitor voltage, to maintain their balance. The input capacitor voltage is regulated by processing the difference (error) between the measured input-capacitor voltage and desired reference voltage $V_{\text{REF(IN)}}$ derived from the sensed input voltage. The error determines a delay-time that is necessary to achieve and maintain the desired input voltage. By selecting reference voltage $V_{\text{REF(IN)}}$ to be $V_{\text{IN}}/2$, the converters can achieve perfectly balanced input voltages. Moreover, once the balance of input voltages $V_{\text{IN1}}$ and $V_{\text{IN2}}$ is achieved, the interleaved converters draw equal energy, i.e., the power sharing of the two converters is also achieved.

III. EXPERIMENTAL RESULTS

The performance of the SRC converter with delay-time control was evaluated on a 1.8-kW prototype implemented with two interleaved 900-W power stages. The converter was designed to operate from the 240–450-V input-voltage range and provide a 13.8-V output. Since the required full-power of each power stage is relatively low (1 kW), the half-bridge topology is selected, as can be seen in Fig. 5.
which shows the circuit diagram of the experimental circuit. The list of semiconductor and passive components used in the experimental prototype circuit are given in Table I and Table II, respectively. Figure 6 shows a photo of the prototype.

It should be noted that because the secondary circuit layout is designed to cancel the output current ripples of the interleaved converters, the output rectifier switches of the two power stages and output capacitors (forty five 22-\(\mu\)F multi-layer ceramic capacitors in parallel) are tightly interconnected. As a result, measuring the output current of the individual power stage is not physically possible in this prototype since no single trace is available that carries the total current of the individual converters. However, since the magnetizing current of the proposed converter is much smaller than the resonant current due to a relative large magnetizing inductance, the measured primary current waveform of each power stage is proportional to its secondary current waveform whose rectified average represents the output current.

Figure 7 shows measured primary-current and gate-voltage waveforms of secondary switches \(S_{S11}\) and \(S_{S12}\) when the converter operates without current sharing control and delivers 40-A load from the 240-V input. As seen in Fig. 7, because of resonant-component mismatching, primary currents \(i_{P1}\) and \(i_{P2}\) are significantly imbalanced, i.e., the interleaved power stages do not share the load current (power) well.

Figures 8(a), (b), and (c) show the measured waveforms of primary currents \(i_{P1}\) and \(i_{P2}\) along with the gate-drive waveforms of secondary switches \(S_{S11}\) and \(S_{S12}\) when the circuit operates with proposed current sharing control and delivers full power from the 240-V, 350-V, and 450-V input, respectively. The measured waveforms show a very good current balance of the two interleaved converters. To avoid control loop interactions, the bandwidth of the delay-time control loop is set to approximately 100 Hz which is about ten times lower than that of the variable-frequency output-voltage regulation loop.

Finally, Fig. 9 shows measured efficiency of the prototype as a function of the load current for different input voltages. The two power stages operate in interleaved mode from full load down to 30 % of the full load. When the output power decreases below 30% of the full load, i.e., at approximately 40 A, one power stage is turned off to improve the light load efficiency. The converter exhibits the highest full-load efficiency of 94.8% for the nominal voltage of 350 V. The peak efficiency occurs of 95.4% occurs at the 40% of the full load and nominal input voltage. It should be noted that the full-load efficiency of the prototype could have been increased for 1.5-2.5% by further optimization. However, this additional optimization has not been done.

### Table I: Semiconductor component list

<table>
<thead>
<tr>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Switches:</td>
<td>IPW65R041CFD (TO-247)</td>
</tr>
<tr>
<td>(S_{P11}, S_{P21}, S_{P12}, S_{P22})</td>
<td>650 V, 0.41 m(\Omega)</td>
</tr>
<tr>
<td>(S_{S11}, S_{S21}, S_{S12}, S_{S22})</td>
<td>BSB008NE2LX (CanPAK)</td>
</tr>
<tr>
<td>(V_{GATE}<em>{SS11}, V</em>{GATE}_{SS12})</td>
<td>25 V, 0.08 m(\Omega)</td>
</tr>
<tr>
<td>DSP Controller</td>
<td>TMS320F28027 (TI)</td>
</tr>
<tr>
<td>Driver</td>
<td>SI8235 (Silicon Lab)</td>
</tr>
</tbody>
</table>

### Table II: Passive component list

<table>
<thead>
<tr>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{R1}, C_{R2}, C_{R3})</td>
<td>100nF-942C12P1K – CDE [9.2 A(\text{rms})]</td>
</tr>
<tr>
<td>(C_{O})</td>
<td>22(\mu)F-MLCC-25 V, 45 in parallel</td>
</tr>
<tr>
<td>(L_{S1}, L_{S2})</td>
<td>79uH (PQ35/35 — DMR)</td>
</tr>
<tr>
<td>(L_{r}) Winding</td>
<td>0.1mmx300 strands 28Ts</td>
</tr>
<tr>
<td>(TR_{r}, TR_{s}) : Lm</td>
<td>800uH</td>
</tr>
<tr>
<td>(TR_{r}, TR_{s}) : Turn Ratio</td>
<td>9:1 (ETD59/28 — 3C94)</td>
</tr>
<tr>
<td>(TR_{r}, TR_{s}) : Primary Winding</td>
<td>0.1mmx300 strands 9Ts</td>
</tr>
<tr>
<td>(TR_{r}, TR_{s}) : Secondary Winding</td>
<td>42 mils (1.067 mm), 9mm Width, copper foil 1Turn</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>40kHz</td>
</tr>
</tbody>
</table>
since the primary purpose of the prototype was to verify the performance of the proposed active current-sharing method.

IV. SUMMARY

In this paper, a novel control method for achieving active load-current-sharing of paralleled or interleaved isolated series-resonant converters has been introduced. In the proposed control method, the output voltage is regulated by variable-frequency control of the primary switches, while delay-time control of secondary-side rectifier switches is employed to correct current imbalance between the converters. The evaluation of the proposed control method was performed on a 1.8-kW prototype that was implemented by two 900-W series-resonant converters in interleaved operating from a 240-450-V input-voltage range and providing a 13.8-V output. The prototype shows excellent current balancing between the interleaved converters.

REFERENCES