REDUCTION OF VOLTAGE STRESS IN INTEGRATED HIGH-QUALITY RECTIFIER-REGULATORS BY VARIABLE-FREQUENCY CONTROL

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Abstract **– The Integrated High-Quality Rectifier-Regulators (IHQRRs) suffer from relatively high stress on the internal-energy storage capacitor and, consequently, on primary-side semiconductors. As a result, they are not practical in applications with the universal input-voltage range. In this paper, a variable-frequency control that reduces the voltage stress and makes the IHQRRs suitable for universal input-range applications is described. Evaluation results of a 90 W, experimental BIBRED converter that uses the proposed variable-frequency control are presented.**

1 Introduction

Utility/dc interfaces that draw nearly sinusoidal current from the utility lines have been extensively used in high-power conversion systems for decades. The use of these high-power-factor, low-harmonic-distortion power processors has been primarily dictated by the need to maximize the power that can be extracted from the utility [1].

In applications with power levels substantially lower than the maximum power available from the utility outlet, a utility/dc interface has been used rarely due to its cost. However, the imminent introduction of power-quality standards that are expected to limit the current harmonic content of power processors starting at power levels as low as several tens of watts (e.g. IEC 555-2) has spurred significant research and development efforts in the area of low-power, low-cost, low-current-distortion converters.

The most commonly used approach in ac-dc conversion that meets high power-quality requirements is the "two-stage" approach [2]. In this approach, a non-isolated boost-like converter, which is controlled so that the rectified line current follows the line voltage, is used as the input stage that creates an intermediate dc bus with a relatively large second harmonic ripple. This power-factor-correction (PFC) stage is then followed by a dc/dc converter which provides isolation and high-bandwidth voltage regulation. For high-power levels, the PFC stage is operated in the continuous-conduction mode (CCM), while the dicontinuous-conduction-mode (DCM) operation is commonly used at lower power levels due to a simpler control.

Although relatively simple, mature, and viable in a wide power-range applications, the two-stage approach suffers from several drawbacks. First, due to two-stage power processing, conversion efficiency is reduced. Second, a separate PFC stage adds components and complexity and, consequently, increases the cost. The cost increase is especially undesirable for low-power supplies used in consumer electronic products such as, for example, personal computers, low-end printers, home appliances, etc.

In an effort to reduce the component count and also improve the performance, a number of "single-stage" PFC ac-dc converters have been introduced recently [3] - [7]. In a single-stage approach, power-factor-correction, isolation, and high-bandwidth control are performed in a single step, i.e., without creating an intermediate dc bus. Generally, these converters use an internal energy-storage capacitor to handle the differences between the varying instantaneous input power and a constant output power. This storage capacitor is connected to the output through switch(es) as opposed to the energy-storage capacitor in the conventional PFC converters where it is connected directly across the load.

Among the single-step approaches, the Integrated High-Quality Rectifier-Regulator (IHQRR) approach described in [4] seems particularly attractive from the cost point of view since it can be implemented with only one switch and simple control. Generally, the IHQRR concept combines the DCM boost converter with various dc-dc converters in a single stage. Low input-current harmonic distortions are achieved through the inherent property of the DCM boost converter to draw a sinusoidal-like current if its duty cy-

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cle during a line period is held relatively constant. Although the proposed family of the IHQRR has a number of members that imply high- and medium-power applications (e.g., bridge-type IHQRRs) [4], this approach seems practical at lower power levels due to the limitations imposed by the input characteristic of the IHQRRs which is the same as that of the DCM boost converter.

The major drawback of the IHQRRs is relatively high voltage stress on the internal energy-storage capacitor and the primary-side semiconductors. As a result, this approach in its originally proposed form is not practical for applications with the universal input-voltage range.

The objective of this paper is to introduce and describe a variable-frequency control technique for the IHQRRs that reduces the voltage stress and, therefore, makes the IHQRR approach practical for low-power, universal input-voltage range power supplies.

2 Review of Operation and Characteristics of BIFRED and BIBRED

In this section, the basic operation principles and key characteristics of the Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc (BIFRED) and Boost Integrated with Buck Rectifier/Energy storage/Dc-dc converter (BIBRED) converters are reviewed [4].

2.1 BIFRED [4]

The circuit diagram of the BIFRED power stage along with its key waveforms is shown in Fig. 1.

Although the BIFRED power stage has only one switch, two conversion stages can be identified for the purpose of analysis. In fact, input inductor L_1, rectifier D_1, switch S_1, and internal energy-storage capacitor C_1 form a DCM boost power stage, while switch S_1, the transformer with magnetizing inductance L_2, output rectifier D_2, and output-filter capacitor C_2 make up a flyback power stage.

When S_1 is turned on, L_1 is energized by the rectified input voltage and inductor current i_{in} increases. At the same time, magnetizing inductance L_2 is energized by C_2 which during conduction of S_1 appears in parallel with the primary of the transformer. As a result, magnetizing current i_m also increases. Due to a reverse bias, D_2 is off when S_1 is conducting.

When S_1 is turned off, energy stored in L_1 is being transferred to C_1 while i_{in} is decreasing toward zero. During this period, D_2 is conducting so that the energy stored in L_2 is being transferred to the output. As a result, magnetizing current i_m is also decreasing.

To achieve low harmonic distortions in i_{in}, L_1 must be operated in the DCM [4], i.e., current i_{in} must reach zero before S_1 is turned on again. Generally,

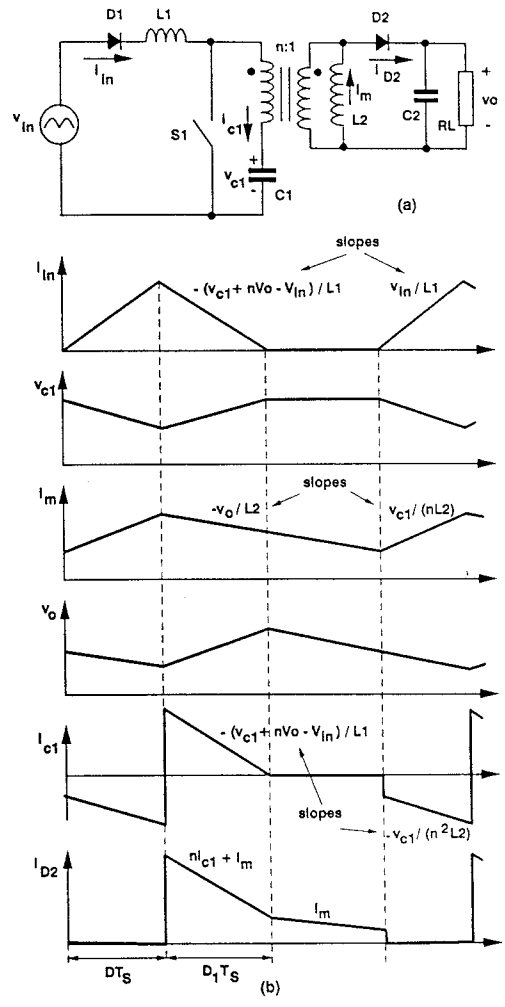

Fig. 1: BIFRED power stage: (a) circuit diagram; (b) key waveforms [4].

L_2 can be operated in either the DCM or the CCM. However, to reduce the current stresses, it is more desirable to operate L_2 in the CCM [7].

The voltage conversion ratio of the BIFRED can be estimated from the volt-second balance on inductors L_1 and L_2, and input-output power balance. Assuming that, at twice the line frequency, the ripple of the energy-storage capacitor voltage V_C1 and output voltage V_O is small, i.e., assuming that V_C1 and V_O are essentially dc voltages, the volt-second balance on L_1 and L_2 (for the CCM operation) yields:

$$V_{in}D = (V_{C1} + nV_O - V_{in})D_1, \tag{1}$$

$$\frac{V_{C1}}{n}D = V_O(1-D), \tag{2}$$

where V_{in} is the amplitude of the line voltage, n is the turns ratio of the transformer, D is the duty ratio of switch S_1, and D_1 is duty cycle that corresponds to the time interval of the decreasing i_{in}.

From Eqs. (1) - (2), the following voltage conversion ratios can be obtained:

$$M_{DCM} = \frac{V_{C1} + nV_O}{V_{in}} = 1 + \frac{D}{D_1}, \quad (3)$$

$$M_1 = \frac{V_{C1}}{V_{in}} = (1-D)\left(1 + \frac{D}{D_1}\right), \quad (4)$$

$$M_{CCM} = \frac{V_O}{V_{C1}} = \frac{1}{n}\frac{D}{1-D}, \quad (5)$$

$$M = \frac{V_O}{V_{in}} = M_1 M_{CCM} = \frac{1}{n} D\left(1 + \frac{D}{D_1}\right), \quad (6)$$

where M_{DCM} and M_{CCM} are the effective voltage-conversion ratios of the DCM boost and the CCM flyback stages.

Ratio D/D_1 can be found from the input-output power balance. Taking quasi-static approach and assuming ideal components (100% efficiency), it follows that:

$$< i_{in} > V_{in} = 2 I_O V_O, \quad (7)$$

where $< i_{in} >$ is the average input current during a switching cycle. Factor 2 on the right-hand side accounts for the fact that in a PFC converter the maximum instantaneous power that occurs at V_{in} is twice the dc output power $I_O V_O$, if it is assumed that the input current faithfully follows the input voltage (PF=1) [6].

Since the average input current from the i_{in} waveform in Fig. 1(b) is:

$$< i_{in} >= \frac{1}{2}\frac{V_{in}}{L_1} D T_S D + \frac{1}{2}\frac{V_{in}}{L_1} D T_S D_1, \quad (8)$$

from Eqs. (7) and (8) it follows that:

$$\frac{D}{D_1} = \frac{-1 + \sqrt{1 + 2/K_1}}{2}, \quad (9)$$

where:

$$K_1 = \frac{2L_1 f_S}{n^2 R_L} = \frac{2L_1 f_S I_O}{n^2 V_O}, \quad (10)$$

and where f_S is the switching frequency and R_L is the load resistance.

2.2 BIBRED [4]

The circuit diagram of the BIBRED power stage along with its key waveforms is shown in Fig. 2.

As in the BIFRED, when S_1 is turned on, L_1 is energized by the rectified input voltage, and inductor current i_{in} increases. At the same time, the output-filter inductance L_2 is energized by C_2 which during conduction of S_1 appears in parallel with the primary

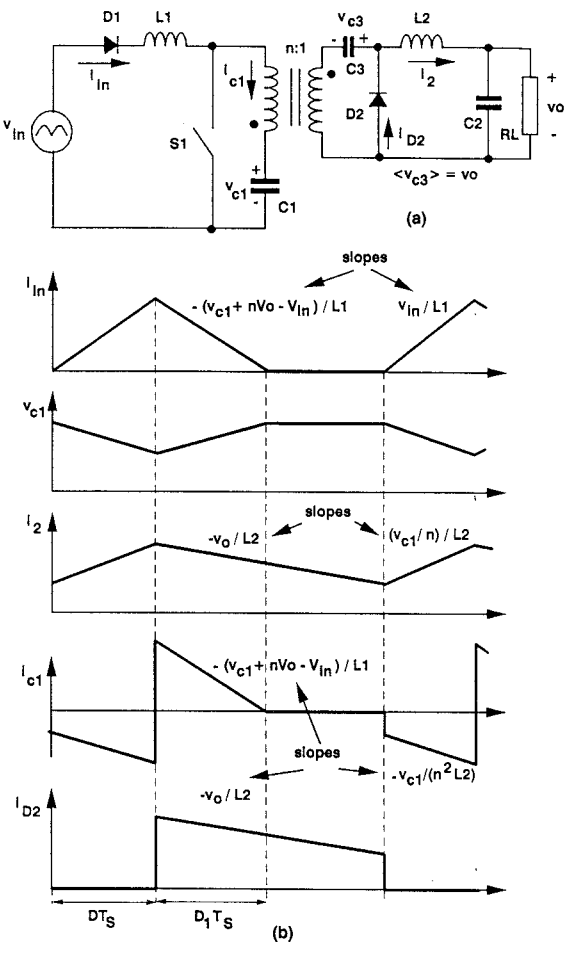

Fig. 2: BIBRED power stage: (a) circuit diagram; (b) key waveforms.

of the transformer. As a result, current i_2 also increases. Due to a reverse bias, D_2 is off when S_1 is conducting.

When S_1 is turned off, energy stored in L_1 is being transferred to C_1 while i_{in} is decreasing toward zero. During this period, D_2 is conducting current i_2, which is also decreasing. During this interval, the transformer core is being reset by the voltage across capacitor C_2, whose average voltage is equal to V_o.

As in BIFRED, to achieve low harmonic distortions in i_{in}, L_1 must be operated in the DCM [4], i.e., current i_{in} must reach zero before S_1 is turned on again. Generally, L_2 can be operated in either the DCM or the CCM. However, to reduce the current stresses, it is more desirable to operate L_2 in the CCM [7].

The voltage-conversion ratio of the BIBRED is identical to that of the BIFRED since Eqs. (1) - (10) are the same for both converters. As a result, the conditions for the DCM operation of L_1 and the CCM operation of L_2 in the BIFRED are the same as the corresponding conditions for L_1 and L_2 in the BIFRED [7].

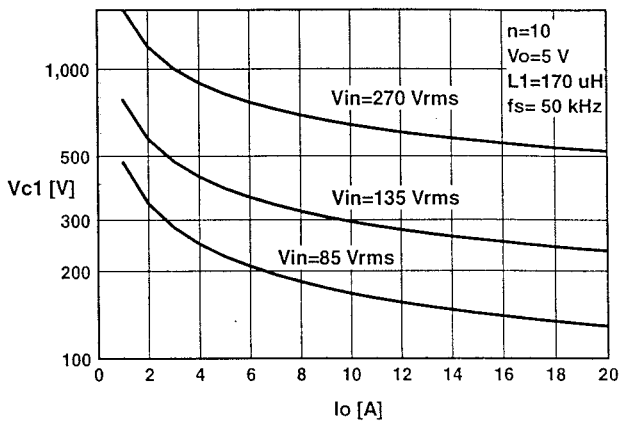

Fig. 3: Voltage of bulk capacitor in BIFRED and BIBRED as a function of the output current for different line voltages. Power stage parameters are shown in upper right corner.

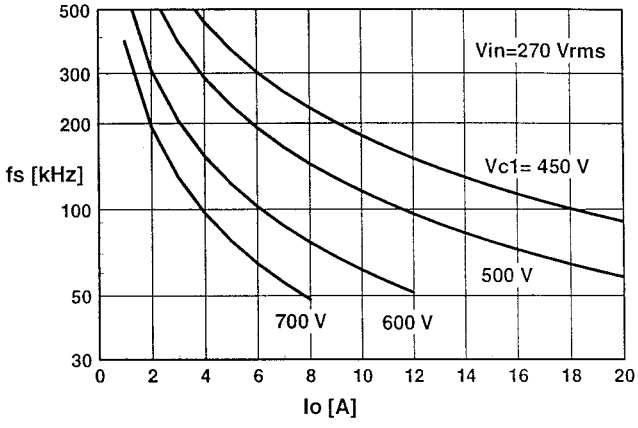

Fig. 4: Switching frequency as function of output current for different regulated voltages of bulk capacitor. Circuit parameters are the same as in Fig. 3.

2.3 Voltage Stress of Bulk Capacitor

In both the BIFRED and BIBRED, the internal, low-frequency storage capacitor (bulk capacitor) simultaneously serves as the output-filter capacitor of the DCM boost stage and input-voltage source for the dc/dc converter operating in CCM. Since the output voltage of the DCM boost stage is strongly dependent on the load current (Eqs. (3), (9), and (10)), and since the voltage-conversion ratio of the CCM dc/dc converter is the same as that of the buck/boost converter (Eq. (5)), the bulk capacitor voltage is a strong function of the load current if the output voltage is regulated. The dependence of the bulk capacitor voltage on the load current can be estimated from the following equation:

$$V_{C1} = \frac{V_{in}}{2}\left[1+\sqrt{1+\frac{n^2 V_O}{L_1 f_S I_O}}\right] - nV_O, \qquad (11)$$

which is derived by substituting Eq. (9) into Eq. (3).

Figure 3 shows a plot, generated using Eq. (11), of the bulk-capacitor voltage as a function of the output current for different line voltages.

As can be seen, the capacitor voltage increases as the output current decreases and/or the line voltage increases. For the universal input-voltage range (85-270 Vrms), the capacitor voltage stress and, therefore, switch voltage stress are extremely high at lighter loads. For example, from Fig. 3, for V_{in}^{rms}=270 V and at 20% of full load (4A), the capacitor voltage is approximately 900 V, while the switch voltage is 50 V ($nV_O = 10 * 5$) higher. According to Eq. (11), the voltage stress could be decreased by decreasing the turns ratio of the transformer. However, to attain an acceptable voltage stress at a relatively low minimum load (e.g., 10% of the full load), a very small turns ratio would be required, which would result in an unacceptable deterioration of the CCM dc/dc converter efficiency and, consequently, of the overall efficiency. Therefore, a more desirable method of limiting the capacitor voltage is required.

3 Variable-Frequency Control

Since the gain of the CCM dc/dc stage of both the BIFRED and BIBRED depends only on the duty cycle (Eq. 5), and the gain of the DCM boost input stage depends on the frequency but not on the duty cycle (Eq. (3), it is possible to regulate the bulk-capacitor voltage (without affecting the output) by a variable-frequency (VF) control [8], [7], [6]. Figure 4 shows the switching frequency as a function of the load current for a VF control of the circuit with characteristics shown in Fig. 3. The curves in Fig. 4 were obtained by solving Eq. (11) for the switching frequency as a function of the output current and input voltage.

As can be seen from Fig. 4, the frequency range required to regulate the capacitor voltage is strongly dependent on the desired regulation voltage. For example, if the capacitor voltage is regulated at 700 V, then the required frequency range for full load down to 10% of full load extends from 50 kHz to 200 kHz. In fact, in this case, the voltage regulation is active only for loads below 8 A since for higher load currents the voltage of bulk capacitor is below 700 V. However, if the voltage were to be regulated in the 450-500 V range, the maximum frequency would be well in excess of 500 kHz. Since neither the BIFRED nor the BIBRED handles circuit parasitics (mainly

leakage inductance of the transformer) well, the implementation of the circuit at such high frequencies would be extremely complex and inefficient. Therefore, there is a strong trade-off between the voltage stress on the bulk capacitor and the frequency range of the control. In fact, while it is desirable to limit the capacitor voltage to a lower value because of a lower stress, the minimum voltage of the capacitor is limited by the desired harmonic distortions in the input current [9], [4], [6], [7]. Namely, the sum of the capacitor voltage and the reflected output voltage to the primary represents the output voltage of the DCM boost input stage. Input-current harmonic distortions and power-factor are strongly dependent on the difference between the output voltage and the input voltage of the DCM stage. The distortions increase as this difference decreases [9], [6], [7]. In fact, it was found that an acceptable level of harmonic distortions is obtained if the output voltage is kept 25% higher than the peak line voltage [8]. Therefore, for the converter with characteristics shown in Figs. 3 and 4, the minimum capacitor voltage at high line ($1.41 * 270 = 380$ V) is in the 450 V range (450 V + reflected output voltage $10 * 5$ V = 500 V).

Since a tight regulation of the capacitor voltage requires an unacceptably wide frequency range, it is necessary to make a trade-off between the frequency range and the voltage regulation range. For example, from Fig. 4, if the capacitor voltage at V_{in}^{rms}=270 V is loosely regulated so that it is allowed to change from 500 V at full load (20 A) to 600 V at 10% of full load (2 A), then the required maximum frequency is 300 kHz. Moreover, if the voltage were allowed to increase up to 700 V, the maximum frequency would be 200 kHz. Implementation of a VF control with a wide regulation range requires low-gain, low-bandwidth control loop.

Finally, it should be noted that in the above considerations it was assumed that the output dc/dc stage was always operating in the CCM. However, if at light loads the dc/dc converter enters the DCM, the capacitor voltage dependence on the load current is much less dramatic since the gain of the dc/dc stage operating in the DCM is higher than that in the CCM. Also, in practical circuits, the frequency range is significantly smaller than the theoretically calculated one because of the power loss (i.e. efficiency much lower than 100%).

4 Experimental Results

To verify the proposed control, an experimental, 90W BIBRED IHQRR with the following specifications was designed:

V_{in}^{rms}=85 - 270 V V_O=5 Vdc

I_O=1.8 - 18 Adc f_s^{min}=50 kHz

The circuit diagram of the power stage is shown in Fig. 5. It was built with the following components:

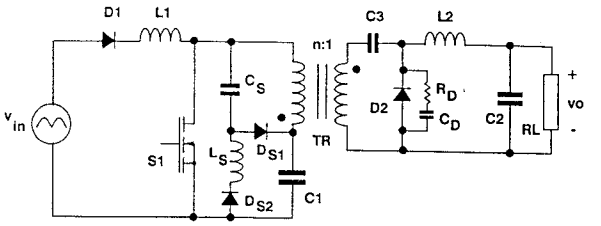

Fig. 5: Circuit diagram of experimental 90 W BIBRED power stage.

S_1 - IRFPE50, D_1, D_{S1}, D_{S2} - PH BYR34, D_2 - IR 30CPQ150, C_1 - 330 μF/450V X 2 in series, $C-2$ - 200 μF, C_3 - 47 μF, C_S - 0.4 μF, C_D - 1 nF, L_1 - 170 μH (TDK PC40, 22 turns of AWG #22), L_2 - 23 μH (Micrometals T106-26, 15 turns of 3 strands of AWG #19), L_S - 25 μH (MPP 55353-A2, 27 turns of AWG #23), TR (TDK PC40, primary 50 turns of AWG #26, secondary 5 turns of 3-mil copper foil, L_m = 1.35 mH), and R_D=100 Ω.

To control the voltage spike across the switch caused by the energy stored in the leakage inductance, the lossless snubber consisting of C_S, L_S, D_{S1}, and D_{S2} was used.

The VF control of the bulk-capacitor voltage was implemented using the approach shown in Fig. 6 [10]. In this approach, the frequency change is obtained by varying the effective timing resistance of a standard PWM chip as a function of the difference between the bulk capacitor and reference voltage. In fact, transistor Q along with resistor R_E act as a voltage-controlled current source that charges timing capacitance C_T. Resistor R_T sets the minimum frequency. The reference voltage determines the starting regulation voltage. For voltages below this level, transistor Q is off, and the converter runs at a constant frequency determined by R_T and C_T. The voltage regulation range is set by the gain of the error ampli-

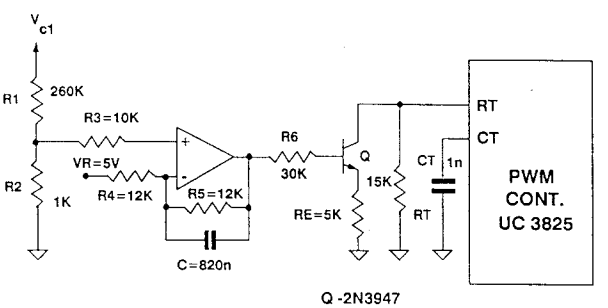

Fig. 6: Circuit diagram of variable-frequency control implementation.

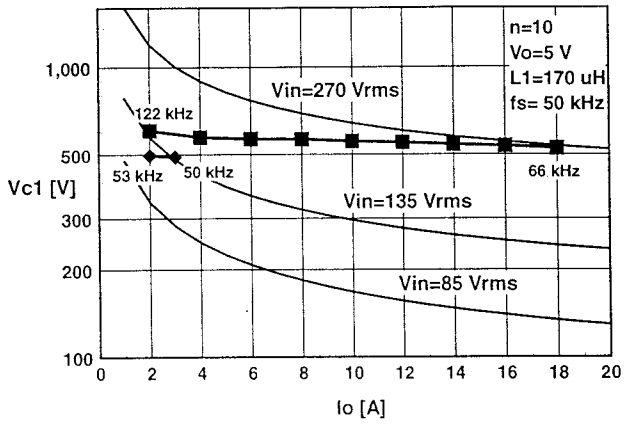

Fig. 7: Measured voltage of bulk capacitor as function of load current for VF control that starts at 500 V.

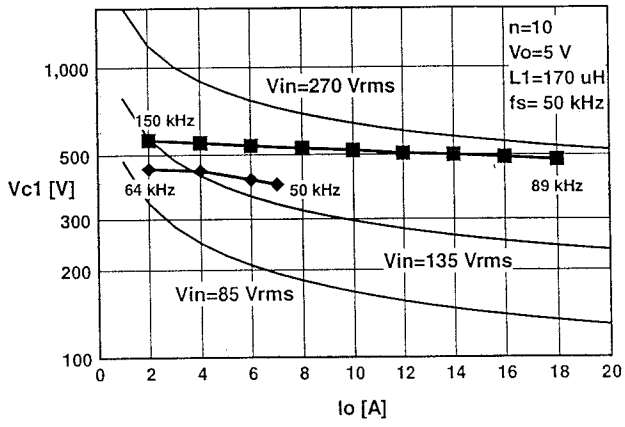

Fig. 8: Measured voltage of bulk capacitor as function of load current for VF control that starts at 400 V.

fier, while C is used to limit the bandwidth. The component values used to implement the VF controller are shown in Fig. 6.

Figure 7 shows the superimposed plots of the measured bulk-capacitor voltage as a function of the load current for a VF control and the theoretically calculated values that correspond to the parameters of the experimental circuit (Fig. 3). As can be seen from Fig. 7, the VF control starts regulating the capacitor voltage when it reaches approximately 500 V. The maximum capacitor voltage that occurs at high line (V_{in}^{rms}=270 V) and minimum load (I_O=1.8 A) is limited to around 600 V, which is twice as low as without VF control. At this operating point, the converter operates with the maximum switching frequency of 122 kHz.

Figure 8 shows the measured capacitor voltage when the starting regulation voltage is decreased to 400 V. In this case, the maximum capacitor voltage is limited to 550 V at the switching frequency of 150 kHz. Although this control results in lower voltage stress on the capacitor and switch, it does not make any difference in the selection of the voltage ratings of these components. Both implementations require a 800 V switch and a 700 to 800 V rated capacitor, which is usually implemented by a series connection of lower voltage rated capacitors. To be able to select these components with a lower rating, e.g., 600 V switch, it would require a VF control with an impractically wide range.

The measured efficiencies of the power stage as functions of the line voltage at full load (I_O=18 A) for the above discussed VF control implementations are shown in Fig. 9.

Since in both implementations, for line voltages approximately below 180 Vrms, the converter at full load operates at a constant frequency (50 kHz), the efficiency of the converter is independent of the VF-control implementation. In fact, the small differences in the measured efficiencies seen in Fig. 9 are the result of measurement inaccuracies. However, for voltages greater than 180 Vrms, the efficiencies of the VF implementations with the regulation threshold of 400 V becomes lower than that of the implementation with the 500 V threshold. The difference increases as the line voltage increases, and is more than 2% at V_{in}^{rms}=270 V. The difference is the result of higher frequency-dependent losses in the 400 V regulation threshold VF implementation. Generally, the efficiency is relatively poor compared to the two-stage approach which, for this application, can yield overall efficiencies in the seventy-percent range.

Finally, the measured line current distortions for both implementations are within the limits of the IEC 555-2 specifications [11]. For the 500 V regulation threshold application, the measured total harmonic distortions are 18%, while for the 400 V regulation threshold implementation the THD is approximately

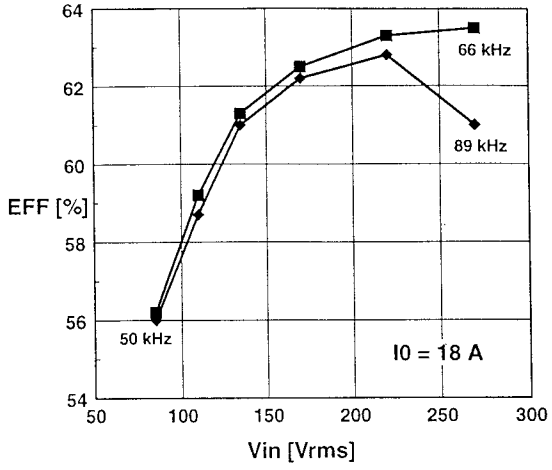

Fig. 9: Measured efficiencies as functions of line voltage at full load. Squares correspond to VF control with 500 V threshold (Fig. 7).

21%. Figure 10 shows the oscillogram of the line current and voltage at V_{in}^{rms}=270 V and I_O=18 A.

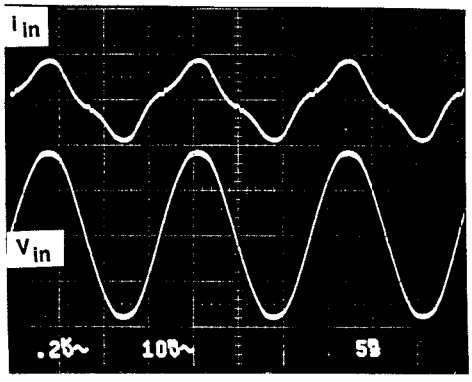

Fig. 10: Oscillogram of line current and line voltage at V_{in}^{rms}=270 V and I_O=18 A. Scales: 200 V/div; 1 A/div; 5 μs/div.

5 Summary

Due to high voltage stress on the internal energy-storage capacitor and switch, the Integrated High-Quality Rectifier-Regulators (IHQRR) are not suitable for applications with the universal line-voltage range (85 - 270 Vrms). By applying a variable-frequency (VF) control, voltage stress can be reduced so that IHQRRs can be used in universal line-voltage-range applications. In this paper, design trade-offs for the VF control are discussed and verified on an experimental, 90 W BIBRED converter.

Acknowledgement

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