Single-Phase Three-Level Boost Power Factor Correction Converter

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Abstract **In many single-phase PFC applications, the power level can reach several kilo-watts; and in some situations, the input voltage can be quite high too. For high power and/or high voltage applications, the major concerns of the conventional boost PFC converter are the inductor volume and weight, and losses on the power devices, which will affect converter cost, efficiency, and power density. In this paper, a three-level boost converter is adopted for single-phase power factor correction (PFC), which uses a much smaller inductor and lower voltage devices than the conventional boost PFC converter does, yielding high power density, high efficiency, and low cost.**

I. Introduction

In recent years, due to the power factor correction (PFC) requirement, the single-ended boost converter has been widely used as the front-end single-phase PFC converter due to its step-up voltage conversion ratio, continuous input current, simple topology, and high efficiency. However, a couple of things are still of concern. For high power applications, the boost inductor will become one of the major factors affecting the system cost, volume, and weight. For high voltage applications, high voltage devices have to be used, which produces high conduction losses and high switching losses. When voltage is higher than a certain level, some type of devices are even not available. Therefore, it is very desirable to use smaller inductor and lower voltage devices.

The multi-level power conversion techniques have been studied before. Most works focused on the buck type which is most frequently used in high frequency DC/DC power conversion [1, 2]. A three-level boost converter was also developed for three-phase rectifier application [3]. However, due to the line commutation of the diode bridge, only two out of three lines are carrying current at any time, producing significant amount of low frequency harmonic distortion. Therefore, the three-level boost topology did not receive much attention. With the ever increasing desire of power factor correction, a single-phase rectifier can reach several kilo-watts nowadays, and the input voltage is quite high in certain situations also. By using the three-level boost topology in the high power and/or high voltage single-phase applications, significant advantages will be achieved over the conventional boost converter. With the three-level boost converter, the inductance of the boost inductor can be greatly reduced, and the semiconductor device voltage rating is only half of the output voltage. As a result, the converter power density and efficiency will be significantly improved, and cost will be reduced for high power and/or high voltage applications.

II. Three-Level Single-Ended Boost Converter

The three-level boost converter is shown in Fig. 1. The output has a capacitor voltage divider. The voltage of the center point is $V_o/2$, which is obtained by choosing $C_1=C_2$ and the symmetrical operation of the two boost switches, as explained below.

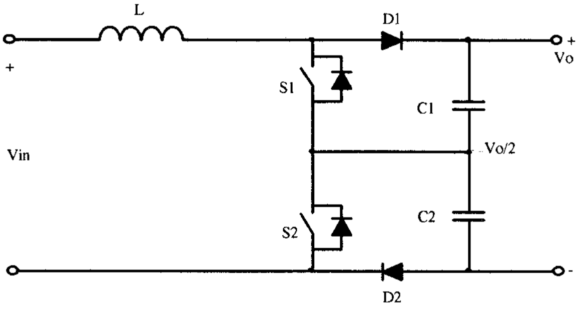

Fig. 1 Three-level boost converter

Operation Principles:

There are two regions where this converter can operate, depending on whether the input voltage is lower or higher than half of the output voltage.

Region I ($V_{in} < V_o/2$):

In this region, the boost inductor charging voltage must be V_{in}, since it is the minimum available charging voltage. However, the discharging voltage, which used to be V_o-V_{in} in a conventional boost converter, can be chosen as $V_o/2$-V_{in}. The operation waveforms are given in Fig. 2 (a).

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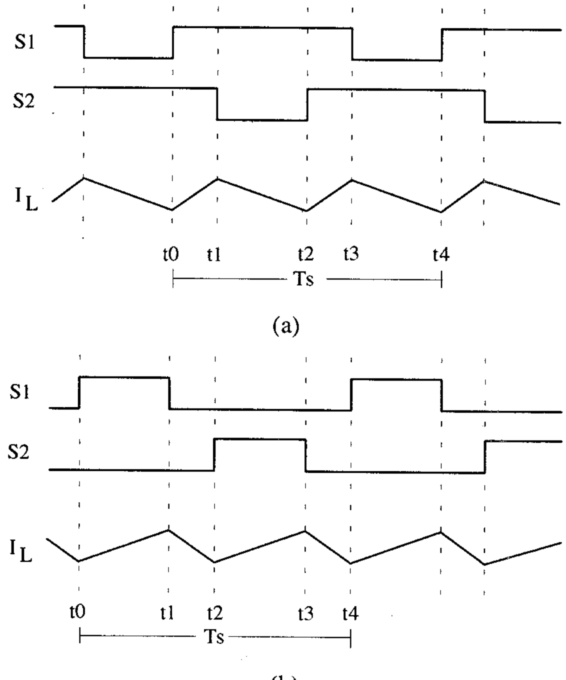
At time t_0, which is the beginning of a switching cycle, the switch S_1 is turned on and both switches are conducting. The inductor is charged with the input voltage just as in a conventional boost converter. At time t_1, which is determined by the input current compensator, S_2 is turned off, forcing the inductor current to flow through the bottom output capacitor C_2 and the bottom diode D_2. Hence, the discharging voltage applied on the inductor is $V_o/2 - V_{in}$. At time t_2, which is fixed at $t_0+T_s/2$, S_2 is turned on, charging the inductor with the input voltage again. At time t_3, S_1 is turned off, and the inductor current will go through D_1, C_1 and S_2, discharged by $V_o/2 - V_{in}$ again. Since the upper and lower capacitors are alternatively used for discharging the inductor, their voltages are theoretically balanced.



(a)

(b)

Fig. 2 Operation waveforms of a three-level boost converter

(a) Vin < Vo/2; (b) Vin > Vo/2

Region II ($V_{in} > V_o/2$):

In this region, the boost inductor charging voltage is chosen to be V_{in}-$V_o/2$, and the discharging voltage will be V_o-V_{in}. The operation waveforms are shown in Fig. 2 (b).

At time t_0, which is the beginning of a switching cycle, S_1 is turned on with S_2 left open, the inductor current flows through S_1, C_2 and D_2, and builds up under V_{in}-$V_o/2$. At time t_1, which is determined by the input current compensator, S_1 is turned off, forcing the inductor current to go through D_1, C_1, C_2 and D_2, and to decrease under V_o-V_{in}. In the next half cycle, S_2 repeats the above action.

III. Single-Phase Three-Level Boost PFC Converter

Since two active switches are used, this three-level boost converter is more favorable for high power applications. The low device voltage rating benefit is especially important in high voltage applications. From a practical point of view, the best application of the three-level boost converter would be the single-phase off-line power factor correction, where the output voltage is usually at around 400 V or higher, and the power level can be multi-kilo watts.

When the three-level boost converter shown in Fig. 1 is used for single-phase PFC, the input voltage is in a rectified sinusoidal waveform, as shown in Fig. 3. It stays in region I under the low line condition, and travels to region II if the input voltage peak is higher than Vo/2. The operations in either regions are the same as that described above, except that the duty-ratio changes with the input voltage.

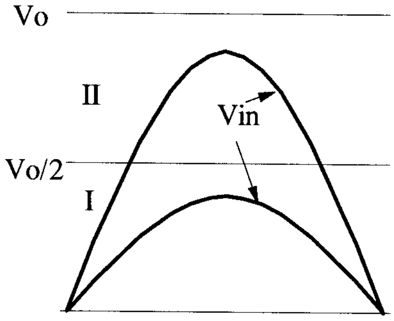


Fig. 3 Input voltage of the three-level boost PFC converter

The quantitative benefits of the single-phase three-level boost PFC converter over the conventional boost PFC converter are calculated in the following.

Less Current Ripple:

It can be proven that the maximum inductor current ripple in a boost converter occurs when the duty-ratio is 0.5. Considering the universal input line range, the maximum inductor current ripple of a conventional boost PFC converter occurs at V_{in}=0.5V_o, and is given in Eq. (1)

$$\begin{aligned}\Delta i_{\max} &= \frac{V_{in}}{L}\cdot D\cdot T_s\\ &= \frac{V_o\cdot T_s}{4L}\end{aligned} \tag{1}$$

For the three-level boost converter, the maximum current ripple in region I occurs when V_{in}=0.25V_o, where the duty-ratio is 0.5, and is given in Eq. (2).

$$\begin{aligned}\Delta i_{\max I} &= \frac{V_{in}}{L}\cdot D\cdot\frac{T_s}{2}\\ &= \frac{V_o\cdot T_s}{16L}\end{aligned} \tag{2}$$

For region II, the maximum current ripple occurs when $V_{in}=0.75V_o$, also corresponding to 0.5 duty-ratio. The maximum current ripple is given in Eq. (3).

$$\begin{aligned}\Delta i_{\max 2} &= \frac{V_{in}-0.5V_o}{L}\cdot D\cdot\frac{T_s}{2} \\ &= \frac{V_o\cdot T_s}{16L}\end{aligned} \qquad (3)$$

Comparing Eqs. (1), (2) and (3), one can see that the inductor current ripple in the three-level boost converter is one fourth of that of the conventional one. In other words, for the same current ripple, the three-level boost converter requires four times less inductance than the conventional boost converter.

Four times less inductance means four times less stored energy for the same input current. According to the magnetics knowledge, the energy storage density of a core is $\frac{1}{2}\cdot\frac{B^2}{\mu}$, which is only determined by the flux density B and the effective permeability μ, which are the same for both cases. Therefore, the inductor in the three-level boost converter has about one fourth the size of that in the conventional boost converter, which will be seen from the design examples in Section IV.

Higher Efficiency and Lower Cost:

First, the switching loss is a strong function of the voltage. The capacitive turn-on loss of the three-level boost converter is reduced eight times, assuming the same output capacitance for devices with different voltage ratings (the lower voltage device actually has less output capacitance from the device data sheet); the diode reverse recovery losses are also reduced, since the reverse voltage is only half of the output voltage, and the diodes with half voltage rating could be faster. Therefore, the total switching losses are reduced.

Secondly, the conduction losses could also be reduced when using MOSFETs as the power switches. The MOSFETs used in the conventional boost converter with above 600 V rating have significantly larger on-resistance than the half voltage rated MOSFETs in the three-level boost converter.

In fact, from performance point of view, the more competitive counterpart of the three-level boost converter is the two-interleaved boost converter drawn in Fig. 4. The inductance of each boost inductor is set at 2L (L is the inductance of the boost inductor in the three-level boost converter), which yields the same energy storage capability for both the two-interleaved boost converter and the three-level boost converter.

Figure 5 shows the two inductor ripple currents (i_1 and i_2) and the input ripple current (i_{in}), which is the result of the partial cancellation of the two inductor ripple currents. It is assumed that these two inductor ripple current waveforms are exactly the same, except for the 180° phase shift. The input current ripple frequency is two times higher than that of the inductor current ripple; therefore, to find out the input current ripple, only the period of $T_s/2$ needs to be analyzed.

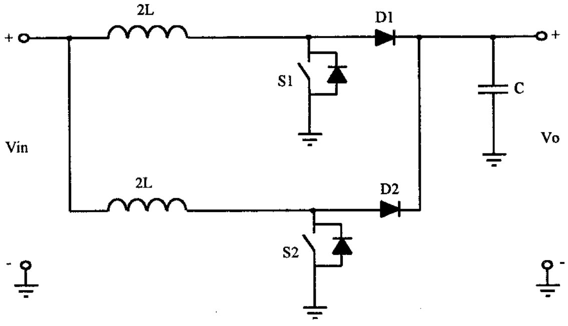


Fig. 4 Two interleaved boost converters

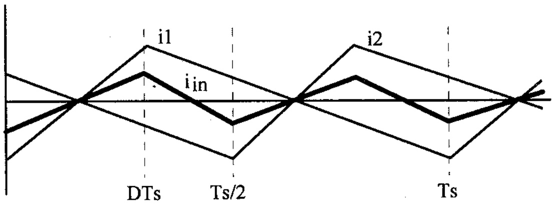


Fig. 5 Inductor ripple currents and input ripple current of the two interleaved boost converters

Assuming D<0.5, the input current ripple is $\Delta i=(k_1-k_2)DT_s$, where $k_1=V_{in}/2L$ and $k_2=(V_o-V_{in})/2L$ are the inductor current charging and discharging slops. Thus,

$$\Delta i = \frac{2V_{in}-V_o}{2L}\cdot(1-\frac{V_{in}}{V_o})\cdot T_s, \qquad (4)$$

The maximum current ripple occurs at the point where $\frac{\partial \Delta i}{\partial V_{in}}=0$. This point is $V_{in}=0.75V_o$, which is the same point where maximum current ripple occurs in the three-level boost converter. The current ripple amplitude at this point can be calculated from Eq. 4, obtaining $\Delta i = \frac{V_o\cdot T_s}{16L}$, which is the same as the expression describing the current ripple of the three-level boost converter, as given in Eq. 3.

For D>0.5, the input current ripple is $\Delta i=(k_2-k_1)D'T_s$, where $k_1=V_{in}/2L$ and $k_2=(V_o-V_{in})/2L$ are the inductor current charging and discharging slops. Thus,

$$\Delta i = \frac{V_o-2V_{in}}{2L}\cdot\frac{V_{in}}{V_o}\cdot T_s, \qquad (5)$$

With $\frac{\partial \Delta i}{\partial V_{in}}=0$, it is found that the maximum current ripple occurs at the point of $V_{in}=0.25V_o$., which is also the same point where the maximum current ripple presents in the three-level boost converter, and the maximum current ripple is also $\Delta i = \dfrac{V_O \cdot T_s}{16L}$.

Therefore, the input current ripple of the three-level boost converter is the same as that of the two-interleaved boost converter.

However, the two-interleaved boost converter has the following drawbacks compared with the three-level boost converter.

- Two complete boost converters are in parallel, including two inductors, two input current sensors, two PFC controllers with proper interleaving and input current sharing;
- Each inductor has higher ripple current, which causes higher core loss in the inductor and higher conduction losses in both inductor and the semiconductor devices;
- More severe diode reverse recovery problem occurs due to the use of high voltage diodes;
- EMI is higher since the PWM actions are happening between full output voltage and the ground;
- High voltage devices are still needed and cannot deal with high input voltage.

These drawbacks make the two-interleaved boost converter much less competitive than the three-level boost converter for high power and/or high input voltage applications.

The above advantages of the three-level boost PFC converter will be verified with the large signal simulation and the design examples given in the next section.

IV. Simulation Verification and Design Examples

Large signal simulation has been done to verify the proper operation and the input current ripple reduction of the three-level boost PFC converter as compared with the conventional boost converter. The simulation was for a 5 kW system with 50 μH boost inductance, 100 kHz switching frequency, 185 V (rms) input voltage, and 400 V output voltage. The simulation waveforms of both the conventional boost converter and the three-level boost converter are given in Fig. 6 and Fig. 7.

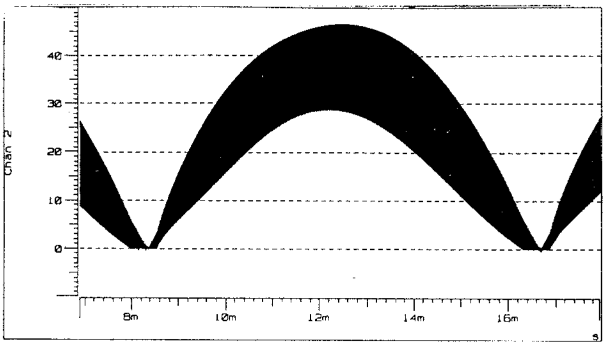


Fig. 6 Large signal simulation of the conventional boost PFC converter

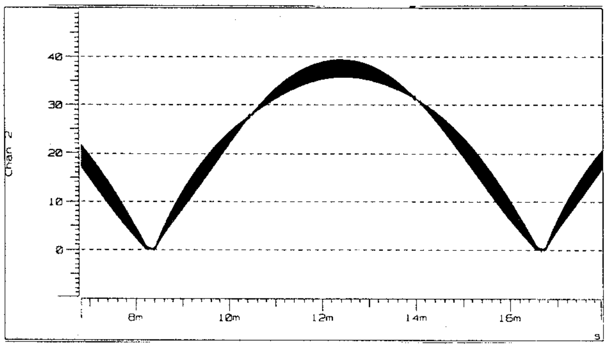


Fig. 7 Large signal simulation of the three-level boost PFC converter

Comparing the above two waveforms, one can see that the maximum current ripple in the conventional boost converter (at V_{ac}=0.5V_O), is four times larger than that in the three-level boost converter (at V_{ac}=0.25V_O and 0.75V_O).

To verify the improvement of the converter efficiency and the reduction of the inductor size, designs were made for the conventional boost converter, the two-interleaved boost converter, and the three-level boost converter. All designs are based on practical available components, and for single-phase 5 kW PFC with 185 V (rms) input, 400 V output, and 100 kHz switching frequency.

Figure 8 shows the efficiency comparison for the three 5 kW converters with different output voltages. It can be clearly seen that the three-level boost converter has obvious advantage over the other two at high output voltage due to using low voltage devices. Even at 400 V output voltage, which is for the universal line range, the three-level boost converter still has competitive efficiency performance.

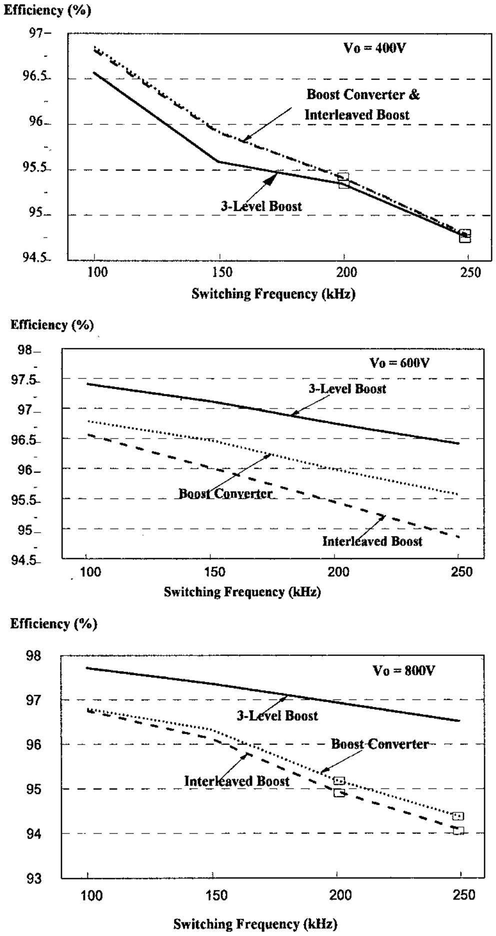


Fig. 8 Power stage efficiency for different output voltages

The other aspect of comparison is the magnetic component size. From the above analysis, for the same ripple current, the required inductance of the boost inductor is *L* for the three-level boost converter, 2×2*L* for the two-interleaved boost converter, and 4*L* for the conventional boost converter. With the assumption of 20% input ripple current (without input filter), Fig. 9 illustrates the inductor size comparison. The size of the two-interleaved boost converter is slightly higher than that of the three-level boost converter because of larger core loss due to larger ripple current in each inductor.

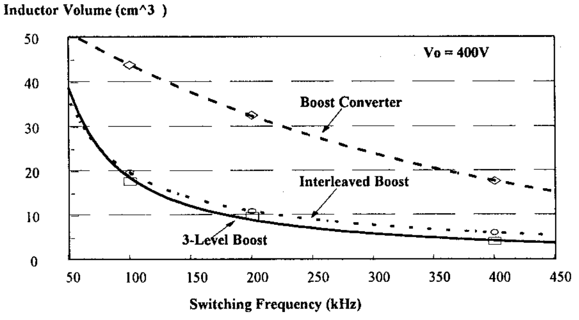


Fig. 9 Inductor size comparison

The above comparison does not consider the fact that the current ripple frequencies of the three-level boost converter and the two-interleaved boost converter are twice as high as that of the conventional boost converter. The ripple current frequency has a significant impact on the input filter size.

Form the above comparison, it can be concluded that the three-level boost converter is much better than the conventional boost converter with regard to the converter efficiency (for high output voltages) and the inductor size. The two-interleaved boost converter has better performances than the conventional boost converter, but still not as good as the three-level boost, as stated in Section III.

V. Soft-Switching of the Three-Level Boost Converter

Although this three-level boost converter already has less switching losses than the conventional boost converter, soft-switching technique is still appreciated for high voltage, high power, and high switching frequency applications.

Directly applying the zero-voltage-transition technique [4], the ZVT three-level boost converter can be constructed as shown in Fig. 10, by adding two auxiliary resonant networks.

Basically, the top resonant network achieves the ZVS for the top switch S_1, and the bottom resonant network for the bottom switch S_2. Since the turn-on actions of the two main switches are interleaved, the auxiliary networks are also running alternatively. The driving signals are drawn in Fig. 11, where the main switch driving waveforms are the same as shown in Fig. 2.

The auxiliary switch driving signal is applied a short period before the turn-on of the corresponding main switch so that a current builds up in the resonant inductor. When the resonant inductor current reaches the boost inductor current, resonance occurs between the resonant inductor and the resonant capacitor, which is the junction capacitor of the main switch together with external capacitors, if any. This resonance will discharge the resonant capacitor, and the anti-parallel diode of the main switch will then conduct. Therefore, the zero-voltage switching condition is achieved. It is noted that the energy in the upper resonant inductor is released to the upper output capacitor, and the energy in the lower resonant inductor is released to the lower output capacitor, respectively, which ensures the output capacitor voltage balancing.

All the auxiliary devices are also rated at half of the output voltage, which has less conduction and switching losses than the auxiliary devices in the conventional ZVT boost converter.

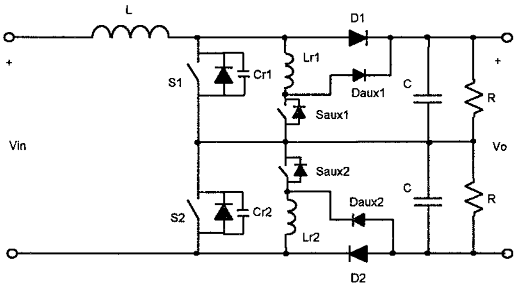
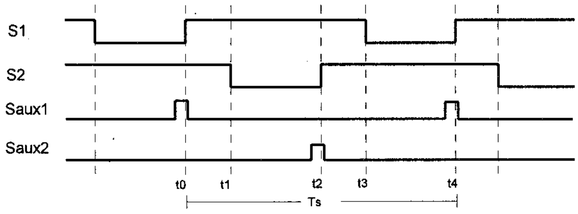
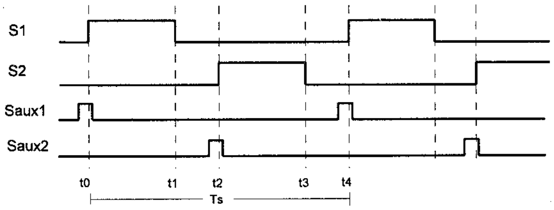


Fig. 10 ZVT three-level boost converter



(a) Vin<Vo/2



(b) Vin>Vo/2

Fig. 11 Driving signals of the ZVT three-level boost converter

The zero-current-transition technique [5] can also be applied by simply replacing the above two ZVT networks with two ZCT networks. However, in most applications, the half of the output voltage is low enough to use MOSFETs as the main power switches, and their turn-off losses are quite little. Hence, the three-level boost converter generally prefers ZVS rather than ZCS for the purpose of alleviating the diode reverse recovery problem.

VI. Conclusions

For the three-level boost converter discussed in this paper, the inductance of the boost inductor can be significantly reduced compared with the conventional boost converter. The device voltage rating is only half of the output voltage, which is desirable for high voltage applications, and reduces both conduction and switching losses. Utilization of smaller inductor and low voltage devices yields higher efficiency, higher power density, and lower cost. The ZVT three-level boost converter can further reduce the switching losses, including the diode reverse recovery losses and the capacitive turn-on losses . It would be useful for high switching frequency operation and EMI reduction.

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