

# Forward Converter with Current-Doubler Rectifier: Analysis, Design, and Evaluation Results

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**Abstract** - Complete steady-state analysis of the forward converter with the current-doubler rectifier is provided. Advantages and disadvantages of this topology compared to the conventional forward converter are discussed. Step-by-step design guidelines are also outlined. Finally, experimental evaluation results obtained on a 3.3-V, 50-A dc/dc converter prototype for the 40-60-V input-voltage range are presented.

## I. INTRODUCTION

In a continuing effort to decrease power consumption and increase the speed of data-processing circuits, their power-supply-voltage requirements are continuously being reduced. Currently, 3.3-V ICs are gradually replacing the standard 5-V ICs due to their better speed/power-consumption performance and higher integration densities. However, the transition to lower supply voltages usually requires higher output currents as well as lower output-voltage ripples. As a result, the design of an efficient secondary-side circuit is an extremely challenging task. The efficiency of the secondary-side circuit in a converter with a high output current may be improved by employing the current-doubler-rectifier (CDR) technique. The idea was first described in [1], while implementations of the CDR in the half-bridge, full-bridge, and forward converters were reported in [2]-[7]. Since the forward converter with CDR operates in a forward-flyback fashion, this topology is also called forward/flyback converter with CDR. The CDR offers the following advantages compared to the conventional secondary-side rectifier topologies such as the full-wave diode bridge, the full-wave rectifier with center-tapped transformer secondary, and the conventional forward:

- reduced rms value of the transformer-secondary current,
- reduced output-voltage ripple through cancellation of ripple currents of the two output inductors,

- extended continuous-conduction-mode (CCM) range to lower output currents,
- more evenly distributed power dissipation.

This paper provides a complete steady-state analysis of the forward converter with CDR. To facilitate the understanding of operation, the converter circuit in each topological stage within a switching cycle is reduced to a first- or second-order equivalent circuit. Design guidelines are also given. Advantages and disadvantages of the CDR forward converter vs. the conventional forward converter are evaluated on a 3.3-V, 50-A dc/dc converter prototype for the 40-60-V input-voltage range.

## II. ANALYSIS

The circuit diagram of the active-clamp forward converter with the current-doubler rectifier is shown in Fig. 1. There are two possible CDR topologies: with common-anode diodes, Fig. 1(a), and with common-cathode diodes, Fig. 1(b). For practical implementation, the CDR with common-cathode diodes is more convenient due to the widespread availability of the common-cathode configuration in a single package. To simplify the analysis, output filter inductances  $L_1$  and  $L_2$  and clamp capacitance  $C_{cl}$  are assumed to be sufficiently large. Thus, they can be considered as current and voltage sources, as shown in the equivalent circuit in Fig. 2. Also, it is assumed that all semiconductor components are ideal, except for the output capacitances of switches  $Q_1$  and  $Q_2$ , which are included into equivalent parallel capacitance  $C_{eq}$ . The magnetizing current,  $i_M$ , of the transformer consists of dc component  $I_M = I_o / (2N)$ , which is necessary to support the secondary current during off time, and ac component  $i_m$ .

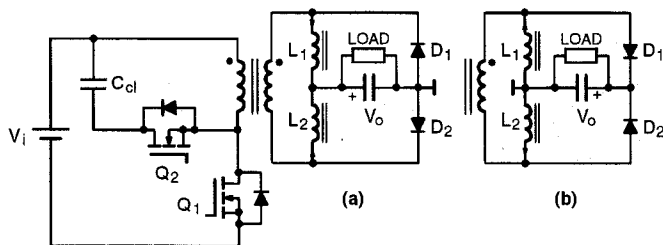


Fig. 1 Circuit diagram of active-clamp forward converter with CDR: (a) common-anode diodes, (b) common-cathode diodes

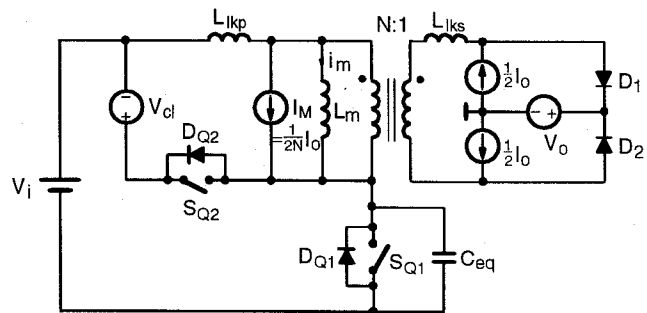


Fig. 2 Equivalent circuit of active-clamp forward converter with CDR

Inductances  $L_{lkp}$  and  $L_{lks}$  are the primary- and secondary-side leakage inductances.

Under steady-state operation, eight stages can be identified within each switching cycle, as shown in Fig. 3. Key waveforms are presented in Fig. 4. For clarity, the durations of the turn-on and turn-off intervals are exaggerated.

During  $[T_0 - T_1]$  interval, switch  $Q_1$  is on and its current is equal to the sum of reflected secondary current  $I_o/2N$  and magnetizing current  $i_M$ , which increases with a constant slope,  $V_i/L_m$ , i.e.,

$$i_{Q1} = \frac{I_o}{2N} + I_M + i_m = \frac{I_o}{2N} + i_m(T_0) + \frac{V_i}{L_m} \cdot (t - T_0) \quad (1)$$

The whole output current flows through diode  $D_1$ , as shown in Fig. 3.

Switch  $Q_1$  is turned off at  $t = T_1$ . During  $[T_1 - T_2]$  interval, capacitance  $C_{eq}$  is almost linearly charged from zero voltage to input voltage  $V_i$  by an approximately constant current,

$$i_{Ceq} \approx \frac{I_o}{N} + i_m(T_1) \quad (2)$$

At  $t = T_2$ , secondary voltage  $v_s$  reaches zero and diode  $D_2$  starts to conduct. During commutation of the output current from  $D_1$  to  $D_2$  and vice versa, leakage inductances  $L_{lkp}$  and  $L_{lks}$  play a significant role.

During  $[T_2 - T_3]$ , inductances  $L_{lkp}$  and  $L_{lks}$  resonate with

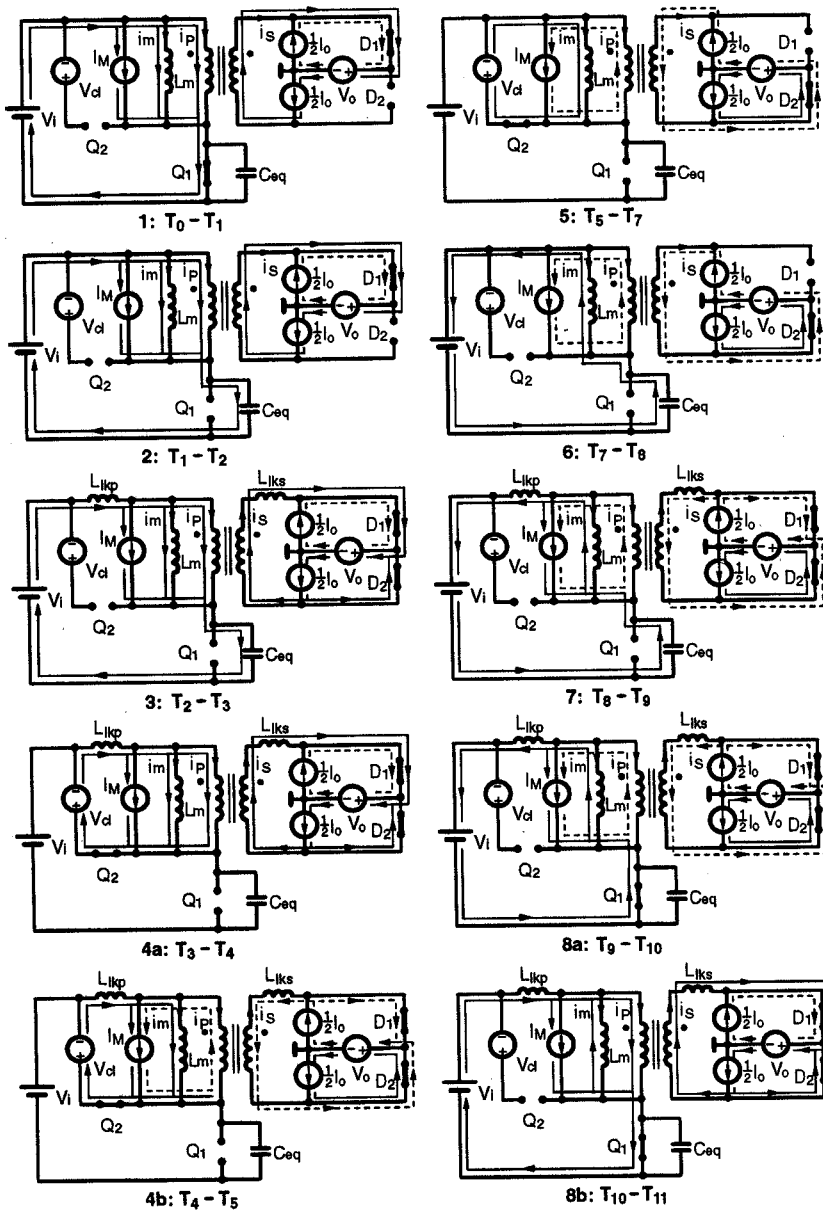


Fig. 3 Equivalent topological stages

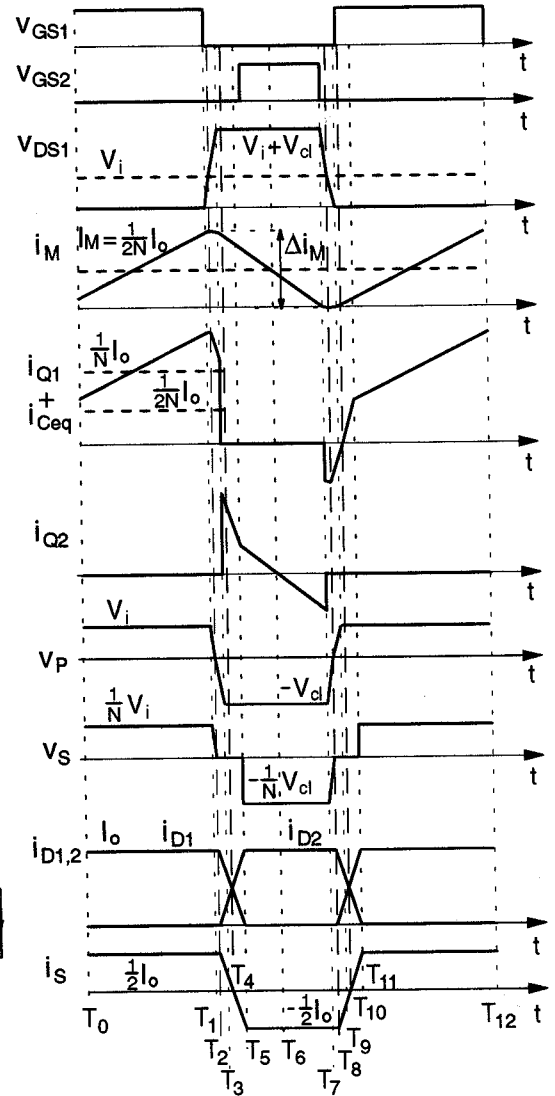


Fig. 4 Key waveforms

capacitance  $C_{eq}$ , as shown in the equivalent subcircuit in Fig. 5(a). It can be assumed that during commutation of the output current from  $D_1$  to  $D_2$ , the magnetizing current is approximately constant and equal to its maximum value:

$$i_M = i_M^{\max} = \frac{I_o}{2N} + \frac{\Delta i_M}{2}, \quad (3)$$

where  $\Delta i_M$  is the peak-to-peak variation of the magnetizing current. The constant magnetizing current flowing through leakage inductance  $L_{lkp}$  does not cause an additional voltage drop on  $L_{lkp}$  and, therefore, the subcircuit in Fig. 5(a) can be simplified as shown in Fig. 5(b). Notice that the current of the total equivalent leakage inductance,  $i_{Llk}$ , is equal to the reflected secondary current,  $i_s/N$ . Current  $i_{Llk}$  decreases in a resonant fashion,

$$i_{Llk} = -\left(\frac{I_o}{2N} + \frac{\Delta i_M}{2}\right) + \left(\frac{I_o}{N} + \frac{\Delta i_M}{2}\right) \cdot \cos(\omega_r(t - T_2)), \quad (4)$$

where

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_{eq}}} \quad (5)$$

is the angular resonant frequency. The voltage on  $C_{eq}$  during  $[T_2 - T_3]$  increases as

$$v_{Ceq} = V_i + V_r^+ \cdot \sin(\omega_r(t - T_2)), \quad (6)$$

where the amplitude of the sinusoidal component is

$$V_r^+ = Z_r \cdot \left(\frac{I_o}{N} + \frac{\Delta i_M}{2}\right), \quad (7)$$

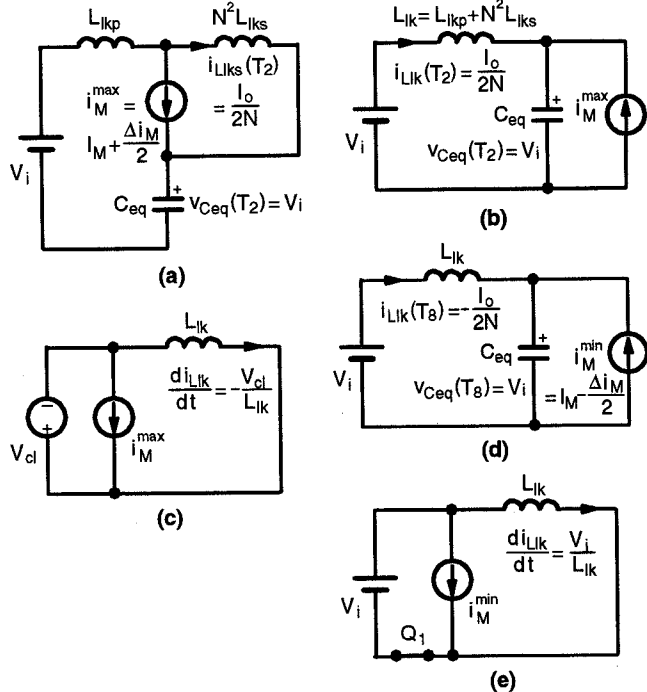


Fig. 5 Equivalent primary-side subcircuit during (a)-(b)  $[T_2 - T_3]$ , (c)  $[T_3 - T_3]$ , (d)  $[T_8 - T_8]$ , and (e)  $[T_9 - T_{11}]$  intervals

and

$$Z_r = \sqrt{\frac{L_{lk}}{C_{eq}}} \quad (8)$$

is the characteristic impedance of the resonant circuit in Fig. 5(b). Interval  $[T_2 - T_3]$  terminates either when voltage  $v_{Ceq}$  rises to  $V_i + V_{cl}$  and the clamp diode,  $D_{Q2}$ , starts to conduct or when the output current completely commutates from  $D_1$  to  $D_2$  and diode  $D_1$  turns off, whichever occurs first. Notice that for  $i_{D2} = I_o$ ,  $i_{Llk} = -I_o/(2N)$  is necessary. In Fig. 4, it is assumed that voltage  $v_{Ceq}$  reaches  $V_i + V_{cl}$  before diode  $D_2$  takes the full output current. The condition for this can be obtained from (4) and (6) as

$$\sqrt{1 - \left(\frac{V_{cl}}{V_r^+}\right)^2} > \frac{\frac{\Delta i_M}{2}}{\frac{I_o}{N} + \frac{\Delta i_M}{2}}. \quad (9)$$

For example, at  $\Delta i_M/2 = I_o/(2N)$ , as in Fig. 4, it follows from (9) that  $V_{cl} < 0.94 \cdot V_r^+$ .

During  $[T_3 - T_3]$  interval, the voltage on  $C_{eq}$  is clamped to  $V_i + V_{cl}$ . Using the same reasoning as during  $[T_2 - T_3]$  interval, the equivalent subcircuit during  $[T_3 - T_3]$  interval is obtained as shown in Fig. 5(c). The leakage-inductance current decreases with a constant slope,  $V_{cl}/L_{lk}$ . At  $t = T_4$ , secondary current changes sign. At  $t = T_5$ , diode current  $i_{D2}$  reaches the full output current and diode  $D_1$  turns off.

If during  $[T_2 - T_3]$  interval, the commutation of the output current from  $D_1$  to  $D_2$  completes before voltage  $v_{Ceq}$  reaches  $V_i + V_{cl}$ , then during  $[T_3 - T_3]$  interval capacitor  $C_{eq}$  will continue to be charged by the ac component of the magnetizing current ( $i_m = \Delta i_M/2$ ), as the entire dc component,  $I_M$ , is needed to support the negative secondary current,  $i_s = -I_o/2$ . In this case, voltage  $v_{Ceq}$  reaches  $V_i + V_{cl}$  and diode  $D_{Q2}$  starts to conduct at  $t = T_5$ .

During  $[T_5 - T_7]$  interval, the dc magnetizing current,  $I_M$ , supports the negative secondary current,  $i_s = -I_o/2$ , and the ac magnetizing current,  $i_m$ , flows through the clamp-voltage source,  $V_{cl}$ , decreasing with a constant slope,  $V_{cl}/L_m$ . During  $[T_5 - T_6]$   $i_m$  is positive and flows through diode  $D_{Q2}$ , and during  $[T_6 - T_7]$   $i_m$  is negative and flows through switch  $S_{Q2}$ . Switch  $S_{Q2}$  should be turned on during  $[T_5 - T_6]$  interval to assure turn on with zero voltage.

At  $t = T_7$ , switch  $S_{Q2}$  is turned off and ac magnetizing current  $i_m$  is commutated from switch  $S_{Q2}$  to capacitance  $C_{eq}$ . During  $[T_7 - T_8]$  interval, capacitance  $C_{eq}$  is almost linearly discharged from voltage  $V_i + V_{cl}$  to input voltage  $V_i$  by the ac magnetizing current, which can be approximated as constant during  $[T_7 - T_8]$ , i.e.,

$$i_{Ceq} = i_m \approx i_m(T_7). \quad (10)$$

At  $t = T_8$ , secondary voltage  $v_s$  reaches zero and diode  $D_1$  starts to conduct. During commutation of the output current

from  $D_2$  to  $D_1$ , the magnetizing current is approximately constant and equal to its minimum value:

$$i_M \approx i_M^{\min} = \frac{I_o}{2N} - \frac{\Delta i_M}{2} \quad (11)$$

Using again the same reasoning as during  $[T_2 - T_3]$  interval, the equivalent subcircuit during  $[T_8 - T_9]$  interval is obtained as shown in Fig. 5(d). The equivalent leakage inductance on the primary side of the transformer,  $L_{lk}$ , resonates with capacitance  $C_{eq}$ . Current  $i_{Llk}$ , which is equal to the reflected secondary current,  $i_s/N$ , and current  $i_{Ceq}$  increase in a resonant fashion:

$$i_{Llk} = -\frac{I_o}{2N} + \frac{\Delta i_M}{2} - \frac{\Delta i_M}{2} \cdot \cos(\omega_r(t - T_8)) \quad (12)$$

and

$$i_{Ceq} = -\frac{\Delta i_M}{2} \cdot \cos(\omega_r(t - T_8)) \quad (13)$$

The voltage on  $C_{eq}$  during  $[T_8 - T_9]$  decreases as

$$v_{Ceq} = V_i - V_r^- \cdot \sin(\omega_r(t - T_8)) \quad (14)$$

where

$$V_r^- = Z_r \cdot \frac{\Delta i_M}{2} \quad (15)$$

Interval  $[T_8 - T_9]$  terminates either when voltage  $v_{Ceq}$  decreases to zero and diode  $D_{Q1}$  starts to conduct or when the output current completely commutates from  $D_2$  to  $D_1$  and diode  $D_2$  turns off, whichever occurs first. In Fig. 4, it is assumed that voltage  $v_{Ceq}$  decreases to zero before diode  $D_1$  takes the full output current. The condition for this can be obtained from (12) and (14) as

$$\sqrt{1 - \left(\frac{V_i}{V_r^-}\right)^2} > \frac{-\frac{I_o}{N} + \frac{\Delta i_M}{2}}{\frac{\Delta i_M}{2}} \quad (16)$$

For all cases  $\Delta i_M/2 < I_o/N$ , which also includes the example in Fig. 4 ( $\Delta i_M/2 = I_o/(2N)$ ), the only condition required to satisfy (16) is  $V_i < V_r^-$ .

During  $[T_9 - T_{11}]$  interval, the voltage on  $C_{eq}$  is equal to zero. Using the same reasoning as during  $[T_2 - T_3]$  interval, the equivalent subcircuit during  $[T_9 - T_{11}]$  interval is obtained as shown in Fig. 5(e). Leakage-inductance current  $i_{Llk}$  and switch current  $i_{Q1}$  increase with a constant slope,  $V_i/L_{lk}$ . During  $[T_9 - T_{10}]$  interval, current  $i_{Q1}$  is negative and flows through diode  $D_{Q1}$ . Switch  $S_{Q1}$  should be turned on during this interval; that results in turn on at zero voltage. During  $[T_{10} - T_{11}]$  interval, current  $i_{Q1}$  is positive and it flows through switch  $S_{Q1}$ . At  $t = T_{11}$ , diode current  $i_{D1}$  reaches the full output current and diode  $D_2$  turns off, starting the next switching cycle.

### III. DESIGN

The design of the forward converter with CDR is illustrated on a 3.3-V, 50-A dc/dc converter for the 40-60-V input-voltage range. The key design parameters are the minimum and maximum duty cycles,  $D_{\min}$  and  $D_{\max}$ , the turns ratio of the transformer,  $N$ , the switching frequency,  $f_s$ , and the air-gap length,  $l_g$ , of the selected transformer core.

The output voltage of the CDR forward converter in continuous conduction mode (CCM) of operation is determined by the same expression as the output voltage of the conventional forward converter in CCM:

$$V_o = D \cdot \frac{V_i}{N} - V_F \quad (17)$$

where  $V_F$  is the forward-voltage drop on the secondary-side diodes. From (17), the ratio of the maximum and minimum duty cycles is obtained as

$$\frac{D_{\max}}{D_{\min}} = \frac{V_{i\max}}{V_{i\min}} = 1.5 \quad (18)$$

The conventional design approach of the active-clamp forward converter is to minimize the switch voltage stress over the input voltage range, i.e., to ensure equal switch voltage stress at minimum and maximum input voltages. The voltage stress on both switches,  $Q_1$  and  $Q_2$  in Fig. 1, is equal to  $V_i + V_{cl}$ . The clamp voltage is obtained from the flux balance of the transformer:

$$V_{cl} = \frac{D}{1-D} \cdot V_i \quad (19)$$

Using (19), the voltage stress on both switches is

$$V_{Q\max} = \frac{V_i}{1-D} \quad (20)$$

The condition for equal switch-voltage stress at minimum and maximum input voltages is obtained from (18) and (20) as

$$D_{\max} + D_{\min} = 1 \quad (21)$$

It follows from (18) and (21) that  $D_{\min} = 0.4$  and  $D_{\max} = 0.6$ . Then, from (17), the transformer turns ratio  $N = 6.6 \approx 7$  is obtained, where  $V_F = 0.35$  V was used. Substituting back in (17), the corrected minimum and maximum duty-cycles are  $D_{\min} = 0.43$  and  $D_{\max} = 0.64$ . From (20), the switch voltage stresses are  $V_{Q}(V_{i\min}) = 110.8$  V and  $V_{Q}(V_{i\max}) = 104.5$  V. For the switches, 200-V mosfets were selected as shown in Fig. 6. The voltage stresses on the secondary-side diodes are

$$V_{D1\max} = \frac{V_{cl\max}}{N} - V_F = 10.1 \text{ V} \quad (22)$$

and

$$V_{D2\max} = \frac{V_{i\max}}{N} - V_F = 8.2 \text{ V} \quad (23)$$

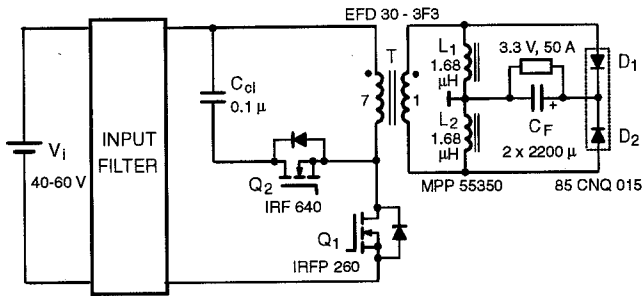


Fig. 6 Experimental circuit diagram

As can be seen from (22) and (23), for secondary-side diodes 15-V Schottky diodes—which have the lowest forward-voltage drop—can be employed.

Using Faraday's law and (17), the transformer-flux excursion is obtained as

$$\Delta B = \frac{V_o + V_F}{N_S A_c f_s}, \quad (24)$$

where  $N_S$  is the number of secondary turns and  $A_c$  is the effective cross-sectional area of the transformer core. To minimize the transformer-secondary copper loss,  $N_S = 1$  is selected. Choosing the switching frequency  $f_s = 250$  kHz and selecting the economic-flat-design core EFD30-3F3 [8],  $\Delta B = 212$  mT is obtained.

The air-gap length is determined from the required stored energy in the transformer. Choosing  $B_{max} = \Delta B$ , the stored energy in the transformer is

$$W_c = \frac{A_c \cdot B_{max}^2}{2\mu_o} \left( l_g + \frac{l_c}{\mu_a} \right) = \frac{V_o I_o \max}{2\eta_{min} f_s}, \quad (25)$$

where  $l_c$  is the effective core length,  $\mu_a$  is the amplitude permeability, and  $\eta_{min}$  is the estimated minimum efficiency. With  $\eta_{min} = 0.85$ , from (25), the air-gap length  $l_g = 0.3$  mm = 12 mil is obtained. The transformer primary and secondary windings are implemented with 2 strands of 150/42 Litz wire and 2 strands of 5-mil copper foil, respectively.

Each of the secondary-side inductors,  $L_1$  and  $L_2$ , is implemented with one molypermalloy powder (MPP) core 55350 and 4 turns, 4 strands of wire AWG 17, resulting in  $L_1 = L_2 = 1.68$   $\mu$ H.

The control circuit is based on the conventional low-cost, current-mode, PWM controller chip 3843.

#### IV. EXPERIMENTAL RESULTS

For experimental evaluation of the forward converter with CDR vs. the conventional forward converter, the circuit shown in Fig. 6 was built. For the conventional forward converter, the same circuit was used, only the output filter inductor and the transformer gap were different: the output

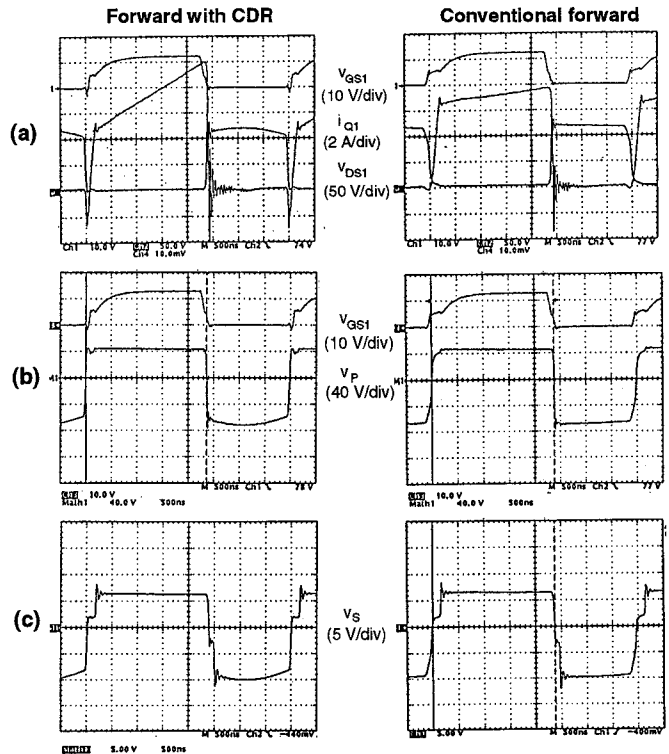


Fig. 7 Experimental waveforms of (a) main-switch voltages and currents, (b) transformer primary voltage, and (c) transformer secondary voltage at nominal input voltage ( $V_i = 48$  V) and full load ( $I_o = 50$  A)

filter inductor was implemented with one MPP core 55930—which has about the same volume and weight as the two cores used in the forward converter with CDR—and 3 turns, 6 strands of wire AWG 17, resulting in 1.41- $\mu$ H inductance; the transformer gap was reduced to zero. Comparative experimental waveforms of the main-switch voltages and currents as well as of the transformer primary and secondary voltages at nominal input voltage  $V_i = 48$  V and full load ( $I_o = 50$  A) are shown in Fig. 7. As can be seen, the corresponding waveforms of the CDR and conventional forward converters are very similar, except for the main-switch current waveform,  $i_{Q1}$ . The switch current of the CDR forward converter is significantly steeper during on time. In fact, the transformer of the CDR forward converter has a significantly lower magnetizing inductance in order to generate the dc magnetizing current needed to support the secondary current during off time. The switch voltage and current waveforms of the CDR forward converter in Fig. 7(a) nicely illustrate the ZVS at turn on. It should be noticed that the secondary voltage in Fig. 7(c) is different from zero during output-current commutation intervals. This is caused by the additional voltage drop on the series inductances of diodes  $D_1$  and  $D_2$ , which was neglected in the analysis in Section II. In fact, the series inductances of the secondary-side diodes increase the commutation time of the output current between the two diodes.

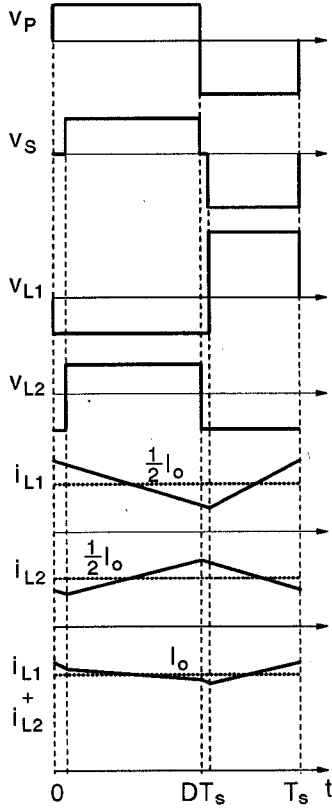


Fig. 8 Ripple cancellation

## V. EVALUATION

The most important advantages of the CDR forward converter vs. the conventional forward converter are:

- lower transformer-secondary copper loss,
- lower main-switch turn-on loss due to ZVS, and
- ripple cancellation seen by the output filter capacitor and secondary-side diodes (see Fig. 8).

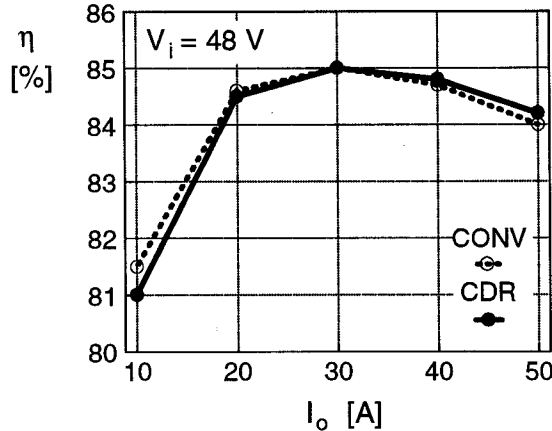


Fig. 9 Efficiency measurements

The disadvantages of the CDR forward converter are:

- higher transformer-primary copper loss,
- higher transformer core loss,
- higher conduction loss of both switches, and
- higher turn-off loss of both switches.

Whether the advantages will prevail over the disadvantages depends on input and output conditions. As an example, efficiency and temperature measurements of the experimental CDR and conventional forward converters at nominal input voltage  $V_i = 48$  V and five different output currents are shown in Fig. 9 and Table I, respectively. At light load ( $I_o = 10$  A), the CDR forward converter has a slightly lower efficiency, which is due to a higher core loss and higher clamp-switch loss, as it follows from Table I. At full load ( $I_o = 50$  A), a lower secondary-copper loss of the CDR forward converter has the dominant effect, resulting in a slightly higher efficiency of the CDR forward converter. In fact, the benefits of the ZVS turn-on of the CDR forward converter will become fully advantageous only at higher input voltages as, for example, in off-line applications.

TABLE I  
TEMPERATURE MEASUREMENTS ( $V_i = 48$  V)

$I_o$ [A]	$T(Q_1)$ [°C]		$T(Q_2)$ [°C]		$T(XF_{Fe})$ [°C]		$T(XF_{Cu})$ [°C]	
	CDR	CONV	CDR	CONV	CDR	CONV	CDR	CONV
10	28	28	28	23	34	32	30	30
20	32	32	28	23	38	34	34	34
30	37	36	30	24	41	37	39	39
40	44	42	32	25	45	42	45	48
50	56	52	34	26	51	46	51	56

The transformer-secondary copper loss is determined as [9],

$$P_{Cu,S} = R_{S,dc} I_{S,dc}^2 + \sum_{n=1}^{\infty} R_{S,ac,n} I_{S,ac,n}^2 = R_{S,ac}^{PWM} I_{S,rms}^2, \quad (26)$$

where  $R_{S,dc}$  is the dc resistance of the transformer-secondary copper,  $R_{S,ac,n}$  is its ac resistance at the  $n$ -th harmonic of the switching frequency,  $R_{S,ac}^{PWM}$  is the total ac resistance of the transformer-secondary copper carrying a PWM (squarewave) current,  $I_{S,dc}$  is the dc component of transformer-secondary current  $i_S$ ,  $I_{S,ac,n}$  is the rms of the  $n$ -th harmonic of current  $i_S$ , and  $I_{S,rms}$  is the rms of the total secondary current. The current components of the CDR and conventional forward converters are summarized in Table II. The ac component,  $I_{S,ac}$ , is determined as

$$I_{S,ac}^2 = \sum_{n=1}^{\infty} I_{S,ac,n}^2 = I_{S,rms}^2 - I_{S,dc}^2. \quad (27)$$

Notice that the ac components in Table II are identical.

TABLE II  
TRANSFORMER-SECONDARY CURRENT COMPONENTS

FORWARD CONVERTER	CDR	CONV
$i_s$ waveform		
$I_{s,dc}$	$I_o (D - 0.5)$	$I_o D$
$I_{s,rms}$	$0.5 I_o$	$I_o \sqrt{D}$
$I_{s,ac}$	$I_o \sqrt{D(1-D)}$	$I_o \sqrt{D(1-D)}$

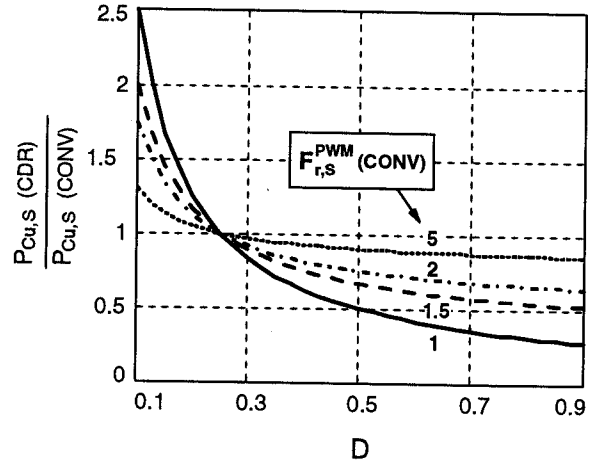


Fig. 10 Ratio of transformer-secondary copper losses of CDR and conventional forward converters

The ratio of the transformer-secondary copper losses of the CDR and conventional forward converters is obtained as

$$\frac{P_{Cu,s}(\text{CDR})}{P_{Cu,s}(\text{CONV})} = \frac{F_{r,s}^{PWM}(\text{CONV}) - 1 + \frac{0.25}{D}}{F_{r,s}^{PWM}(\text{CONV})}, \quad (28)$$

where

$$F_{r,s}^{PWM}(\text{CONV}) = \frac{R_{S,ac}^{PWM}(\text{CONV})}{R_{S,dc}} \quad (29)$$

is the ratio of the transformer-secondary ac and dc resistances of the conventional forward converter (with unipolar squarewave secondary current). This ratio is determined as [10]

$$F_{r,s}^{PWM}(\text{CONV}) = D \left[ 1 + 2 \sum_{n=1}^{\infty} \frac{R_{S,ac,n}}{R_{S,dc}} \cdot \left( \frac{\sin(n\pi D)}{n\pi D} \right)^2 \right]. \quad (30)$$

As can be seen from Fig. 10, the CDR forward converter has lower transformer-secondary copper losses only if the ac resistance of the secondary winding is not significantly larger than its dc resistance, i.e. for small values of  $F_{r,s}^{PWM}(\text{CONV})$ .

For the experimental converter, the calculated value of  $F_{r,s}^{PWM}(\text{CONV})$  at nominal input voltage  $V_i = 48$  V ( $D = 0.53$ ) and full load ( $I_o = 50$  A) is  $\approx 1.7$ , which, from (28), results in a decreased transformer-secondary copper loss of the CDR forward converter by about 31% compared to that of the conventional forward converter. This is in good agreement with the measurements. As shown in Fig. 10, for duty cycles  $D < 0.25$ , the CDR forward converter has higher transformer-secondary copper loss than its conventional counterpart.

## VI. SUMMARY

A thorough analysis of the forward converter with the current doubler rectifier (CDR) is performed. To facilitate the understanding of operation, the converter circuit in each topological stage within a switching cycle is reduced to a first- or second-order equivalent circuit. The design of the forward converter with CDR is illustrated on a 3.3-V, 50-A dc/dc converter for the 40-60-V input-voltage range. Advantages and disadvantages of the CDR forward converter vs. the conventional forward converter are theoretically and experimentally evaluated. The transformer-secondary copper losses are examined carefully.

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