

# Design Considerations and Performance Evaluations of Synchronous Rectification in Flyback Converters\*

Michael T. Zhang<sup>1</sup>, Milan M. Jovanović<sup>2</sup>, and Fred C. Lee<sup>1</sup>

<sup>1</sup>Virginia Power Electronics Center, The Bradley Department of Electrical Engineering  
Virginia Polytechnic Institute and State University, Blacksburg, VA 24061-0111

<sup>2</sup>Delta Power Electronics Lab., Inc., 1872 Pratt Drive, Blacksburg, VA 24060

**Abstract** — Design trade-offs and performance comparisons of various implementations of the flyback converter with a synchronous rectifier are presented. Specifically, the merits and limitations of the constant-frequency (CF) continuous-conduction-mode, CF discontinuous-conduction-mode (DCM), variable-frequency DCM, and zero-voltage-switched DCM flyback converters with synchronous rectifiers are discussed. The theoretical efficiency improvements of the discussed synchronous rectification approaches relative to Schottky diode implementations are derived. Finally, theoretical results are verified on an experimental, universal-input, off-line, 15-V/36-W flyback prototype.

## I. Introduction

Generally, in low-output-voltage power supplies, the conduction loss of the diode rectifier due to its forward voltage drop is the dominant loss component. In power supplies with the output voltage not too many times higher than the rectifier forward voltage drop, the diode rectifier loss accounts for more than 50% of the total power loss. The rectification loss can be reduced by replacing the diode rectifier with a synchronous rectifier (SR), i.e., with a low-on-resistance MOSFET [1], [2]. Synchronous rectification is most often applied to the buck and buck-derived isolated topologies, which are suitable for step-down, low-output-voltage applications [2]. Generally, in the isolated buck-derived topologies, such as the forward, bridge-type, and push-pull converters, synchronous rectification can be implemented by a direct replacement of the diode rectifiers with low-voltage MOSFETs [3], [4]. Namely, in these self-driven SR implementations, the secondary voltage of the transformer is used to directly drive the SRs, thus reducing the circuit complexity and cost without sacrificing the efficiency.

A number of applications of the SR in the flyback converter have also been reported [5]-[7]. However, in all of these applications, the main purpose of the SR was to provide the post-regulation of the output voltage and not to maximize the conversion efficiency. Specifically, in [5]-[7], the SR is

used as a voltage-controlled resistor in a control loop which adjusts the SR's resistance so that the output voltage is maintained within the regulation range. Generally, the regulation range of these post-regulation approaches is limited to the forward voltage drop of the SR body diode, i.e.,  $\sim 0.7$  V. Moreover, since the voltage drop across the SR is not minimized because of the resistance modulation, the conversion efficiency of these post regulators is reduced, compared to that of the converter with the "true" SR.

The objective of this paper is to evaluate the theoretical and practical limits of the efficiency improvements for various implementations of the flyback converter with the SR with respect to the corresponding converter with the diode rectifier. Specifically, the design considerations and performance evaluations of the constant-frequency (CF) continuous-conduction-mode (CCM), CF discontinuous-conduction-mode (DCM), variable-frequency (VF) DCM, and zero-voltage-switched (ZVS) DCM flyback converters with the SR are discussed.

## II. Synchronous Rectifier Implementations

A flyback converter with the SR is shown in Fig. 1. For proper operation of the converter, conduction periods of primary switch  $SW$  and secondary-side switch  $SR$  must not overlap. To avoid the simultaneous conduction of the  $SW$  and the  $SR$ , a delay between the turn-off instant of switch  $SW$  and the turn-on instant of the  $SR$  as well as between the turn-on instant of the  $SW$  and turn-off instant of the  $SR$  must be introduced in the gate-drive waveforms of the switches. With properly designed gate drives, the operation of the circuit shown in Fig. 1 is identical to that with a conventional diode rectifier. Namely, during the time switch  $SW$  is turned on, energy is stored in the transformer magnetizing inductance and transferred to the output after  $SW$  is turned off.

Generally, the circuit shown in Fig. 1 can work in CCM or DCM either with a constant or variable switching frequency PWM control. Design considerations and SR loss estimates for various modes of operation and different control approaches are given next.

\* This work was supported by Delta Electronic Ind. Co., Ltd., Taiwan.

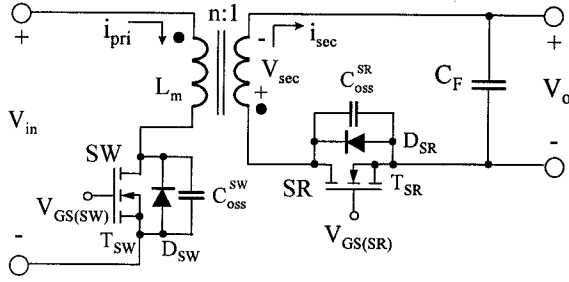


Fig. 1. Flyback converter with synchronous rectifier.

### A. Constant-Frequency (CF) Continuous-Conduction-Mode (CCM)

The key waveforms of the flyback converter with the SR operating in CCM are given in Fig. 2. As can be seen from Fig. 2, during delay times  $T_D^{on}$  and  $T_D^{off}$ , secondary current  $i_{sec}$  flows through the body diode of the SR. The conduction of body diode  $D_{SR}$  not only increases the conduction loss, but also introduces a reverse-recovery loss when primary switch  $SW$  is turned on. The conduction loss of the SR is given by the sum of the channel-resistance loss and body-diode loss as

$$P_{cond}^{SR} = R_{DS(on)} \left[ \frac{I_o^2}{1-D} + \frac{\Delta I_{sec}^2 (1-D)}{12} \right] + V_D I_D (T_D^{on} + T_D^{off}) f_s, \quad (1)$$

where  $R_{DS(on)}$  is the SR on-resistance,  $D = T_{on}/T_s$  is the duty-ratio,  $I_o$  is the output current,  $\Delta I_{sec}$  is the secondary peak-to-peak ripple current,  $V_D$  and  $I_D$  are the forward voltage drop and current of the body diode, respectively.

The reverse-recovery loss of the SR body diode is given by

$$P_{RR}^{SR} = Q_{RR} (V_o + \frac{V_{in}}{n}) f_s, \quad (2)$$

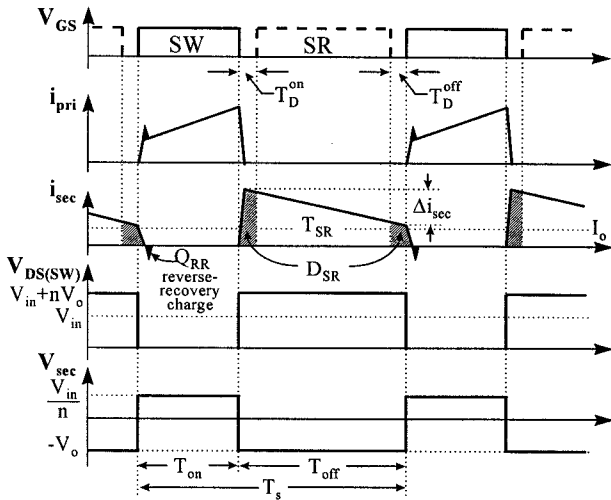


Fig. 2. Key waveforms of CF CCM flyback converter with SR. Body diode of SR conducts in shaded area (■).

where  $Q_{RR}$  is the recovered charge of the SR body diode, and  $V_o + V_{in}/n$  is the steady-state reverse voltage across the SR.

In addition to  $P_{cond}^{SR}$  and  $P_{RR}^{SR}$  losses, the CF CCM converter in Fig. 1 exhibits a loss each time the SR is turned off (i.e., each time the  $SW$  is turned on) because of a parasitic resonance between  $C_{oss}^{SR}$  and the leakage inductance of the transformer (see Fig. 9). Since the parasitic resonance must be damped by a snubber to limit the maximum voltage across the SR, the resonance dies out completely before SR is turned on again. As a result, the power loss due to this parasitic resonance can be calculated from

$$P_{off}^{SR} = \frac{1}{2} C_{oss}^{SR} (V_o + \frac{V_{in}}{n})^2 f_s. \quad (3)$$

Finally, for proper operation of the circuit, the  $SR$  must be turned off before primary switch  $SW$  is turned on (delay time  $T_D^{off}$  in Fig. 2). Therefore, the flyback converter with the SR cannot be self-driven from the secondary winding of the transformer. In fact, the circuit shown in Fig. 1 requires an external control circuit to turn off the SR.

### B. CF Discontinuous-Conduction-Mode (DCM)

The key waveforms of the constant-frequency flyback converter with the SR operating in DCM are shown in Fig. 3. In DCM, the energy stored in the magnetizing inductance of the transformer during the on time of switch  $SW$  is completely discharged during the subsequent off time. As can be seen from Fig. 3, secondary current  $i_{sec}$  reaches zero before primary switch  $SW$  is turned on. To prevent the discharging of the output filter capacitor through a conducting SR, the SR channel conduction (transistor  $T_{SR}$ ) must be terminated at the moment  $i_{sec}$  reaches zero, or a short while after. Therefore, the DCM flyback converter with the SR requires a zero-current-crossing detector in the control circuit.

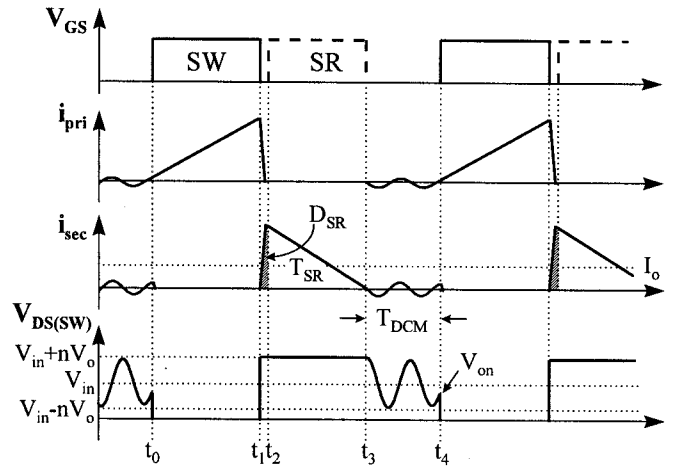


Fig. 3. Key waveforms of CF DCM flyback converter with SR. Body diode of SR conducts in shaded area (■).

After the SR is turned off, the magnetizing inductance of the transformer  $L_m$  and capacitance  $C_{eq} = C_{oss}^{SW} + C_{oss}^{SR} / n^2$  starts resonating, as shown in Fig. 3. For a converter with a regulated output, the duration of resonant interval  $T_{DCM}$  in Fig. 3 changes significantly with the input voltage and less dramatically with the output current. As a result, the voltage across the primary switch at the moment of its turn on can range anywhere between  $V_{in} + nV_o$  and  $V_{in} - nV_o$ , producing the capacitive turn-on loss of

$$P_{cap(SW)} = \frac{1}{2} C_{oss}^{SW} V_{on}^2 f_s, \quad (4)$$

where  $V_{in} - nV_o \leq V_{on} \leq V_{in} + nV_o$ . Since  $P_{cap(SW)}$  is maximum at the peaks of the  $V_{DS(SW)}$  oscillation and minimum at its valleys, the efficiency of the converter shows strong fluctuations with the input voltage. In addition, because typical SRs have a much larger output capacitance  $C_{oss}^{SR}$  than the Schottky rectifiers, the characteristic impedance,  $Z_m = \sqrt{L_m / C_{eq}}$ , of the resonant tank consisting of  $L_m$  and  $C_{eq}$  is much lower for the converter with an SR compared to that with a Schottky diode. As a result, the resonant-tank current of the converter with an SR is much higher than that of the converter with a Schottky, causing a larger conduction loss. For certain line and load conditions, this power loss can completely offset the power-loss savings obtained by the SR, making the efficiency of the converter with the SR lower than that of the converter with the diode rectifier.

Finally, it should be noted that in the DCM flyback converter reverse-rectifier loss  $P_{RR}^{SR}$  is eliminated because the rectifier current becomes zero before primary switch  $SW$  is turned on.

### C. Variable-Frequency (VF) DCM

Capacitive switching loss  $P_{cap(SW)}$  can be minimized, and parasitic oscillation caused by the interaction of  $L_m$  and  $C_{eq}$  can be eliminated if the primary switch  $SW$  is turned on at the moment  $V_{DS(SW)}$  reaches its minimum voltage,  $V_{in} - nV_o$ , the first time after the SR is turned off, as shown in Fig. 4. This can be accomplished by sensing the zero-current-crossing of  $i_{sec}$  and turning on  $SW$  after a constant delay  $T_{delay}$  which is equal to one half of the parasitic-resonance period, i.e.,

$$T_{delay} = \pi \sqrt{L_m C_{eq}}. \quad (5)$$

With this variable-frequency control, the efficiency fluctuations with the input voltage are eliminated. It should be noted that with the VF control, the switching frequency is minimum at low line and full load, and it increases as the line increases and/or load decreases.

The conversion efficiency at low line of the variable-frequency DCM converter can be always made higher than the efficiency of the corresponding constant-frequency

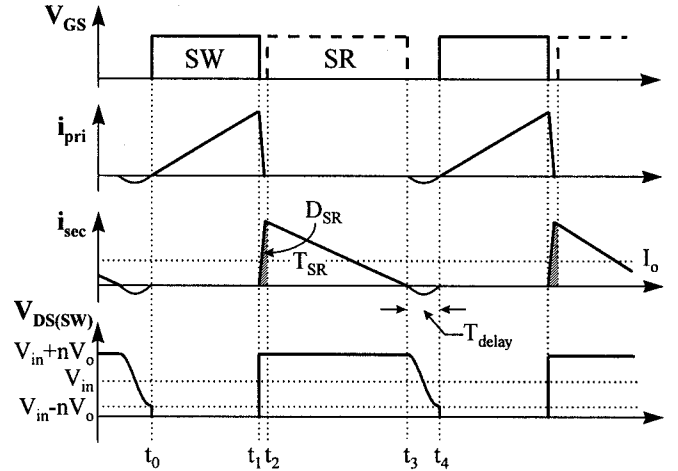


Fig. 4. Key waveforms of VF DCM flyback converter with SR. Body diode of SR conducts in shaded area (■).

counterpart. In addition, the high-line efficiency of the VF DCM converter can also be higher than that of the CF DCM implementation if the power-loss savings due to elimination of the parasitic oscillations and the minimization of the turn-on voltage  $V_{on}$  are lower than the increased switching losses and magnetic losses due to the increased switching frequency.

### D. VF Zero-Voltage-Switched (ZVS) DCM

As can be seen from Fig. 4, if the amplitude of the oscillation after the turn-off of the SR is larger than the input voltage, i.e., if

$$V_{in} < nV_o, \quad (6)$$

primary-switch voltage  $V_{DS(SW)}$  will fall to zero before the switch is turned on at the moment  $t_4 = t_3 + T_{delay}$ . Therefore, for  $V_{in} < nV_o$ , the VF flyback converter can achieve ZVS, i.e., the capacitive turn-on loss of the primary switch can be eliminated. While the ZVS condition in Eq. (6) may be met for certain designs at low input-voltages, generally it is not met at higher input voltages. As a result, at higher input voltages, the VF flyback converter with gate-drive timing given in Fig. 4 operates with partial ZVS.

However, the complete ZVS of the primary switch in the VF flyback converter with the SR can be achieved in the entire input-voltage range if the turn-off instant of the SR after the secondary current zero-crossing is delayed enough to allow a negative secondary current to build up, as shown in Fig. 5. To achieve ZVS in the entire input-voltage range, the energy stored in magnetizing inductance  $L_m$  by the negative secondary current  $I_{ZVS}$  must be large enough to discharge primary switch capacitance  $C_{oss}^{SW}$  from voltage  $V_{in} + nV_o$  down to zero, i.e.,

$$I_{ZVS} \geq \frac{n \sqrt{V_{in(max)}^2 - (nV_o)^2}}{Z_m}. \quad (7)$$

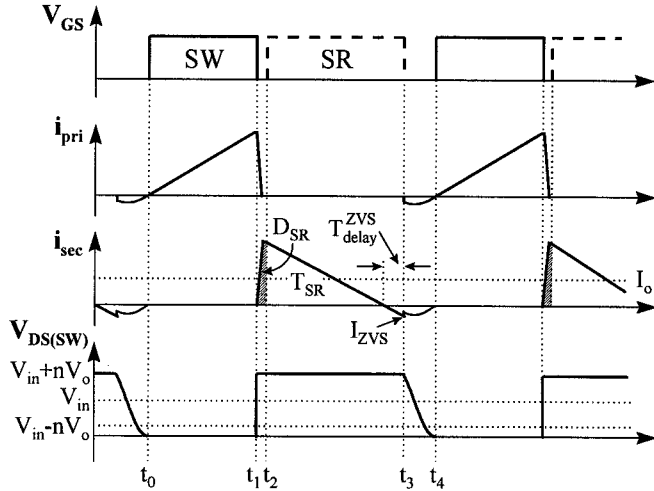


Fig. 5. Key waveforms of VF ZVS DCM operation.

Therefore, to build up the necessary  $I_{ZVS}$ , the turn-off of the SR should be delayed after the zero-crossing of  $i_{sec}$  for

$$T_{delay}^{ZVS} = \frac{L_m \cdot I_{ZVS}}{n^2 \cdot V_o}, \quad (8)$$

as shown in Fig. 5.

Finally, it should be noted that in VF ZVS DCM flyback converter with the SR the capacitive turn-on switching loss of the primary switch is traded off for the conduction loss. Namely, according to Fig. 5, due to the negative secondary current, the RMS value of the secondary current is slightly increased. Therefore, the VF ZVS converter in Fig. 5 might not necessarily achieve higher efficiency compared to the VF converter with partial ZVS (Fig. 4).

### III. SR Efficiency Improvement Estimates

Generally, in a flyback converter, the substitution of the diode rectifier with an SR affects the conduction and switching losses of the rectifier. In addition, the employment of an SR allows for the implementation of VF flyback converter with complete ZVS, i.e., without any primary-switch capacitive turn-on switching loss  $P_{cap(SW)}$ . Table I summarizes theoretical rectifier conduction loss  $P_{cond}$ , rectifier switching losses,  $P_{sw} = P_{off} + P_{RR}$ , and the primary switching loss,  $P_{cap(SW)}$ , of the flyback converter with diode rectifier (DR) and the SR.

The efficiency of a converter with the diode rectifier can be expressed as

$$\eta_{DR} = \frac{P_o}{P_o + P_{cond}^{DR} + P_{sw}^{DR} + P_{cap(SW)}^{DR} + P_{other}}, \quad (9)$$

where  $P_o$  is the output power and  $P_{other}$  is the loss other than the conduction and switching losses of the rectifier, and the capacitive turn-on switching loss of the primary switch.

Similarly, the efficiency of the flyback converter with the SR can be written as

$$\eta_{SR} = \frac{P_o}{P_o + P_{cond}^{SR} + P_{sw}^{SR} + P_{cap(SW)}^{SR} + P_{other}}. \quad (10)$$

By eliminating  $P_{other}$  from Eqs. (9) and (10), the efficiency difference between the SR and the diode rectifier implementations can be calculated as

$$\Delta\eta = \eta_{SR} - \eta_{DR} = \frac{\Delta P_{REC} \eta_{DR}^2}{P_o - \Delta P_{REC} \eta_{DR}}, \quad (11)$$

where,

TABLE I  
Power loss comparisons of flyback converters with diode (DR) rectifier and synchronous rectifier (SR).

		CF CCM	CF DCM	VF DCM	VF ZVS DCM
$P_{cond}$	DR	$V_F I_o$	$V_F I_o$	$V_F I_o$	not possible to implement
	SR	$R_{DS(on)} \left[ \frac{I_o^2}{1-D} + \frac{\Delta I_{sec}^2 (1-D)}{12} \right] + V_D I_D (T_D^{on} + T_D^{off}) f_s$	$R_{DS(on)} \frac{4I_o^2}{3(1-D)}$	$R_{DS(on)} \frac{4I_o^2}{3(1-D)}$	$R_{DS(on)} \left[ \frac{4I_o^2}{3(1-D)} + \frac{I_{ZVS} [2I_o + I_{ZVS} (1-D)]}{3} \right]$
$P_{sw} = P_{off} + P_{RR}$	DR†	$\left[ \frac{C_T}{2} \left( V_o + \frac{V_{in}}{n} \right)^2 + Q_{RR}^{DR} \left( V_o + \frac{V_{in}}{n} \right) \right] f_s$	0	0	not possible to implement
	SR	$\left[ \frac{C_{oss}^{SR}}{2} \left( V_o + \frac{V_{in}}{n} \right)^2 + Q_{RR}^{SR} \left( V_o + \frac{V_{in}}{n} \right) \right] f_s$	0	0	0
$P_{cap(SW)}$	DR	$\frac{C_{oss}^{SW}}{2} (V_{in} + nV_o)^2 f_s$	$\frac{C_{oss}^{SW}}{2} V_{on}^2 f_s$	$\frac{C_{oss}^{SW}}{2} (V_{in} - nV_o)^2 f_s$	not possible to implement
	SR	$\frac{C_{oss}^{SW}}{2} (V_{in} + nV_o)^2 f_s$	$\frac{C_{oss}^{SW}}{2} V_{on}^2 f_s$	$\frac{C_{oss}^{SW}}{2} (V_{in} - nV_o)^2 f_s$	0

† Note that for Schottky rectifiers,  $Q_{RR} \approx 0$ .

$$\Delta P_{REC} = (P_{cond}^{DR} - P_{cond}^{SR}) + (P_{sw}^{DR} - P_{sw}^{SR}) + (P_{cap(SW)}^{DR} - P_{cap(SW)}^{SR}). \quad (12)$$

Using the power loss expressions from Table I and knowing the device characteristics and the circuit parameters, the efficiency improvement of the flyback converter with the SR can be calculated. As an example, Fig. 6 presents the calculated efficiencies for the discussed four implementations of the converter with the SR as functions of the load current. In Fig. 6, it is assumed that the diode rectifier versions of the converter have conversion efficiencies of 89%, which correspond to the efficiencies of the experimental circuit discussed in the next section.

As can be seen from Fig. 6, the efficiency of the ZVS DCM implementation (solid line) is highest at low power levels (i.e., for  $I_o \leq 5-6$  A) because the switching turn-on loss of the primary switch contributes significantly to the total loss in the other implementations. For the same range of the output power, the CF CCM implementation exhibits the lowest efficiency due to the dominant effect of the turn-on switching loss of the primary switch and the turn-off switching loss of the SR. For example, at  $I_o = 2.4$  A (which corresponds to the full-load current of the experimental converter presented in the next section), the efficiency of the ZVS DCM implementation with the SR is approximately 3% higher than the efficiency of the corresponding circuit with the Schottky rectifier. However, at  $I_o = 2.4$  A, the efficiency of the CCM implementation with the SR at  $I_o = 2.4$  A is 1% lower than the efficiency of the same circuit with the Schottky rectifier.

At higher power levels, the conduction losses of the primary switch and the SR start dominating the total loss. As a result, the CF CCM implementation exhibits the highest efficiency at  $I_o > 15$  A due to its smallest primary and secondary RMS currents. On the other hand, the efficiency of the CF DCM implementation monolithically decreases as the load current (output power) increases. In fact, as can be seen from Fig. 6, for  $I_o > 10$  A the efficiency of the CF DCM

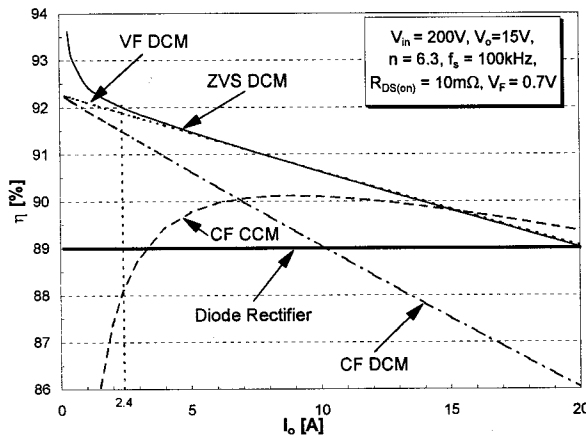


Fig. 6. Theoretical efficiency estimates.

implementation is lower than that of the Schottky implementation. Also, as the load current, and therefore the conduction losses, become larger, the efficiencies of the VF DCM and ZVS DCM implementations converge because the power savings brought about by soft-switching in ZVS DCM implementation are less significant.

Finally, as the output current continues to increase, so that the voltage drop across the SR,  $R_{DS(on)}i_{RMS}$ , approaches that of the Schottky rectifier  $V_F$ , the efficiencies of the CF CCM, VF DCM, and ZVS DCM implementations approach that of the Schottky-rectifier implementation. As can be seen from Fig. 6, at  $I_o = 20$  A the efficiencies of the VF DCM and ZVS DCM implementations fall to the level of the Schottky implementation efficiency. The CF CCM implementation efficiency drops to that of the Schottky-rectifier implementation at  $I_o > 20$  A due to lower  $i_{sec}^{RMS}$ . The only way to achieve efficiency improvements at higher load currents i.e., when  $R_{DS(on)}i_{RMS} \approx V_F$ , is to resort to paralleling of SRs in order to reduce the effective  $R_{DS(on)}$ .

#### IV. Evaluation Results

The discussed SR implementations were experimentally evaluated on a 15-V/2.4-A flyback converter designed to operate in the 100-370 Vdc input-voltage range. The diode-version power stages were implemented with Motorola MTP6N60 ( $V_{RRM} = 600$  V,  $R_{DS(on)} = 1.2 \Omega @ T_j = 25^\circ\text{C}$ ,  $C_{oss} = 350$  pF @  $V_{DS} = 25$  V) MOSFETs for the primary switches and two IR 10CQT150 ( $V_{RRM} = 150$  V,  $V_F = 0.73$  V @  $5$  A<sub>PK</sub>,  $T_j = 125^\circ\text{C}$ ,  $C_T = 200$  pF @  $V_R = 5$  V) Schottky diodes in parallel for the secondary rectifiers. In implementations of the power stages with SRs, the Schottky diodes were replaced with IXYS IXFK100N10 ( $V_{RRM} = 100$  V,  $R_{DS(on)} = 11$  mΩ @  $T_j = 25^\circ\text{C}$ ,  $C_{oss} = 3300$  pF @  $V_{DS} = 25$  V,  $V_{BD} = 1.1$  V) MOSFETs. The turns-ratio of the transformer for the CCM implementation was  $n = 64:10$  ( $L_m = 637$  μH), and the converter was operated in CCM at full-load over the entire input line range with switching frequency  $f_s = 100$  kHz [10]. The transformer used for all other implementations (CF DCM, VF DCM, and ZVS DCM) had a turns ratio of  $n = 38:6$  ( $L_m = 229$  μH).

Figure 7 shows the control and drive circuit for the variable frequency DCM flyback converter implementations with the SR. As can be seen from Fig. 7, the converter has a detector which senses zero crossings of secondary current  $i_{sec}$ . The delay time between the zero crossing of secondary current  $i_{sec}$  and the turn-off of the SR is set by the R-C time constant of the  $T_{delay}^{ZVS}$  circuit which is connected to the output of the zero-crossing detector comparator. Resistors  $R_3$  and  $R_4$  are used to set the hysteresis of the zero-crossing detector. The VF control of the converter is achieved by employing the UC 3852 IC controller. Also, an R-C delay circuit is used on the primary side to set a proper delay between the turn-off of the SR and the turn-on of the primary switch.

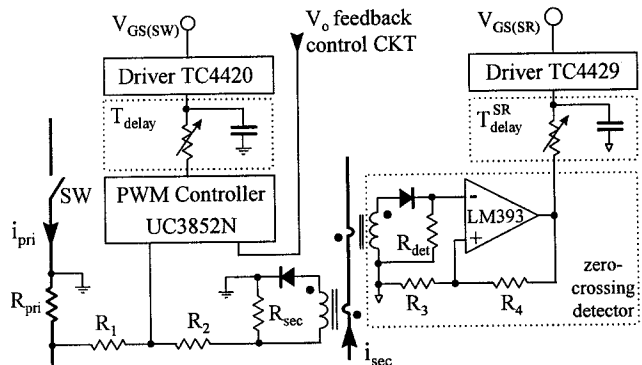


Fig. 7. Control and drive circuit for VF DCM flyback converter with SR. The thick lines belong to the power stage.

### A. CF CCM

Figure 8 shows the measured efficiencies of the CF CCM experimental converters with the Schottky diode and the SR. Because the SR body diode conducts current during delay times,  $T_D^{on}$  and  $T_D^{off}$  in Fig. 2, the rectifier turn-off loss becomes significant at high frequencies. In fact, in the experimental 100 kHz converter, the excessive rectifier turn-off loss in the SR converter exceeds the conduction loss savings. As predicted in Section III, the efficiency of the SR implementation is lower than that of the Schottky implementation, especially at high line, where the reverse-recovery loss given by Eq. (2) is highest.

Figure 9(a) shows the SR turn-off waveforms which are initiated by the primary switch  $SW$  turn-on. The fast-rising voltage  $V_{DS(SR)}$  causes large superimposed capacitor charging and body reverse-recovery currents. To suppress these currents, a saturable core was connected in series with the SR to slow down the rate of  $V_{DS(SR)}$  rise, as shown in Fig. 9(b). As can be seen from Fig. 9(b), with the saturable-core snubber, not only the reverse current amplitude was reduced significantly, but also the rectifier voltage stress was decreased. As a result, the conversion efficiency was improved, as can be seen in Fig. 8. However, this approach cannot completely eliminate the body diode reverse-recovery problem. In fact, output capacitance of the SR,  $C_{oss}^{SR}$ , is significantly higher than the junction capacitance of the two paralleled Schottky diodes  $C_T$  ( $C_{oss}^{SR} = 3300$  pF vs.  $2C_T = 800$  pF), causing a higher capacitor charging loss according to Eq. (3). Therefore, at 36-W power level the CCM converter with the Schottky rectifier exhibits higher efficiency than that with the SR.

### B. CF DCM

Figure 10 shows an oscillogram with key waveform of the CF DCM converter with the SR. During the resonant-interval  $T_{DCM}$ ,  $L_m$ - $C_{eq}$  resonance can be clearly seen in both

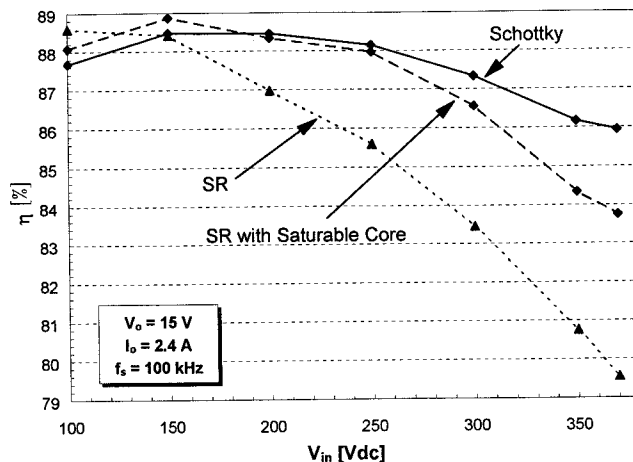


Fig. 8. Measured efficiencies of CF CCM implementation with SR and Schottkies rectifier at full power.

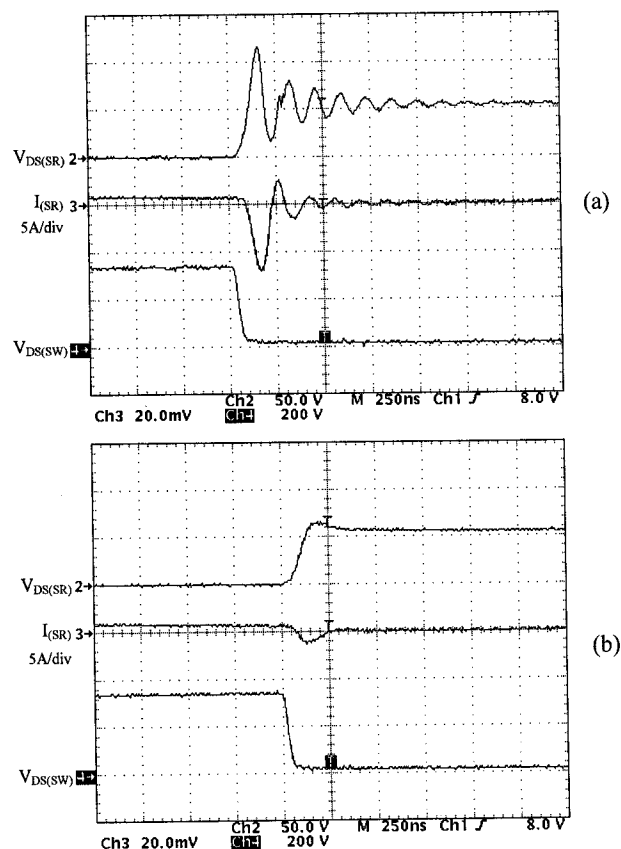


Fig. 9. SR turn-off waveforms of CF CCM converter with SR: (a) w/o saturable core; (b) w/ saturable core.

$I_{(SR)}$  and  $V_{DS(SW)}$  waveforms. The measurement points of the efficiency plot shown in Fig. 11 were collected at the valleys,  $V_{in} - nV_o$ , and the peaks,  $V_{in} + nV_o$ , of  $V_{DS(SW)}$ . As can be seen from Fig. 11, the resonant peak points correspond to the lowest efficiencies, and the resonant valley points

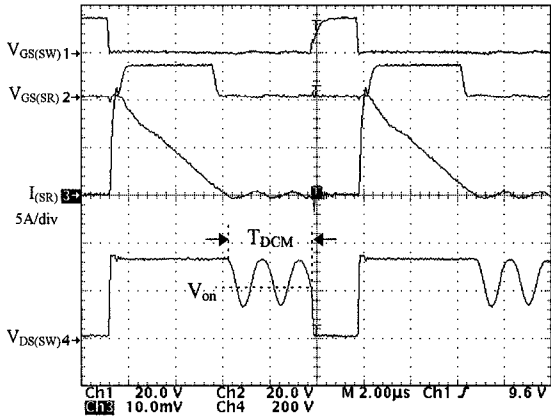


Fig. 10. Measured waveforms of CF DCM converter with SR at  $V_{in} = 250$  Vdc,  $V_o = 15$  V,  $I_o = 2.4$  A.

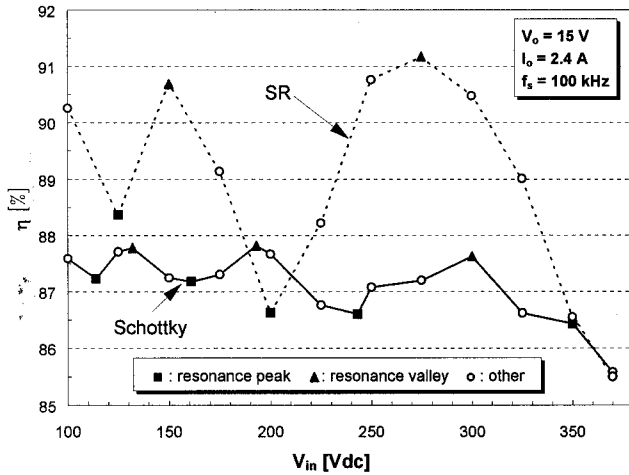


Fig. 11. Measured efficiency of CF DCM implementation with SR and Schottky at full power.

corresponds to the highest efficiencies. The SR and diode rectifier implementations have peaks and valleys at different time instants within a switching period because the resonant period in the SR converter is longer due to a higher  $C_{oss}$  value. Therefore, at certain input voltages, the SR efficiency is lower than that of Schottky and the efficiency improvement is not constant throughout the input range.

### C. VF DCM and ZVS DCM

Figures 12 and 13 show the measured waveforms of the VF DCM and ZVS DCM converters with the SR. As can be seen from Fig. 12, primary switch  $SW$  in the VF DCM implementation is turned on at a voltage lower than  $V_{in}$ . To achieve the switch turn-on with minimum voltage  $V_{DS(SW)}$ , the delay time between the zero-crossing instant of  $i_{sec}$  and the turn-on of the primary switch  $SW$  must be properly designed. Taking the non-linear effect of MOSFET output capacitance

into consideration, the equivalent capacitance of the resonance tank  $L_m-C_{eq}$  is

$$C_{eq} = \frac{3300 p}{(38.6)^2} \cdot \sqrt{\frac{25}{V_{DS}^{SR}}} + 350 p \cdot \sqrt{\frac{25}{V_{DS}^{DR}}} \approx 106 pF. \quad (13)$$

Therefore, according to Eq. (5), the turn-on delay of VF DCM converter with the SR was adjusted to

$$T_{delay} = \pi \sqrt{229 \mu \cdot 106 p} = 0.5 \mu s, \quad (14)$$

as shown in Fig. 12.

By eliminating the parasitic resonance during the  $T_{DCM}$  interval, the efficiency of the VF DCM implementation with the Schottky rectifier is 1% higher than the efficiency of the corresponding CF DCM implementation, as can be seen comparing measurements given in Figs. 11 and 14. Furthermore, the efficiency comparisons in Fig. 14 shows that VF DCM implementation with the SR has a relatively constant 2.5-4% efficiency improvement over VF DCM implementation with the Schottky, as has been predicted. However, in the VF DCM implementation only partial ZVS

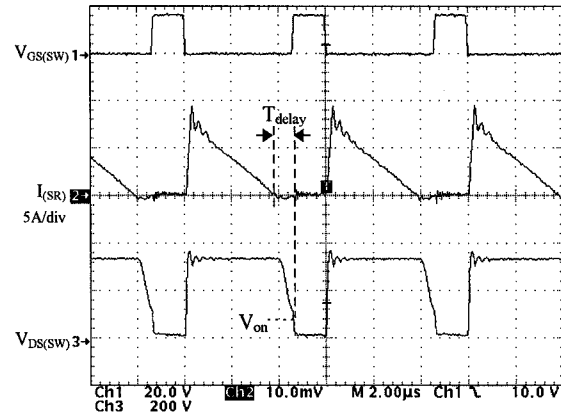


Fig. 12. Measured waveforms of VF DCM implementation with SR at  $V_{in} = 250$  Vdc,  $V_o = 15$  V,  $I_o = 2.4$  A.

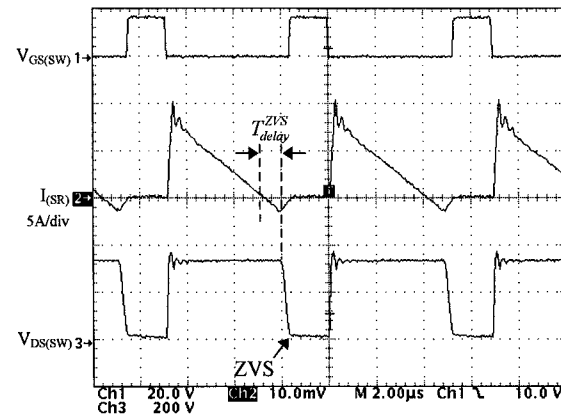


Fig. 13. Measured waveforms of ZVS DCM implementation at  $V_{in} = 250$  Vdc,  $V_o = 15$  V,  $I_o = 2.4$  A.

can be achieved, since in this design, input voltage ( $V_{in} = 100\text{--}370\text{ V}$ ) is larger than the reflected output voltage ( $nV_o = 95\text{ V}$ ), i.e.,  $V_{in} > nV_o$ .

Soft-switching can be obtained for the entire input line range if secondary current  $i_{sec}$  is allowed to flow in the negative direction to the level  $I_{ZVS}$  given in Eq. (7), i.e.,

$$I_{ZVS} = \frac{(38.6) \cdot \sqrt{370^2 - [(38.6) \cdot 15]^2}}{\sqrt{\frac{229\mu}{106p}}} = 1.5\text{ A}. \quad (15)$$

The required delay time for the secondary current to reach  $I_{ZVS}$  is

$$T_{delay}^{ZVS} = \frac{206\mu \cdot 1.5}{(38.6)^2 \cdot 15} = 0.6\mu\text{s}, \quad (16)$$

as shown in Fig. 13.

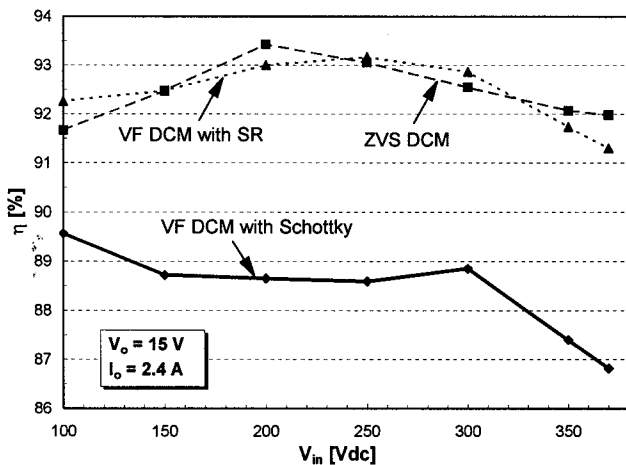


Fig. 14. Measured efficiencies of VF DCM implementations with SR and Schottky, and ZVS-DCM implementation at full power.

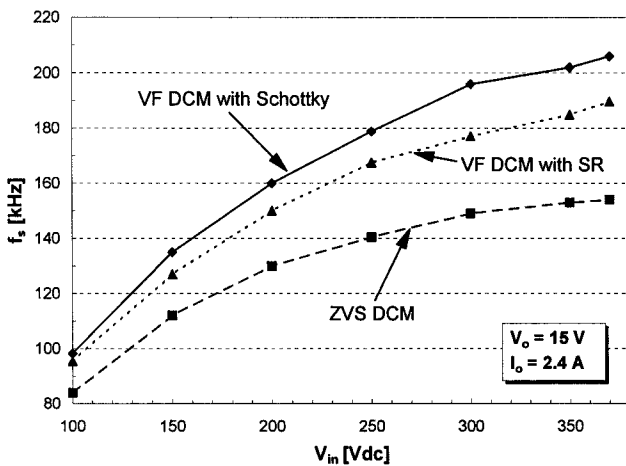


Fig. 15. Switching frequency comparison of VF DCM implementations with SR and Schottky, and ZVS DCM implementation.

The obtained efficiency of the ZVS DCM converter is very close to that of the VF DCM converter with the SR due to the increased conduction loss in the ZVS DCM converter. The switching frequencies of the three VF implementations are shown in Fig. 15. Because of the larger SR output capacitance and additional delay  $T_{delay}^{ZVS}$  required to obtain  $I_{ZVS}$ , VF DCM converter with the Schottky has the highest switching frequency, while ZVS DCM implementation has the lowest switching frequency. Also, the switching frequency range in ZVS DCM implementation is the smallest due to the longest delay time.

## V. Summary

It was shown that the variable-frequency (VF) discontinuous-conduction-mode (DCM) flyback converter implementation is most suitable for synchronous rectification. Moreover, this implementation can be easily designed to work with complete or partial zero-voltage-switching of the primary switch by properly adjusting the delay time between the zero-crossing of the secondary current and the turn-off instant of the synchronous rectifier. In off-line applications, the VF DCM flyback converter with a synchronous rectifier shows a typical efficiency improvement in the 2-4% range compared to the corresponding circuit with a diode rectifier.

## References

- [1] M.W. Smith and K. Owyang, "Improving the efficiency of low output voltage switch-mode converters with synchronous rectification," *Proc. POWERCON 7*, 1980, p. H-4.
- [2] "MOSFETs move in on low voltage rectification," *MOSPOWER Applications Handbook*, Siliconix, 1984, pp. 5-69-6-86.
- [3] J. A. Cobos, J. Sebastian, J. Uceda, E. de la Cruz, and J.M. Gras, "Study of the applicability of self-driven synchronous rectification to resonant topologies," *IEEE Power Electron. Specialists' Conf. Rec.*, 1992, pp. 933-940.
- [4] M.M. Jovanović, M.T. Zhang, and F.C. Lee, "Evaluation of synchronous-rectification efficiency improvement limits in forward converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 4, pp. 387-395, Aug. 1995.
- [5] D.J. Harper, D.R. Hyde, G.M. Fry, and J.A. Houldsworth, "Controlled synchronous rectifier," *High Freq. Power Conversion Conf., Proc.*, 1988, pp. 165-172.
- [6] F.M. Barlage, "Synchronous rectification and regulation in multiple cross regulated outputs," *High Freq. Power Conversion Conf., Proc.*, 1994, pp. 185-193.
- [7] S. Ollero, E. De la Cruz, L. Alvarez, C. Garcia, "New post-regulation and protection methods for multiple output power converters with synchronous rectification," *Proc. IEEE Int. Telecommun. Energy Conf.*, 1996, pp. 462-469.