

# Design and Performance Evaluation of Low-Voltage/High-Current Dc/Dc On-Board Modules

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**Abstract** - The topology selection, design and performance evaluation of an on-board dc/dc converter, which delivers power from a 48-V input to a 1.2-1.65 V/70 A microprocessor load, are presented. It was shown that the symmetrical half-bridge topology with the current doubler and synchronous rectifiers is a suitable approach for this application. The measured full-load efficiency of a 200-kHz experimental half-bridge converter was higher than 82 % in the entire output and input voltage range.

## I. INTRODUCTION

Most of today's high-performance microprocessors operate from voltages between 2 V and 3.3 V and employ power management strategies to minimize the power consumption. Since these microprocessors present very dynamic loads to their power supplies when they transition from the inactive (sleep) mode to the active mode, they require point-of-load regulation to minimize the on-board capacitance required to support the transients [1]. Typically, the current slew-rate of today's microprocessors during a transition between the active and inactive mode, and vice versa, is around 30 A/ $\mu$ s. The present point-of-load dc/dc converters, known as voltage regulator modules (VRMs), use the 5-V output of the existing power supplies to generate the required low voltage. Usually, these VRMs employ the buck topology with synchronous rectifiers (SRs) to attain a high conversion efficiency.

To further increase the processing speed and decrease the power consumption, the operating voltages of the next generation of computer microprocessors will be reduced below 2 V. At the same time, it is expected that these processors will require much more power and will present even more dynamic loads than today's microprocessors. To keep the distribution losses low at an increased power level, the input voltage of the new generation of on-board dc/dc converters has to be increased. In fact, instead of using the 5-V output of existing power supplies, the next generation of the on-board dc/dc converters will be powered either from 12-V or 48-V bus.

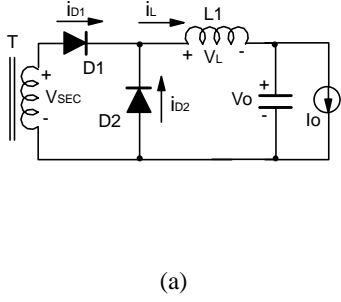
In this paper, design and performance evaluation of the topologies suitable for the next generation of on-board dc/dc modules is presented. The evaluation was performed for the

module which delivers 60-70 A to the 1.2–1.65 V load from the 48 V $\pm$ 10 % bus.

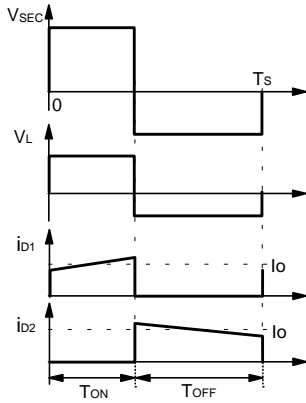
## II. TOPOLOGY SELECTION

Generally, the topology selection for on-board dc/dc converters for the next generation of microprocessors is mainly driven by high-power-density and transient-load-regulation requirements. To achieve a high power density of on-board dc/dc converters placed in a computer box with a limited airflow, the converter efficiency must be maximized. Generally, power conversion with a large step-down ratio, such as from 48 V to below 2 V, can be efficiently performed only in topologies with a step-down transformer. For these isolated, low-output-voltage topologies, the secondary-side power losses are dominant and, consequently, they have the major effect on the conversion efficiency. To maximize the conversion efficiency, it is necessary to reduce the secondary-side losses, primarily, the rectification and transformer-winding loss. The rectification loss can be reduced by replacing Schottky rectifiers with synchronous rectifiers [2]. To minimize the secondary-winding loss, the secondary-winding resistance and rms current should be minimized. The secondary-winding resistance can be reduced by a proper selection of the winding geometry and transformer structure, whereas the secondary-winding rms current can be minimized by employing the current-doubler topology [3]-[5].

To achieve an accurate output regulation during high-slew-rate steps of the microprocessor load with a minimum on-board capacitance, the converter must possess a fast large-signal transient response. For a properly designed wide-bandwidth feedback control, the large-signal transient response is mainly determined by the response of the output filter [1]. The overshoot/undershoot of the output-voltage response can be reduced by decreasing the output-filter inductance value, and by maximizing the voltage on the output-filter inductor during the transients so that the rate of change of the inductor current is maximized. The filter inductance can be reduced by increasing the switching frequency and/or by selecting an appropriate converter topology [6].

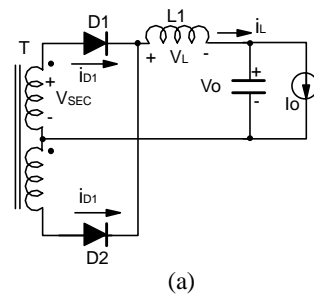


(a)

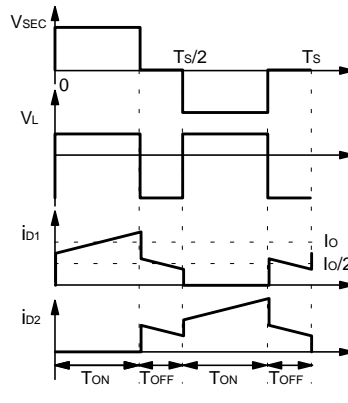


(b)

Fig. 1. Forward secondary-side topology:  
(a) circuit diagram;  
(b) waveforms .

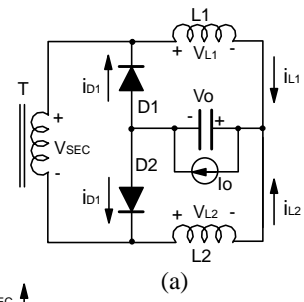


(a)

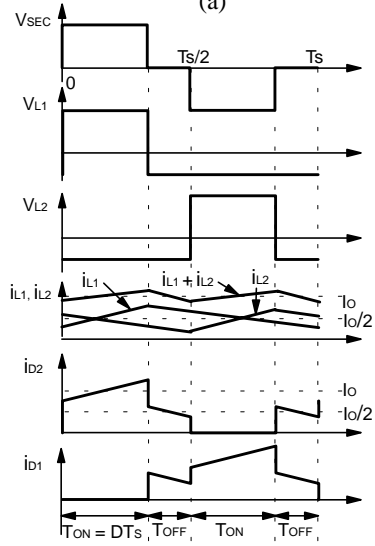


(b)

Fig. 2. Center-tapped secondary-side topology:  
(a) circuit diagram;  
(b) waveforms.



(a)



(b)

Fig. 3. Current-doubler secondary-side topology:  
(a) circuit diagram;  
(b) waveforms .

Figures 1 through 3 show three secondary-side topologies which were evaluated for their suitability for low-voltage/high-current applications. Among the three secondary-side arrangements shown in Figs. 1 through 3, the forward topology shown in Fig. 1(a) has the simplest structure. However, it is the least suitable for low-voltage/high-current applications. Namely, the forward topology requires a larger filter inductance and exhibits larger rectification losses than center-tapped or current-doubler topology, shown in Figs. 2(a) and 3(a). In fact, in the center-tapped topology, the frequency of the output-filter-inductor voltage waveform is twice the switching frequency, while in the forward topology it is equal to the switching frequency. As a result, the required value of the filter inductance in the center-tapped topology is significantly smaller than that in the forward topology.

As can be seen from Fig. 3(b), the frequency of the output-filter-inductor voltage in the current-doubler topology is equal to the switching frequency, i.e., it is the same as in the forward topology. However, in the current-doubler topology, the ripple current of the output filter capacitor is reduced because the ripple currents of the both inductors partially cancel each other, as can be seen from the  $i_{L1} + i_{L2}$  waveform in Fig. 3(b). Due to the ripple cancellation, the required value of the filter inductance is significantly decreased.

Generally, the forward secondary-side topology exhibits a higher conduction loss of the rectifiers than the symmetrically-driven center-tapped or current-doubler topology. Namely, in the forward topology in Fig. 1(a), the inductor current flows through rectifier D1 during on-time  $T_{ON}$  and through D2 during off-time  $T_{OFF}$ , as shown in Fig. 1(b). As a result, the total conduction loss of both rectifiers in the forward topology is equal to the loss of one rectifier carrying the output-filter-inductor current during the entire switching period. However, in the symmetrically-driven center-tapped and current-doubler topology, the load current is evenly distributed between rectifiers D1 and D2 during the off-time, as shown in Figs. 2(b) and 3(b). As a result, the total rectifier conduction loss during the off-time is reduced. For the secondary-side topologies implemented with Schottky diodes this reduction is not very significant because the forward voltage drop of the Schottky diode is not strongly dependent on the current. However, for the implementations with SRs, the loss reduction is tangible. If the center-tapped and current-doubler topologies are driven in such way that they operate without the off-time interval (for example, the asymmetrical half-bridge converter [7]), their rectifier loss is the same as in the forward topology.

For high-current applications the current-doubler topology is preferred to the center-tapped topology for a number of

reasons. First, in the current-doubler topology the inductor currents and the transformer secondary current are two times lower than the corresponding currents in the center-tapped topology. As a result, the current-doubler topology exhibits lower conduction losses than the center-tapped topology. Second, the current-doubler scheme minimizes the number of high-current interconnections that simplifies the secondary layout and further reduces the layout-related loss. Finally, the transformer and the filter inductors in the current-doubler topology can be integrated on a single magnetic core, which simplifies the packaging of the components and may reduce the overall size of the magnetics [8].

The secondary-side current-doubler topology in Fig. 3(a) can be combined with nearly all primary-side topologies such as the forward, half-bridge, push-pull, and the full-bridge topology. Because the forward primary-side topology is not symmetrical, it is not suitable for low-voltage / high-current applications. Specifically, the forward converter with the current doubler transfers the source energy to the secondary side in the forward fashion during the on-time of the primary switch, and in the flyback fashion during the off-time of the primary switch [5]. Since there is no off-time interval, the rectification loss is not minimized. Furthermore, since the transformer serves as the energy source during the off-time of the primary switch, its primary magnetizing current is as high as a half of the load current reflected to the primary. As a result, the primary switch suffers from an excessive current stress and loss.

The push-pull, symmetrical half-bridge, and full-bridge primary-side topologies are well-suited for the low-voltage / high-current applications with the current-doubler secondary. Since the push-pull topology has two times less primary current stress and twice the voltage stress of the primary switches than the half-bridge topology, the push-pull topology is more suited for the low-voltage / high-current on-board converters operating from 12 V than from 48 V. Among considered topologies, the bridge topology seems to be the best choice for the on-board converter with the 48-V input. Although the full-bridge topology offers both the low current stress of the push-pull topology and the low voltage stress of the half-bridge topology, the half-bridge topology is a preferred choice because of the lower component count and overall simplicity. However, it should be noted that the full-bridge topology might be the best choice at high frequencies where soft-switching of the primary switches is required to maintain high efficiency. Namely, by employing the phase-shift control, the full-bridge topology can be implemented with zero-voltage-switching of the primary switches.

### III. DESIGN AND EVALUATION OF SYMMETRICAL HALF-BRIDGE CONVERTER

The circuit diagram and key waveforms of the symmetrical half-bridge (SHB) converter with a current doubler are shown in Figs. 4 and 5, respectively. Since the performance of the circuit in Fig. 4 is mainly determined by the characteristics of the SRs and their driving scheme, as well as by the design of the isolation transformer, the rectifier selection, SR driving techniques, and transformer design are discussed in detail.

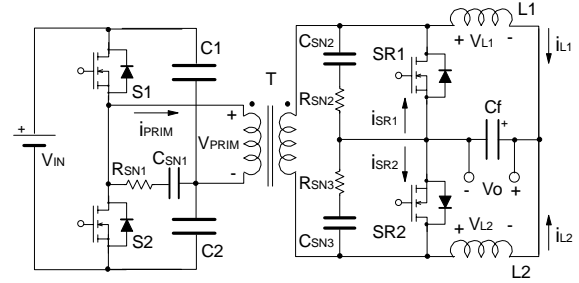


Fig. 4. Circuit diagram of the symmetrical half-bridge converter with the current-doubler rectifier.

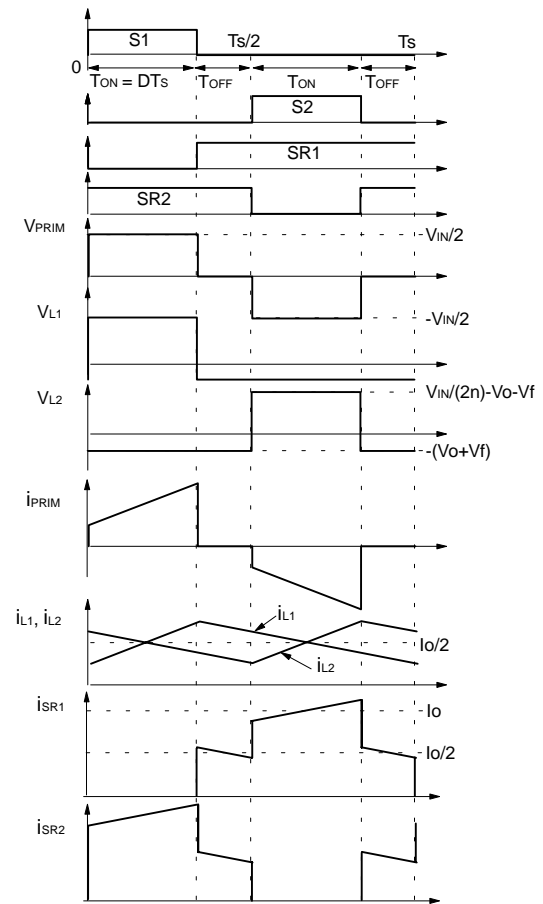


Fig. 5. Idealized waveforms of the symmetrical half-bridge converter.

### A. Rectifier Selection

Although the forward voltage drop of today's state-of-the-art low-voltage Schottky diodes and MOSFET SRs are comparable at 70 A, and although the circuit implementation with the Schottky rectifiers is much simpler, the MOSFET SRs offer superior efficiency when used in parallel. To compare the performance of paralleled Schottky rectifiers and MOSFET SRs, Fig. 6(a) shows the i-v characteristics of the 85CNQ015 Schottky diode and the MTP75N03HDL MOSFET. As can be seen from Fig. 6(a), at 70 A the voltage drop across a single SR is higher than the voltage drop across a single Schottky diode. However, when two SRs are connected in parallel so that each SR carries 35 A, their voltage drop is lower than the voltage drop of two paralleled Schottky diodes. Namely, because of an exponential i-v characteristic, the reduction of the voltage drop of two Schottky diodes in parallel is only 22 % compared to the drop of the single device, whereas, because of a linear i-v characteristic, the reduction of the voltage drop of two SRs in parallel is 50 %. This difference becomes even more pronounced when three or more devices are paralleled. Figure 6(b) shows the comparison of the estimated rectification loss at 70 A for the Schottky rectifiers and SRs as a function of the number of paralleled devices. The loss estimate presented in Fig. 6(b) is obtained for the current-doubler topology, shown in Fig. 3(a), assuming that both rectifiers operate with the 50 % duty cycle. The Schottky rectifier loss includes both the conduction loss of the forward-biased rectifier and the leakage-current loss of the reversed-biased rectifier. To calculate the leakage-current loss, the reverse voltage of 6 V was assumed. The calculated rectification loss of the SRs includes the conduction, switching, and driving loss. In these calculations it was assumed that the current distribution among the paralleled devices is even, and that the device temperature does not depend on the number of devices paralleled. In addition, a switching frequency of 200 kHz was assumed in the switching-loss calculations.

Finally, due to the MOSFET's negative temperature coefficient, paralleled MOSFET devices tend to naturally keep a uniform current distribution among the individual devices. However, since the Schottky rectifiers have a positive temperature coefficient, the paralleling of Schottky diodes requires much more design effort to assure an even current sharing among the paralleled devices.

### B. Driving of Synchronous Rectifiers

In general, SR's drive can be implemented with a self-driven, hybrid-driven, or control-driven scheme. In a self-driven SR implementation, the SRs are driven directly by voltages on the windings of the power transformer. Since the gates of the self-driven SRs are charged and discharged in a resonant fashion, the driving loss is very much reduced. As a result, the self-driven SR approach is very attractive for its low driving loss, simplicity, and low cost. Unfortunately, the

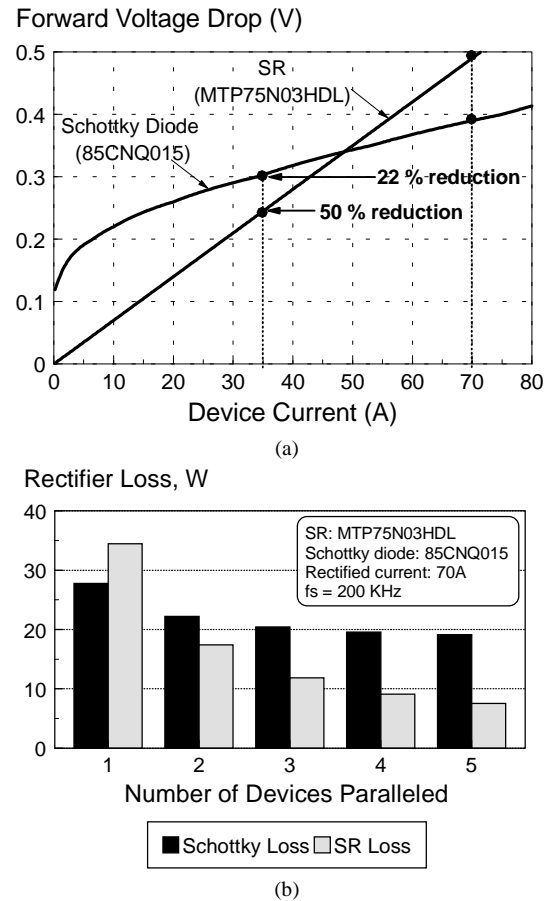


Fig. 6. Comparison between paralleled Schottky and Synchronous rectifiers. (a) Forward voltage drop. (b) Loss.

self-driven SRs cannot be implemented in the SHB converter. Namely, as can be seen in Fig. 5, the voltage on the transformer winding in the SHB converter is zero during intervals  $T_{OFF}$  when both SRs should conduct. Therefore, during the  $T_{OFF}$  intervals the SR current would flow through the body diodes of the SRs, instead of flowing through the channels of the SRs. As a result, the conduction and reverse-recovery loss of the self-driven SRs in the SHB topology would be high.

The described deficiency of the self-driven SRs can be overcome by employing control-driven SRs which derive the gate-drive signals from those of the primary switches. However, the control-driven SR implementation is complex, less efficient, and more expensive.

The complexity of the control-driven SR drive can be reduced by resorting to the hybrid-type SR drive. In a hybrid-driven SR implementation, the SRs are turned on by a transformer winding voltage and turned off by a control signal. Figure 7 shows a hybrid SR drive for the SHB converter. In Fig. 7, the gate-source capacitances of the SRs are charged by the voltages on two additional windings  $N_{SR1}$ ,  $N_{SR2}$  of the power transformer and discharged by auxiliary switches SA1 and SA2. The gate signals for SA1 and SA2 switches are easy to derive because they coincide with the gate signals of primary switches

S1 and S2. The power needed to drive the auxiliary switches is minimal.

The hybrid driving scheme in Fig. 7 relies on the energy stored in the leakage inductance of the transformer to turn on the SR during off-time  $T_{OFF}$ . To facilitate the explanation of the SR gate charging mechanism, Figures 8(a) and 8(b) show the equivalent circuit and waveforms of the SHB converter with the emphasis on the resonant transition after the primary switch turn-off. In Fig. 8(a), the voltage sources on the primary side and the current sources on the secondary side represent half-bridge capacitors and output-filter inductors, respectively. Inductors  $L_{S1}$ - $L_{S4}$  and capacitors  $C_{iss}(SR1)$ ,  $C_{iss}(SR2)$ ,  $C_{oss}(S1)$ , and  $C_{oss}(S2)$  represent leakage inductances of the transformer windings, input capacitances of SR1 and SR2, and output capacitances of primary switches S1 and S2, respectively.

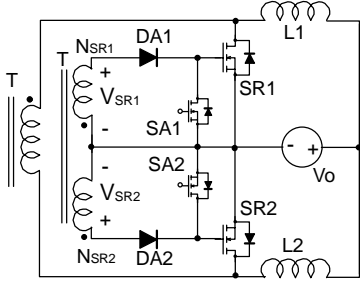


Fig. 7. Driving SRs from power transformer windings.

It should be noted that when switch S1 is conducting, SR1 is off and SR2 is on. After S1 is turned off  $t = T_0$ , it is necessary to turn on SR1 while still keeping SR2 on. Otherwise, if SR1 was not turned on after the turn-off of S1, the body diode of SR2 would conduct, thus, increasing the conduction loss. To turn on SR1, it is necessary to induce positive voltage  $V_{SR1}$  across driving winding  $N_{SR1}$ . This positive voltage can be generated only if the voltage across the primary winding,  $V_{PRIM}$  becomes negative immediately after S1 is turned off.

As shown in Fig. 8(b), during interval  $[T_0-T_1]$ , output capacitance  $C_{oss}(S2)$  of primary switch S2 is discharged by reflected output-inductor current  $I_O/(2 \cdot n)$ , where  $n = N_p/N_s$ , and the voltage across switch S2,  $V_{DS(S2)}$  decreases linearly. When  $V_{DS(S2)}$  reaches  $V_{IN}/2$  level at  $t = T_1$ , the body diode of SR1 starts conducting. Since after  $t = T_1$  both SR2 and the body diode of SR1 are conducting, the secondary of the power transformer is shorted, i.e.,  $V_{SEC} = 0$ . As a result, after  $t = T_1$ , transformer leakage inductances  $L_{S1}$  and  $L_{S2}$  start to resonate with output capacitances  $C_{oss}(S1)$  and  $C_{oss}(S2)$  of primary switches S1 and S2. As shown in Fig. 8(b), this resonance continues to discharge  $C_{oss}(S2)$  below  $V_{IN}/2$  level so that voltage  $V_{DS(S2)}$  continues to decrease towards zero. If enough energy is stored in leakage inductances  $L_{S1}$  and  $L_{S2}$ ,  $V_{DS(S2)}$  will reach zero, as illustrated in Fig. 8(b). After  $V_{DS(S2)}$  reaches zero at  $t = T_2$ , it stays clamped to zero until the leakage inductance is completely discharged at  $t = T_3$ , i.e., until primary current  $i_{PRIM}$  falls to zero. After  $i_{PRIM}$  becomes zero at  $t = T_3$ ,  $V_{DS(S2)}$  starts resonating back towards its steady-state value of  $V_{IN}/2$ . In the circuit in Fig. 8(a) this resonance is damped by the  $R_{SN}-C_{SN}$  snubber placed across the

transformer primary winding so that after  $V_{DS(S2)}$  reaches  $V_{IN}/2$  at  $t = T_4$ , it stays at the  $V_{IN}/2$  level until switch S2 is turned on at a later moment.

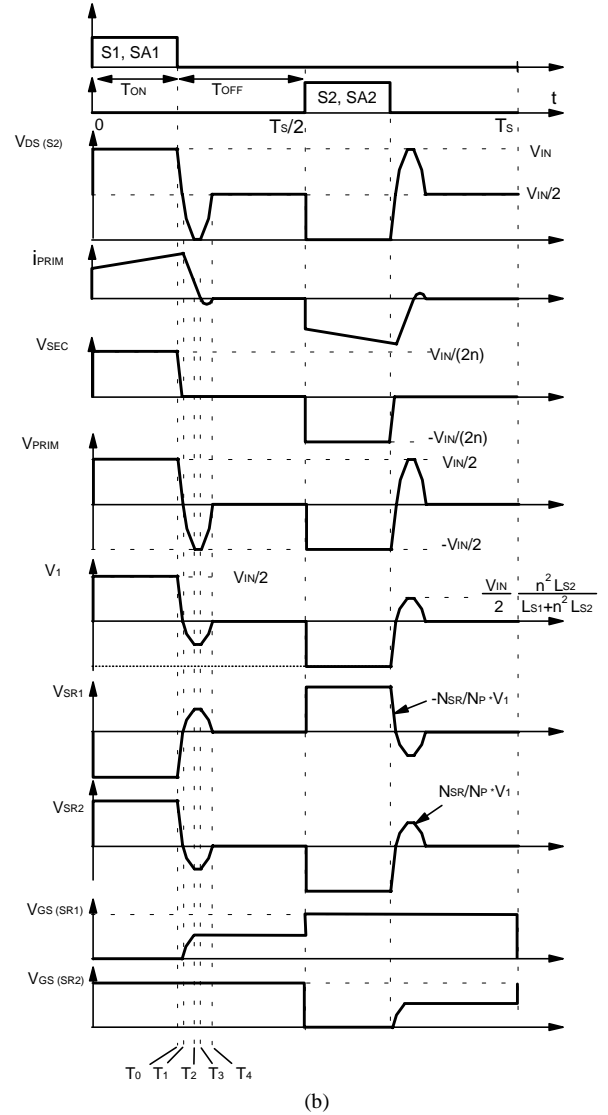
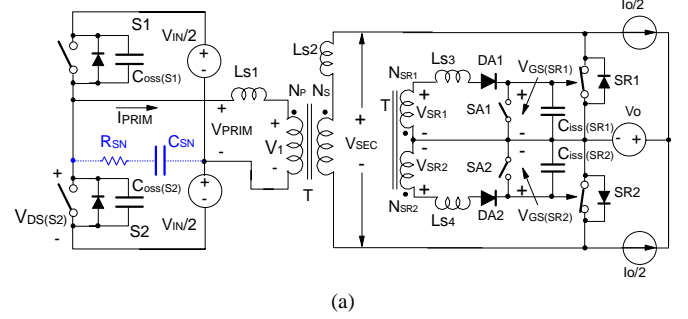


Fig. 8. Equivalent circuit and waveforms of the resonant charging of SRs' gates during off-time.

As can be seen in Fig. 8(a), when the secondary winding is shorted by the simultaneous conduction of SR1 and SR2 during interval  $[T_1-T_4]$ , primary voltage  $V_{PRIM}$  is divided between the voltage drop across primary leakage inductance  $L_{S1}$  and the voltage drop across reflected secondary leakage inductance  $L_{S2} \cdot n^2$ . As a result, the peak value of voltage  $V_I$  across the reflected leakage inductance  $L_{S2}$  is given by  $V_{I\text{PEAK}} = [n^2 \cdot L_{S2} / (L_{S1} + n^2 \cdot L_{S2})] \cdot V_{IN} / 2$ . The voltages of SR driving windings  $N_{SR1}$  and  $N_{SR2}$  are proportional to  $V_I$ :  $V_{SR2} = -V_{SR1} = (N_{SR1} / N_P) \cdot V_I = (N_{SR2} / N_P) \cdot V_I$ , as indicated in Fig. 8(b).

As can be seen from Fig. 8(b), the negative resonant voltage observed in the primary voltage waveform during interval  $[T_1-T_4]$  induces a positive driving voltage  $V_{SR1}$  that charges the gate of SR1. When the gate voltage  $V_{GS(SR1)}$  exceeds the gate-to-source threshold voltage, the current which was flowing through the body diode of SR1 starts flowing through the channel of the SR1 MOSFET. Once the SR1 gate is charged, it stays charged until auxiliary switch SA1 is turned on  $t = T_S$  because diode DA1 prevents the discharge of the SR1 gate.

Since the magnitude to which the SR1 and SR2 gates are charged during their respective off-time resonance depends on the voltage on driving windings  $N_{SR1}$  and  $N_{SR2}$ , the value of leakage inductance  $L_{S2}$  determines the performance of the drive. If  $L_{S2}$  is not large enough so that voltages  $V_{SR1}$  and  $V_{SR2}$  are not sufficient to turn on the respective SRs, an external inductance must be added in series with the secondary winding to provide the necessary secondary-side inductance required for proper operation. However, since the energy stored in the added inductance must be dissipated, the value of the added inductance should be minimized. Otherwise, the loss reduction gained by the optimization of the driving-voltage level of the SRs may be diminished by the loss of the additional-inductor energy. It should be noted that because the additional inductance is typically small, the added inductor can be implemented with ferrite bead(s). Finally, the proper design of the SR drive requires the duration of the resonant interval  $[T_2-T_3]$  to be longer than the time of a resonant charging of the gate-source capacitance of SR1 and SR2, i.e., longer than one-quarter of the resonant period of the gate-drive circuit.

The dependence of the SR drive on the leakage inductance  $L_{S2}$  can be removed by resorting to the hybrid-drive implementations shown in Figs. 9(a) and 9(b). In Fig. 9(a), the drive voltages for the SRs are derived from the windings of small driving transformer TA, instead from the windings of the power transformer. Since the output of transformer TA is not shorted during resonant interval  $[T_1-T_4]$ , its secondary voltage waveform follows the primary voltage. In addition, because TA has much larger number of primary turns than power transformer T, the SR driving voltage level can be chosen with a much higher resolution when TA is used for driving SRs instead of T.

In the hybrid-drive implementation in Fig. 9(b), the SR driving voltages are obtained from additional windings  $N_{SR1}$  and  $N_{SR2}$  of output-filter inductors L1 and L2, respectively. This approach exploits the fact that the timing of the voltage waveforms of the output inductors, shown in Fig. 5, coincides with the timing required for the proper operation of the SRs.

This driving scheme requires two extra switches SA3 and SA4, since the SR should be disconnected from the driving winding prior to the gate discharge. To minimize the cross-conduction of the resulting totem-pole driver at high switching frequencies, it is recommended to use complimentary low-power MOSFET transistors for implementation of switches SA1-SA4.

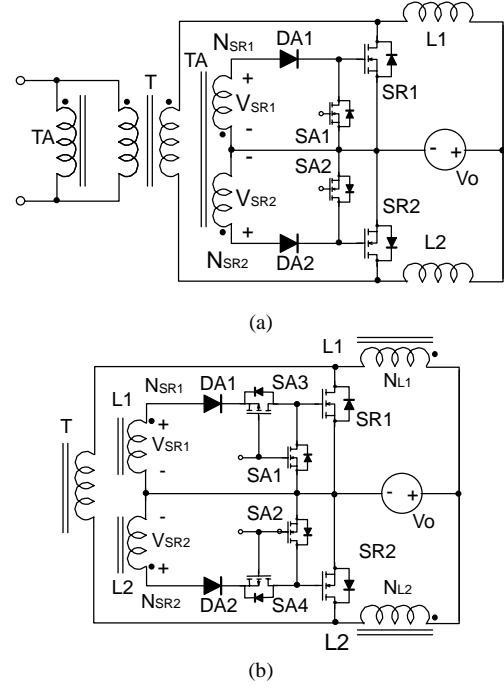


Fig. 9. Alternative SR driving schemes: (a) driving from auxiliary transformer windings; (b) driving from windings of output inductors.

For all three hybrid SR drives, the selection of the number of turns of the driving windings is constrained by the required range of the gate-source voltage. The SR gate-source voltage should be high enough to attain the lowest possible value of the drain-source "on" resistance (typically 10-12 V), while it should be below the maximum allowable driving voltage (typically 15-20 V). For the SRs driven from the power transformer as in Fig. 7, driving voltage magnitude  $V_{SR}$  is proportional to the input voltage  $V_{IN}$ , and varies within the same 10% limit as the input voltage. The number of turns of the driving winding is determined from  $N_{SR} = 2 \cdot N_P \cdot V_{SR} / V_{IN}$ .

For the SRs driven by the windings of output inductors as in Fig. 9(b), the driving voltages  $V_{SR1}$ ,  $V_{SR2}$  are proportional to the sum of the output voltage  $V_O$  and forward voltage drop  $V_F$  of the SR. Assuming that  $V_F = 0.2$  V, the variation of the SR driving voltage is 1.32:1 in the entire output-voltage range. Therefore, the  $V_{SR}$  value can be easily selected in the 9.8-13 V range which provides the minimum SR "on" resistance, as well as the compliance with the SR gate-source voltage rating. The number of turns of the driving winding can be calculated as

$N_{SR} = N_L \cdot V_{SR} / (V_O + V_F)$ , where  $N_L$  is the number of turns of the output-filter inductor.

### C. Transformer Design

Due to the topology symmetry and blocking action of capacitors C1 and C2, the transformer of the SHB converter in Fig. 4 carries no dc magnetizing current and, consequently, its core does not require to be gapped. As a result, the transformer in the SHB converter can be designed with a low ac magnetizing current. To minimize the secondary-winding conduction loss and to simplify the manufacturing of the transformer, the single-turn secondary winding should be selected. Also, to minimize the leakage inductance, the primary and the secondary winding should be interleaved. Finally, to simultaneously provide high-current capability and tight coupling, a copper foil should be used for both primary and secondary windings. For the  $48 \text{ V} \pm 10 \%$  input and the maximum output voltage of 1.65 V, the transformer requires the 4:1 turns ratio.

In the SHB converter in Fig. 4 implemented with the hybrid drive shown in Fig. 7, the resonance between the drain-to-source capacitances of the primary MOSFETs and the leakage inductance of the transformer is utilized to turn on the appropriate SR immediately after a primary switch turn-off. However, this resonance continues after the leakage inductance is completely discharged, thus, producing undesirable ringing of the primary voltage waveform during the remainder of the off-time. To eliminate this undesirable ringing, the circuit in Fig. 4 employs the  $R_{SN1}-C_{SN1}$  snubber placed across the primary winding of the transformer. In addition, after the turn-on of the primary switches, the transformer leakage inductance resonates with the drain-source capacitance of the SR which is being turned off. This parasitic secondary-side resonance is damped by the  $R_{SN2}-C_{SN2}$ ,  $R_{SN3}-C_{SN3}$  snubbers connected across the drain and source terminals of the SRs.

Generally, the switching frequency of the SHB converter in Fig. 4 is limited by the snubber losses. It was found that for the application described in this paper the switching frequency of around 200 kHz results in an optimal trade-off between the size of the energy-storage components and the converter efficiency.

### D. Experimental Results

The performance of the SHB converter with the SRs and the current-doubler secondary in Fig. 4 was evaluated experimentally. The converter prototype was constructed using the following components.

- S1, S2 - HUF75639P (100-V, 28-m $\Omega$  MOSFET).
- SR1, SR2 - 3 x MTP75N03HDL (30-V, 7.5-m $\Omega$  MOSFET).
- L1=L2=2.2  $\mu$ F - A-310090-2 Arnold MPP core, 4 turns of 7 strands of AWG 19 solid wire.

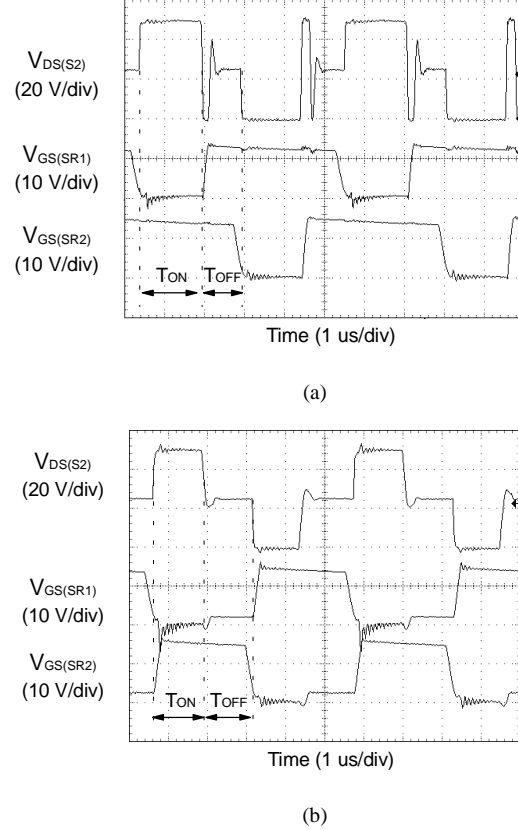


Fig. 10 Experimental waveforms of the switch S2 drain-source voltage  $V_{DS(S2)}$ , SR1 and SR2 gate-source voltages  $V_{GS(SR1)}$ ,  $V_{GS(SR2)}$ : (a)  $V_{in} = 48 \text{ V}$ ,  $V_o = 1.45 \text{ V}$ ,  $I_o = 72 \text{ A}$ ; (b)  $V_{in} = 48 \text{ V}$ ,  $V_o = 1.45 \text{ V}$ ,  $I_o = 2.5 \text{ A}$ .

- T - EFD-30-3F3 Philips core; primary: 4 turns of 3-mil foil; secondary: 1 turn of 12-mil foil; driving windings: 2 turns of 2-mil foil; magnetizing inductance measured on the primary side  $L_M = 30 \mu\text{H}$ ; leakage inductance measured on the primary side  $L_S = 100 \text{ nH}$ .
- $C_B$  - 3 x 4.7- $\mu\text{F}$ , 63-V ceramic capacitors.
- $C_F$  - 3 x 820- $\mu\text{F}$ , 4-V OSCON capacitors.

Figures 10(a) and 10(b) show the experimental waveforms of the SHB converter with SRs driven from the power transformer windings at the load current of 70 A and 2.5 A, respectively. As it can be seen in Fig. 10(a), at full load the resonance between the leakage inductance and the output capacitance of the primary switches during the off-time is strong enough to turn on the appropriate SR. As a result, during the off-time both SRs conduct the current. It is important to note that at full-load operation the SRs' body diodes do not conduct and, consequently, there is no loss associated with their reverse recovery. However, at light load, as shown in Fig. 10(b), the energy stored in the leakage inductance is low, and the resonance is not sufficient to turn-on the corresponding SR. Therefore, during the off-time the corresponding inductor current flows through the body diode of this SR. As a result, the reverse-recovery loss of the SR body diode reduces converter efficiency at light load. This reverse-recovery loss can be

significantly reduced by driving SRs from windings of the output inductors, as shown in Fig. 9(b), or by adding Schottky diodes in parallel with SRs.

The full-load measured efficiency of the experimental SHB converter at  $V_o=1.2$  V, 1.45 V, and 1.65 V is shown in Fig. 11. In the entire voltage range the measured full-load efficiency was above 82 %. Employment of a better packaging technique can minimize the interconnect resistances and inductances on the secondary side and can further increase the efficiency by 2-3 %. Finally, Figure 12 shows the measured efficiency and power loss as a function of the load. As can be seen in Fig. 12, the efficiency reaches maximum in the 35-48 A load-current range. At higher loads, the efficiency decreases because the SR conduction loss increases rapidly with the current increase. In the 0-25 A range, the converter loss increases as the load decreases. This happens because the leakage energy is not sufficient to turn on the appropriate SR during the off-time, and the reverse-recovery loss of the SRs' body diodes increases.

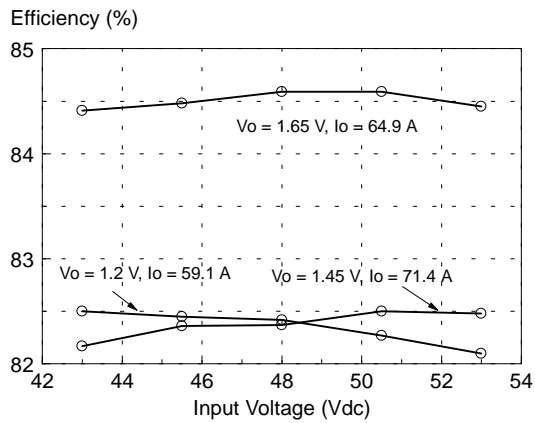


Fig. 11. Measured efficiency of the symmetrical half-bridge converter as a function of input voltage.

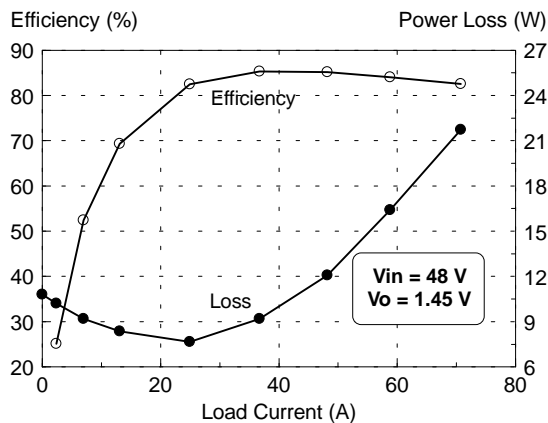


Fig. 12. Measured efficiency and power loss of the symmetrical half-bridge converter as a function of load.

#### IV. SUMMARY

The topology selection, design guidelines, and performance evaluation of low-voltage/high-current dc/dc on-board modules operating from a  $48\text{-V} \pm 10\%$  input were presented. The symmetrical half-bridge converter with the current doubler and synchronous rectifiers was found to be a suitable topology for the implementation of the next generation of on-board dc/dc converters for computer applications. The measured full-load efficiency of the experimental 1.2-1.65 V/60-70 A symmetrical half-bridge converter was higher than 82% in the entire input-voltage and output-voltage range.

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