Performance Evaluation of 70-W Two-Stage Adapters for Notebook Computers

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***Abstract* - The paper presents design and performance evaluation of two-stage ac adapters for notebook computers which deliver 70 W from the universal line. Three versions of the flyback converter, as well as the PWM and resonant half-bridge converter were evaluated and compared with respect to their efficiency, component stress, output filter size, and complexity.**

I. INTRODUCTION

With ever increasing power consumption of notebook computers, the power-density increase of their ac adapters is a major design challenge. While adapters with 3-4 W/in^3 power density were prevalent a couple of years ago, today's adapters have power densities in excess of 6 W/in^3. To achieve the power density above 6 W/in^3, the adapters need to have a minimum efficiency in the 85-87 % range. This high efficiency is required, because for safety reasons external adapters are packaged in completely sealed enclosures and, consequently, the heat from the adapters is removed only by the natural convection.

Generally, for power levels below approximately 50 W, the flyback converter preceded by a diode rectifier with a capacitive filter, shown in Fig. 1(a), has been proven to be the most cost-effective solution [1, 2]. The main disadvantage of the circuit in Fig. 1(a) is a wide variation of the voltage across the energy-storage capacitor C_B. As the result, the energy-storage capacitor contributes significantly to the adapter size and cost. In addition, the wide input-voltage range of the universal-line adapters has a detrimental effect on efficiency. The disadvantages of the single-stage approach can be alleviated by resorting to the two-stage approach, shown in Fig. 1(b). In Fig. 1(b), the boost front-end stage maintains a relatively constant voltage on the energy-storage capacitor, making possible to use a lower value and a smaller size energy-storage capacitor, as well as to improve the conversion efficiency of the dc-dc stage. In addition, the boost front-end stage is able to provide a power factor correction. Therefore, the two-stage approach is a natural choice for adapters with an input power exceeding 75 W that are required to meet IEC 1000-3-2 standard specifications.

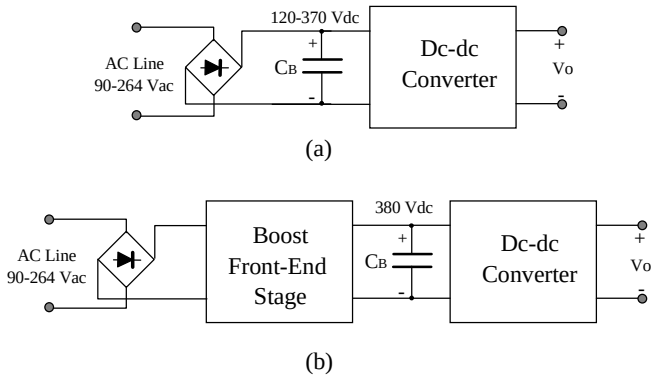

Fig. 1 Adapter approaches: (a) single-stage, (b) two-stage.

At the 70-W power level, the boost converter operating in the critical conduction mode seems to be the most appropriate choice for the front-end stage. This boost circuit has a lower current stress and requires a smaller input filter than the boost converter operating in the discontinuous conduction mode (DCM). At the same time, its performance does not suffer from the diode reverse-recovery problems which exist in the boost converter operating in the continuous conduction mode (CCM). The critical-mode boost converter operates with a variable-frequency control, which can be easily implemented by several inexpensive 8-pin IC controllers available on the market. The worst-case efficiency (at low line) of a 75-W critical-mode front-end stage is 93-94 % typically. Therefore, to have an 85-87 % efficient adapter, the efficiency of the dc-dc stage should be in the 91-93 % range.

The objective of this paper is to develop, evaluate, and compare dc-dc converter topologies for the 70-W two-stage adapter**.** Several implementations of the flyback topology and half-bridge (HB) topology were considered. Specifically, the constant-frequency PWM flyback converter, the variable-frequency (VF) flyback converter, the VF flyback converter with a synchronous rectifier (SR), asymmetrical HB converter, and resonant HB converter were evaluated. The comparative evaluation was performed with respect to the conversion efficiency, component stress, output-filter size, and complexity.

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II. EVALUATION OF FLYBACK IMPLEMENTATIONS

The topology evaluations were performed for the 70-W adapter with the following specifications:

- line voltage 90-264 Vac;
- output voltage 19 Vdc;
- output current 0-3.7 A;
- output voltage ripple 300 mVpp.

A. PWM Flyback Converter

PWM flyback converter, shown in Fig. 2 along with its simplified control diagram, is the prevalent converter topology for adapters below 50 W. It features a low component count and a simple constant-frequency control. Adapter experimental waveforms are presented in Fig. 3. As can be seen from Fig. 3, the circuit operates in the CCM at full load which is preferable from the efficiency point of view since in the CCM component current stresses are lower than in the DCM.

Details of the flyback converter design and optimization can be found in [1]. The main trade-off in the power stage design is the selection of the transformer turns ratio N. Namely, as the turns ratio is increased, the primary-side conduction losses become lower, but the voltage stress $V_{IN}+N\cdot V_O$ and, therefore, the switching loss of the MOSFET also increase. To optimize the conversion efficiency and minimize the cost, it is recommended to choose the maximum turns ratio which allows the use of a 600-V device, which has lower on-resistance and is more cost-effective compared to higher rated devices. Selection of a 600-V MOSFET corresponds to the turns ratio between 5:1 and 6:1. The calculated losses of the semiconductor devices of the PWM flyback converter are shown in Fig. 4. Loss calculations were based on the same assumptions and expressions that were used in [2], except for the computation of the rectifier loss. In this paper, the actual i-v characteristic of the Schottky diode was employed to compute the forward voltage drop as a function of the diode current. The rectifier loss was then computed by numerical integration of the instantaneous diode voltage and current. It was also assumed that two paralleled diodes of the 10CTQ150 package share the current evenly. As can be seen from Fig. 4, the MOSFET in the PWM flyback converter exhibits a significant switching loss. This loss can be reduced by soft switching.

B. Variable-Frequency Soft-Switched Flyback Converter with Schottky Rectifier

The soft switching in the flyback converter can be achieved by operating the converter in the critical conduction mode, *i.e.*, at the CCM/DCM boundary. The operation at the CCM/DCM boundary requires a variable-frequency control.

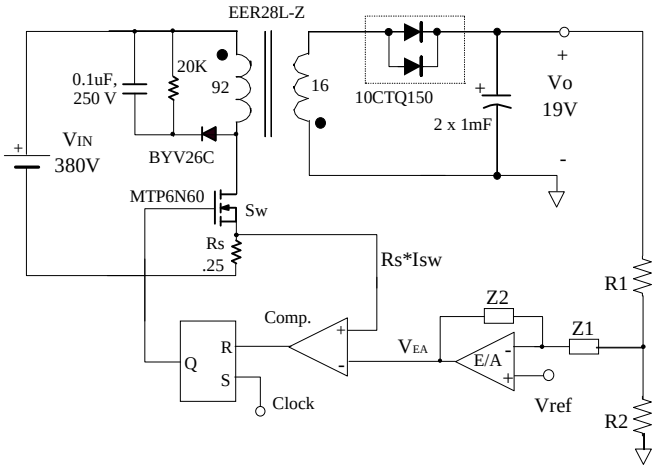

Fig. 2 Flyback PWM converter.

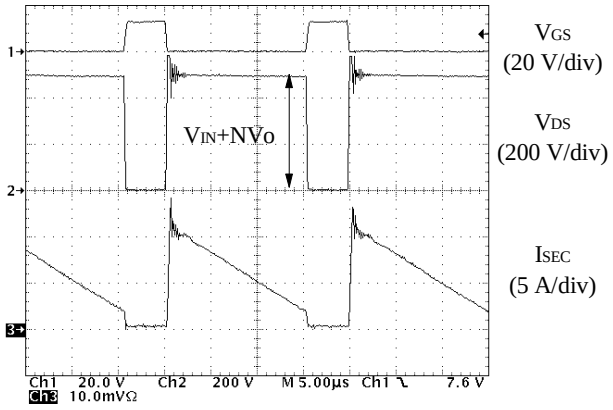

Fig. 3 Experimental waveforms of the PWM flyback converter at full load. V_{GS} - gate-source switch voltage; V_{DS} - drain-source switch voltage; I_{SEC} - transformer secondary current.

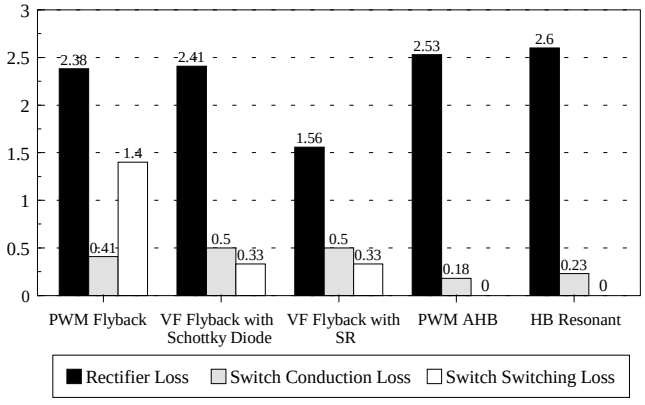

Fig. 4 Calculated device loss breakdown for evaluated converters.

A simplified circuit diagram of the VF flyback converter with Schottky rectifier is given in Fig. 5. The turn-on and turn-off instants of the primary switch are governed by the RS-latch. The switch is turned off when its current exceeds the reference level set by the voltage feedback loop. During the switch off-time, the transformer secondary current linearly decays to zero. The zero crossing of the secondary current is sensed indirectly by detecting the voltage across transformer winding V_{sense}. After the secondary current reaches zero, the transformer magnetizing inductance resonates with the parasitic capacitances of the primary switch and secondary rectifier. Due to the resonance, the voltage across the sensing winding changes its polarity, which is detected by Comparator B in Fig. 5. After delay T_D, the RS-latch is set by the output signal of the CCM/DCM boundary detector. Delay T_D is necessary for the switch voltage to reach the resonance valley and it is ideally equal to the one-fourth of the resonant period. As a result, the voltage across the switch at the turn-on instant in the VF converter is V_{IN}-N·V_O, instead of V_{IN}+N·V_O in the constant-frequency converter.

As can be seen in Fig. 4, the switch conduction loss of the VF converter is slightly higher than that of the PWM converter due to operation at the CCM/DCM boundary, but the switching loss is dramatically decreased.

The converter switching frequency depends on the load, and increases as the load decreases. The minimum switching frequency, which occurs at the full load, was chosen to be 35 kHz. With the load changing from zero to 100 %, the switching frequency varies in the 35-92 kHz range.

Since in the critical conduction mode the switch current starts from zero each switching cycle and its slope is determined by the input voltage, a direct current sensing is not necessary. The switch current waveform can be emulated by generating the ramp with a slope proportional to the input voltage [3].

C. Variable-Frequency Soft-Switched Flyback Converter with Synchronous Rectifier

To further improve the efficiency of the VF flyback converter, the output-rectifier conduction loss can be reduced by replacing the Schottky rectifier with the synchronous rectifier (SR). Contrary to the forward converter, the VF flyback converter cannot be implemented with self-driven SRs [2]. However, the complexity and cost of the SR implementation can be minimized by using a hybrid driving approach and a discrete driver, as shown in Fig. 7. In the implementation in Fig. 7, the gate-source capacitance of the SR is charged by the voltage induced on the driving winding of power transformer T through diode D and current-limiting resistor R. The secondary current is sensed by current transformer TA. When the secondary current of T flows in the positive direction, the secondary current of TA freewheels through diode D1. As soon as the secondary current of T reverses its polarity, the TA secondary current starts flowing into the base of bipolar transistor Q which discharges the SR gate-source capacitance and turns the SR off. The 360-Ω resistor across the gate and source terminal of the SR ensures that the SR is off during the remaining time of the switching period. Figure 6 shows the full-load waveforms of the experimental VF flyback converter with SR.

As shown in Fig. 4, by replacing the Schottky rectifier with the SR, the rectification loss is reduced by 35 %. If any further efficiency improvement is required, bridge-type dc-dc topologies should be employed.

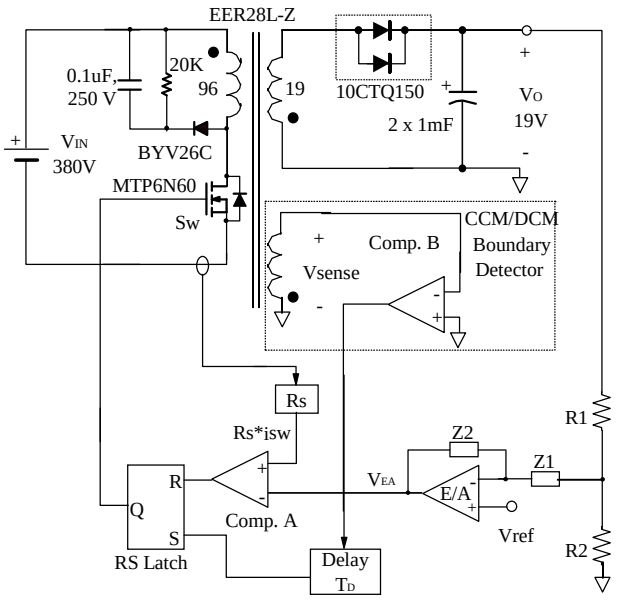

Fig. 5 Variable-frequency soft-switched flyback converter.

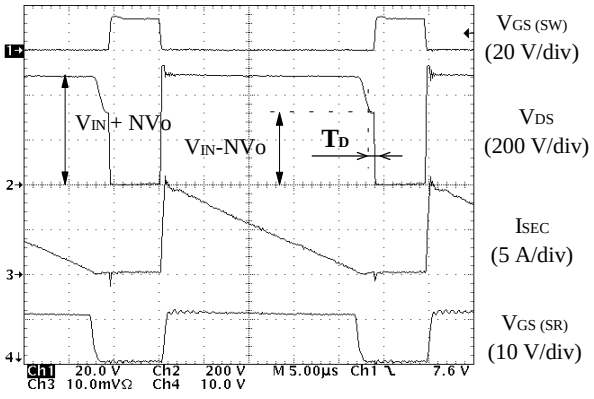

Fig. 6 Experimental waveforms of variable-frequency flyback converter at full load. $V_{GS(SW)}$ - switch gate-source voltage; V_{DS} - switch drain-source voltage; I_{SEC} - transformer secondary current; $V_{GS(SR)}$ - SR gate-source voltage.

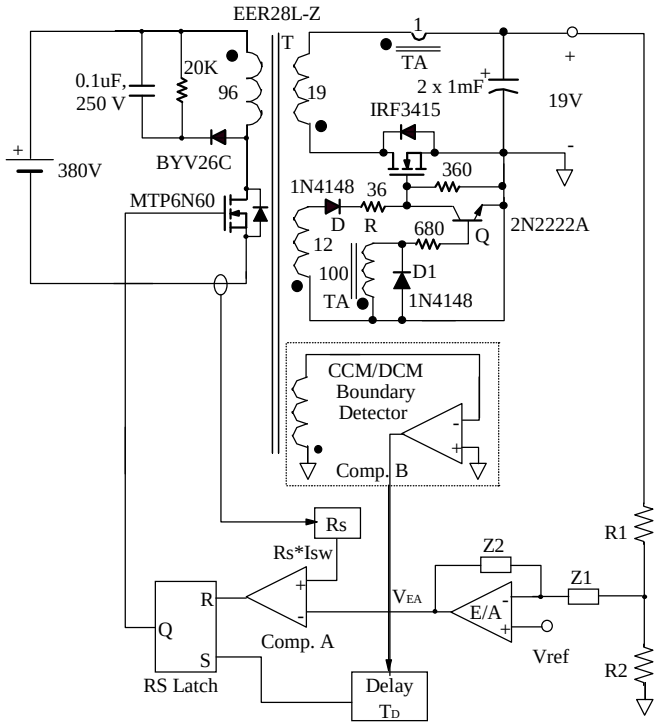

Fig. 7 Variable-frequency soft-switched flyback converter with synchronous rectifier.

III. Evaluation of Half-Bridge Implementations

A. PWM Asymmetrical Half-Bridge Converter

Simplified circuit diagram of the PWM asymmetrical half-bridge (AHB) converter is shown in Fig. 8. The AHB circuit operates with a duty cycle in the range from 0 to 0.5, where duty cycle D is defined as the ratio of the top switch on-time to the switching period. Detailed analysis of the operation and design guidelines for the AHB converter can be found in [4, 5]. The AHB converter complexity and cost are considerably higher than those of the flyback converter since it requires two switches with a 500-V voltage rating, a high-side driver for the top switch, a more complex center-tapped transformer, and an output filter inductor. In addition, the primary of the transformer in the AHB converter carries a significant dc magnetizing current which is required to balance the charge of capacitor Cs. As a result, to prevent the transformer from saturation, its core must be gapped. The saturable reactors on the secondary side allow to use the energy stored in the output filter inductor to achieve ZVS of the primary switches. Due to a large amount of energy stored in the output inductor, the circuit operates with ZVS in a wide load range. In addition, the saturable reactors damp the resonance between the transformer leakage inductance and the rectifier junction capacitance so that R-C snubbers across the output rectifiers are not required. To prevent the cross-conduction of the switches, it is necessary to provide delays between turn-off of one switch and turn-on of the other. Usually, these delays are implemented by a simple RCD network. The output voltage of the AHB converter can be regulated by a number of commercially available low-cost controllers.

The calculated breakdown of the semiconductor losses in the AHB converter is shown in Fig. 4, whereas Fig. 9 shows the oscillograms of key waveforms of the experimental PWM AHB prototype. The experimental circuit was implemented using the UC3845 controller.

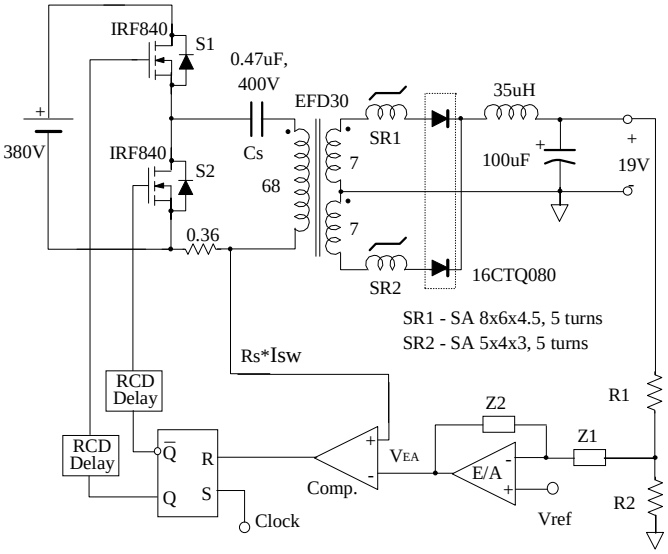

Fig. 8 PWM asymmetrical half-bridge converter.

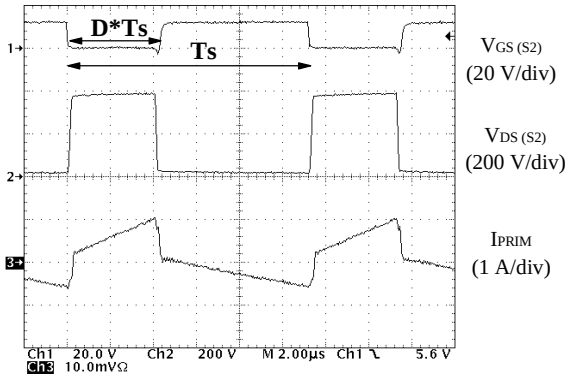

Fig. 9 Experimental waveforms of PWM asymmetrical half-bridge converter at full load. $V_{GS(S2)}$ - switch S2 gate-source voltage; $V_{DS(S2)}$ - switch S2 drain-source voltage; I_{PRIM} - transformer primary current.

B. Resonant HB Converter

A simplified circuit diagram of the resonant HB converter is shown in Fig. 10. The circuit operates with the 50 % duty cycle and its output is regulated by the frequency modulation.

Unlike the traditional half-bridge series-parallel resonant converter (SPRC) [6, 7], the converter in Fig. 10 employs only one capacitor on the primary side and the simple capacitive output filter.

The design of the resonant tank component values is based on the fundamental harmonic approximation [7]. According to this approximation, all voltages and currents in the power stage are represented by their fundamental harmonics, and the high-order harmonics are suppressed by the resonant tank filter. The equivalent circuit of the converter power stage is shown in Fig. 11, where capacitor C_P and load resistance R_O are reflected to the primary side, and L_M, N are magnetizing inductance and turns ratio of the transformer. Inductor L_S represents the sum of the transformer-leakage and external inductance. Among resonant converters, the series resonant converter (SRC) has the minimum circulating energy which allows to maximize its efficiency at full load [7]. However, the SRC cannot regulate the output voltage at light load, and its frequency variation within the load range is relatively wide. The addition of parallel capacitor C_P provides a path for resonant tank current to flow at no load condition so that the converter can maintain the desired output voltage at light loads. Since the light-load operation is achieved at the expense of increased circulating energy, there is a trade-off between the selection of C_p and the efficiency at full power. In order to achieve a high efficiency at full power, the capacitor Cp value should be selected as small as possible, but still large enough to allow the light-load operation. Therefore, all resonant tank components, except Cp, are selected assuming that the role of the capacitor Cp at full power is negligible. After the power stage prototype was built, the Cp value was adjusted empirically to assure the circuit operation at light load.

To minimize switching losses, the operation frequency corresponding to the full power was selected below 100 kHz. To achieve ZVS, the tank input current should lag behind the tank input voltage, but this lag should not be too large to avoid excessive energy circulation. For this reason, the minimum operating frequency was chosen to be 5-10 % higher than the tank resonant frequency. The selection of Q-factor of the tank is a trade-off between the high circulating energy at Q >> 1 and very wide operating frequency range at Q << 1. The selection of Q close to unity seems to be the best choice.

The power density of the converter can be increased by integrating the resonant inductor with the power transformer. The required high value of the transformer leakage inductance can be achieved by physically separating the primary winding from the secondary winding.

Since the resonant tank components operate with high ac voltages and currents, and the resonant converter efficiency is sensitive to the resonant tank losses, low-loss components were used for the resonant tank. Specifically, in the experimental circuit, mica and mylar capacitors with low ESR were employed for C_s and C_p respectively, whereas the integrated transformer/inductor was constructed using the low-loss PC44 ferrite core and the Litz wire for the windings.

The circuit experimental waveforms are shown in Fig. 12. Due to ZVS, the waveforms show minimal ringing. The operating frequency range is from 79 kHz at full load to 236 kHz at no load. The computed losses of the semiconductor devices are shown in Fig. 4.

IV. COMPARISONS

The calculated maximum stresses of the key components in the experimental converters are summarized in Table I. As can be seen from Table I, both current and voltage stresses of the components are considerably lower for the half-bridge converters compared to those for the flyback implementations. Although the flyback converters feature a single magnetic component, the total volume of the magnetic components for the flyback and HB converter is approximately equal because of a higher switching frequency of the HB implementations. The rms current of the secondary rectifiers is considerably lower in the PWM AHB converter than that in the flyback converters. However, according to Fig. 4, the rectification loss in the flyback converters is slightly lower because each of the paralleled diodes carries only half of the total current.

The output capacitor choice is determined by the required ESR value. According to Table I, the largest output capacitor is required for the VF flyback topology due to a triangular shape of its secondary current waveform. The PWM AHB converter requires the smallest capacitor at the output since the shape of its inductor current waveform is close to rectangular.

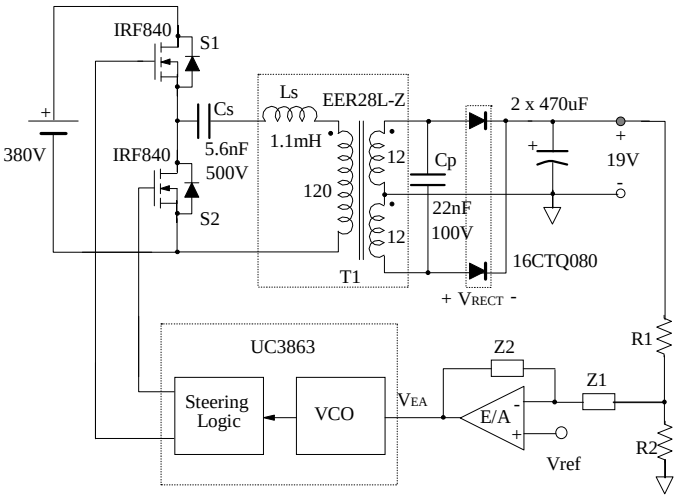

Fig. 10 Resonant HB converter.

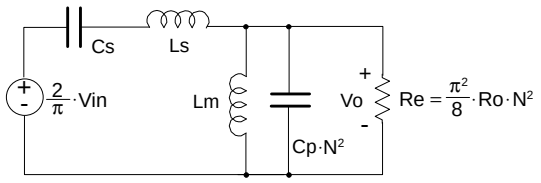

Fig. 11 Ac equivalent circuit of half-bridge resonant converter.

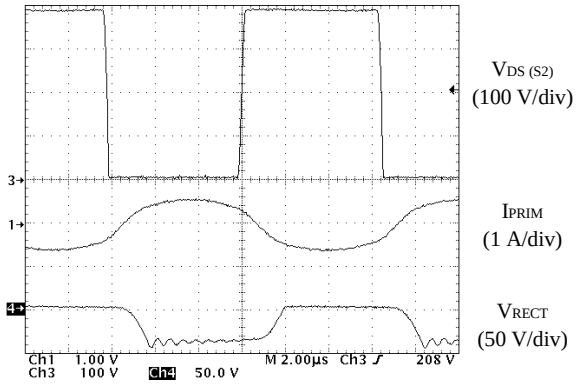

Fig. 12 Experimental waveforms of half-bridge resonant converter at full load. $V_{DS\ (S2)}$ - switch S2 drain-source voltage; I_{PRIM} - primary current; V_{RECT} - secondary rectifier voltage.

The measured efficiency of the flyback converters is plotted in Fig. 13. The efficiency of the VF flyback converter with Schottky rectifier at full load is only 0.4 % higher than the corresponding efficiency of the constant-frequency implementation because of the increased conduction losses in the VF implementation. As expected, the VF flyback converter with the SR exhibits the highest efficiency among the various flyback implementations.

The measured efficiency of the AHB and the resonant HB converter are shown in Fig. 14. As a reference, the efficiency curve of the VF flyback converter with the SR is also shown in Fig. 14. As can be seen in Fig. 14, the PWM AHB converter has the highest efficiency in the entire load range. The full-load efficiency of the PWM AHB converter is 0.5 % higher than the corresponding efficiency of the resonant HB implementation. Also, the efficiency of the resonant HB converter is 1.4-2.0 % higher than the efficiency of the flyback converter with the SR.

Finally, Table II summarizes the full-load efficiency, soft-switching feature, and the relative cost of the dc/dc power stage, as well as the drive requirements, frequency range, and the relative cost of the corresponding control.

It should be noted that the total efficiency of the various adapter implementations is the product of the boost front-end efficiency and the dc-dc stage efficiency. The measured efficiency of the boost front-end stage operating in the critical conduction mode was 94% at the low line (90 Vac) and 98% at the high line (265 Vac). The same boost front-end stage was used in all five implementations.

TABLE I

CALCULATED MAXIMUM COMPONENT STRESS

CONVERTER TOPOLOGY	Switch Voltage Stress	Switch Current Stress	Rectifier Voltage Stress	Required Output Capacitor ESR / Current
PWM Flyback	540 V	0.43 Arms	85 V	31 mΩ / 2.13 Arms
VF Flyback with Schottky Rectifier	525 V	0.48 Arms	95 V	27 mΩ / 2.52 Arms
VF Flyback with Synchronous Rectifier	525 V	0.48 Arms	95 V	27 mΩ / 2.52 Arms
PWM AHB Converter	380 V	0.29 Arms, 0.24 Arms	46 V	654 mΩ / 0.13 Arms
Resonant HB Converter	380 V	0.43 Arms, 0.43 Arms	42 V	52 mΩ / 0.89 Arms

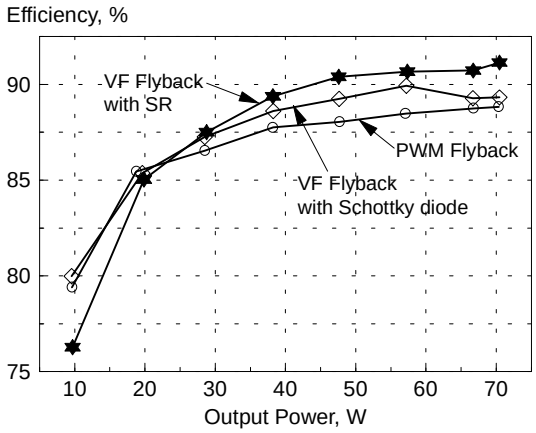

Fig. 13. Measured efficiency of flyback implementations.

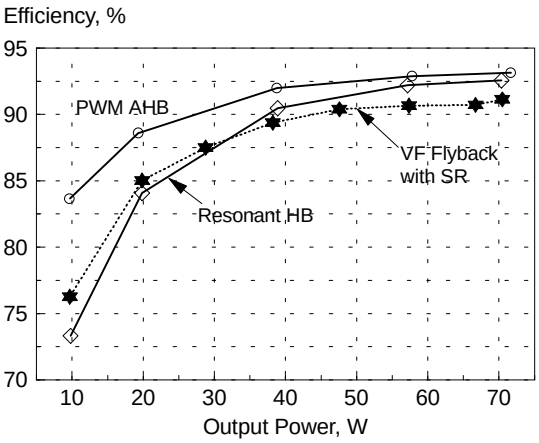

Fig. 14. Measured efficiency of half-bridge implementations.

TABLE II

COMPARISON OF POWER STAGE AND CONTROL IMPLEMENTATIONS

CONVERTER TOPOLOGY	POWER STAGE			CONTROL		
	Efficiency	Soft Switching	Cost	High-Side Driver Required	Frequency Range	Cost
PWM Flyback	88.8 %	No	Low	No	50 kHz	Low
VF Flyback with Schottky Rectifier	89.3 %	Yes	Low	No	35-92 kHz	Medium
VF Flyback with Synchronous Rectifier	91.1 %	Yes	Medium	No	35-68 kHz	Medium-High
PWM AHB	93.1 %	Yes	High	Yes	90 kHz	Medium-High
Resonant HB	92.6 %	Yes	Medium -High	Yes	80-240 kHz	High

IV. SUMMARY

Various implementations of the flyback and half-bridge topology were evaluated for their suitability for high-power-density, two-stage 70-W notebook adapters. The comparative evaluation was performed with respect to the conversion efficiency, component stresses, size, and complexity. It was shown that the half-bridge implementations exhibit higher efficiencies than the flyback implementations at the expense of increased circuit complexity and cost.

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