Design Considerations of Transformer DC Bias of Forward Converter with Active-Clamp Reset

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Abstract - In the forward converter with active-clamp reset circuit, the leakage inductance of the transformer and the parasitic capacitances of the switches produce a dc bias of the magnetizing current of the transformer. The dc bias of the magnetizing current could saturate the transformer core, cause diode reverse recovery problem, and make the active clamp switch lose zero voltage turn-on if the bias is not considered in the transformer design. This paper derives the explicit equation of the dc bias of the magnetizing current for the first time and provides the transformer design procedures according to the derived equations.

I. INTRODUCTION

The performance of the forward converter is strongly dependent on the transformer-reset method. Generally, it has been established that the active-clamp reset approach offers a better performance than the other reset approaches because it allows the operation of the converter with a maximum duty cycle well above 50%, with a minimum stress on the semiconductor components [1]. In fact, due to a large maximum duty cycle, the turns ratio of the transformer can be increased, which decreases the conduction loss on the primary side and allows the selection of the secondary-side rectifiers with a lower breakdown rating, and, consequently, a lower forward-voltage drop. In addition, the active-clamp-reset method recycles the magnetizing energy of the core, as opposed to the other methods (RCD-clamp method, for example) that dissipate this energy. As a result, the conversion efficiency of the forward converter with the active-clamp reset can be higher than that of the same topology with the other reset schemes. Also, the active-clamp reset approach results in the optimal use of the transformer core, since the core is excited symmetrically in the first and third quadrants of the B-H plane. However, the active-clamp-reset method requires an extra switch with the associated drive and a resonant capacitor, i.e., it increases the complexity and the cost of the power stage. Nevertheless, this method seems indispensable in achieving the optimum performance of the forward-converter topology.

A number of papers have discussed design issues relate to the active clamp reset mechanism [2-7]. The negative dc bias of the magnetizing current in the active clamp circuit has been observed and mentioned in the literature [2]. However, no detailed analysis and explicit equations have been provided in the paper. It is very important to estimate the dc bias of the magnetizing current before the prototyping, so that the dc bias can be considered in the original transformer design.

In this paper, we all show that there is a positive or a negative dc bias of the magnetizing current of the transformer in the circuit due to the parasitic capacitance, C_s, and the leakage inductance, L_{lk}. This dc bias could saturate the transformer, cause diode reverse recovery problem, and make the active clamp switch lose zero voltage turn-on. This paper will analyze the dc operation of the active clamp circuit with the parasitic parameters L_{lk} and C_s, derive the numerical equations of the dc bias, and provide the design guideline regarding the dc bias of the transformer. It is the first time that a numerical equation of the dc bias of the magnetizing current has been provided in a paper.

II. PRINCIPLE OF OPERATION

The forward converter power-stage with the active-clamp reset is shown in Fig. 1. The reset circuit consists of auxiliary switch S_2 and clamp-capacitor C_c. To simplify the analysis of operation, it is assumed that the inductance of output-filter inductor L_f is large so that the output filter can be represented by constant-current source I_o. In addition, it is assumed that all semiconductors are ideal. It should be noted that the transformer is modeled as a parallel connection of magnetizing inductance Lm and the ideal transformer with the turns-ratio $n = \frac{N_p}{N_s}$ as shown in Fig. 2. To further facilitate the explanation of operation, Fig. 2 shows topological stages of the simplified circuit during a switching cycle, whereas Fig. 3 shows the essential waveforms.

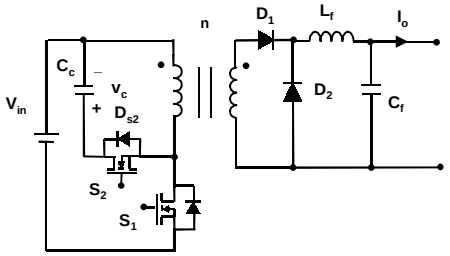
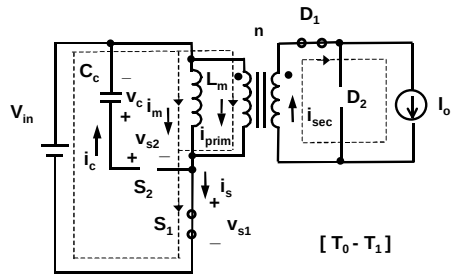
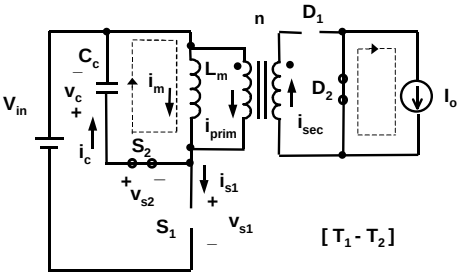


Fig. 1. Forward converter power-stage with the active-clamp reset.



(a)



(b)

Fig. 2. Circuit operation diagrams of the simplified active-clamp forward converter. (a) $[T_0\text{-}T_1]$ interval. (b) $[T_1\text{-}T_2]$ interval.

Since in this analysis, ideal switches with zero switching times are assumed, a complementary gate-drive signals without a dead time are used as shown in Fig. 3. Because of the true complementary gate-drives, the circuit has only two topological stages as shown in Fig. 2.

During the interval $[T_0\text{-}T_1]$, when main switch S_1 is on, the corresponding topological stage is shown in Fig. 2(a). During this sage, output current I_o flows through the secondary winding inducing primary current, $i_{prim} = \frac{I_o}{n}$. At the same time, because a constant positive input voltage V_{in} is connected across the primary of the transformer, magnetizing current i_m increases with a constant slope. During the on time of the switch, switch current i_{s1} is given by the sum of primary current i_{prim} and magnetizing current i_m, as shown in Fig. 3.

When main switch S_1 is turned off at $t = T_1$, output current is instantaneously commutated from rectifier D_1 to freewheeling rectifier D_2, because the leakage inductance of the transformer is neglected, as shown in Fig. 2 (b). At the same time, magnetizing current i_m is commutated from main switch S_1 to the anti-parallel diode of the auxiliary switch S_2. Since S_2 is turned on at $t = T_1$ while its anti-parallel diode is conducting, i.e., while the voltage across it is zero, switch S_2 is turned on under zero-voltage-switching (ZVS) condition. There is no additional turn-on loss at this instant. Due to a negative voltage v_c across the primary winding of the transformer, i_m decreases. If clamp voltage v_c is assumed constant, i.e., if the clamp capacitor capacitance is large, the down-slope of i_m is constant as shown in Fig. 3.

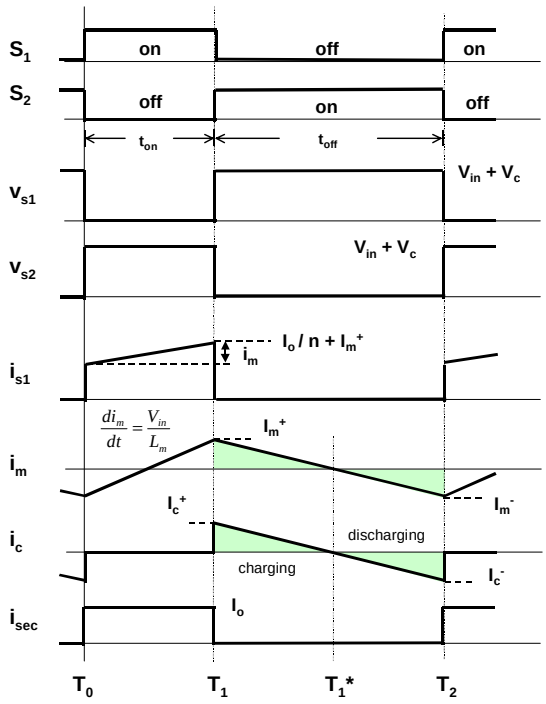


Fig. 3. Key waveforms of the circuit operation of the simplified forward converter with the active-clamp reset.

After i_m reaches zero at $t = T_1^*$, it continues to flow in the negative direction through the transistor (channel) of the closed auxiliary switch S_2. This topological stage ends when auxiliary switch S_2 is turned off and main switch S_1 turned on at $t = T_2$, initiating a new switching cycle.

From the flux-balance requirement of the transformer core, it follows that

$$V_{in} \cdot t_{on} = V_c \cdot t_{off} \tag{1}$$

i.e., clamp voltage V_c is given by

$$V_c = \frac{D}{1-D} \cdot V_{in} \tag{2}$$

where, t_{on} is the on time of main switch S_1, t_{off} is the off time of S_1, $D = \frac{t_{on}}{T_s}$ is the duty cycle of S_1, and T_s is the switching period.

From the charge-balance requirement of the clamp capacitor, it follows that

$$I_c^+ = I_c^- \tag{3}$$

where $I_c^+ = i_c(t_1)$ and $I_c^- = i_c(t_2)$, as shown in Fig. 3.

Since during the off-time, main switch S_1 is off, $i_c = i_m$, it also follows that

$$I_m^+ = I_m^- \tag{4}$$

where $I_m^+ = i_m(t_1)$ and $I_m^- = i_m(t_2)$.

Therefore, the dc component of the magnetizing current of the circuit in Fig. 1 is equal to zero. However, if the parasitic capacitance of the semiconductors and leakage inductance of the transformer are not neglected, the magnetizing current possesses a dc bias, as discussed next.

III. Effect of the Parasitic Capacitance and the Leakage Inductance of the Transformer

As described in the previous section, the average magnetizing current i_m over one switching cycle is zero in an ideal circuit as shown in Fig. 1. However, there is a positive or negative dc bias of the transformer magnetizing current in steady state when the parasitic capacitance C_s, and the leakage inductance of the transformer L_{lk} are considered. The circuit diagram is shown in Fig. 4, in which C_s is the total equivalent parasitic capacitance of the main switch, S_1, active clamp switch, S_2, and the transformer, and L_{lk} is the leakage inductance of the transformer.

In this section, we will show that the amplitude of the dc bias of the magnetizing current is a function of C_s, L_{lk}, input voltage, and load. The positive dc bias is due to the extra energy stored in the parasitic capacitance, and the negative dc bias is due to the extra energy stored in the leakage inductance of the transformer. A large positive dc bias could saturate the transformer core or have diode reverse recovery problem; and a large negative dc bias could saturate the transformer core or lose ZVS of the active-clamp switch as shown in Fig. 5. This section is going to explain the dc bias phenomenon and derive the explicit equation of the dc bias of the magnetizing current, so that the problem related to the dc bias current can be considered in the original transformer design.

A. Positive dc bias of the magnetizing current

Fig. 6 shows the steady state operation waveforms of the active-clamp forward converter with a positive dc bias of the magnetizing current. The positive dc bias of the magnetizing current happens when the energy stored in the leakage inductance L_{lk} is less than the energy stored in the parasitic capacitance C_s. Because of the parasitic capacitance and the leakage inductance, the operation of the circuit in Fig. 4 is slightly different than the one in Fig. 1. The difference can be seen after main switch S_1 is turned off. There are six stages during a switching cycle.

Stage 1 [T_0 - T_1]: After the main switch S_1 is turned on at $t = T_0$, the output current I_o flows through rectifier D_1, inducing a current in the primary winding of the transformer. L_m is charged by input voltage V_{in}. As a result, the main switch current i_{s1} during this interval is given by

$$i_{s1} = i_m + \frac{I_o}{n}. \qquad (5)$$

This topological stage ends at $t = T_1$, when the main switch S_1 is turned off.

Stage 2 [T_1 - T_2]: After the main switch S_1 is turned off at T_1, capacitor C_s is charged by the reflected load current in the primary winding, $\frac{I_o}{n}$. This stage ends when v_{s1} reaches the input voltage V_{in} at T_2.

Stage 3 [T_2 - T_3]: After v_{s1} reaches V_{in}, the secondary voltage becomes equal to zero, and the transformer is shorted. Since the current in rectifier D_1 cannot be reduced to zero immediately due to the leakage inductance, D_1 and D_2 are simultaneously conducting during this period. The leakage inductance i_{lk} starts to resonate with C_s. This stage terminates at $t = T_3$, when the current in D_1 decreases to zero and the leakage inductance current i_{lk} becomes equal to the magnetizing current i_m. During this stage, the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted.

Stage 4 [T_3 - T_4]: At T_3, D_1 disconnects, and the transformer is an open circuit. Since the energy stored in C_s is larger than the energy in L_{lk}, C_s has not been charged to $V_{in} + V_c$ at T_3. L_m and L_{lk} continue to resonate with C_s until $v_{s1} = V_{in} + V_c$ at T_4.

Stage 5 [T_4 - T_4^*]: At T_4, current in the leakage inductance and the magnetizing inductance continues to flow through the anti-parallel diode of switch S_2 and clamp capacitor C_c. Due to a negative voltage V_c across the magnetizing inductance, i_m decreases. If capacitance C_c is assumed large so that the ripple of the clamp voltage V_c is small compared to the dc component, the downslope of i_m is constant. This stage ends, when i_m reaches zero at $t = T_4^*$. The active clamp switch, S_2, can be turned on anytime during this period with ZVS.

Stage 6 [T_4^* - T_5]: When the current in the anti-parallel diode of switch S_2 reaches zero at T_4^*, the active clamp switch S_2 starts to conduct. The magnetizing current, i_m, will continue to flow in the opposite direction through S_2. This stage ends at $t = T_5$, when switch S_2 is turned off.

According to the charge balance, the shaded area of i_c during [T_4 - T_4^*] interval is equal to the one during [T_4^* - T_5] interval as shown in Fig. 6, i.e. $i_c^+ = i_c^-$. The magnetizing current i_m follows the charge current i_c during [T_4 - T_5] interval, but during [T_3–T_4] interval, C_s is charged by i_m and i_{lk}. Since $L_m >> L_{lk}$, L_{lk} is neglected. The additional variation of i_m in this period induces additional magnetizing current, i.e., $I_m^+ > I_m^-$, where, $I_m^+ = i_m(t_3)$ and $I_m^- = i_m(t_5)$.

In order to maintain the flux balance, there is a positive dc bias of the magnetizing current in the transformer as shown in Fig. 6. If the dc bias of the magnetizing current is too large, I_m^- is positive during the whole switching cycle, the magnetizing current is still conducting through the anti-parallel diode of the active-clamp switch S_2 when the main switch S_1 is turned on. As a result, there is a large diode reverse recovery current conducting through diode D_{s2} to the

main switch, S_1, which could damage the semiconductor devices.

According to the energy balance during [T_2 - T_5],

$$\frac{1}{2}\cdot L_{lk}\cdot i_{lk}(t_2)^2+\frac{1}{2}\cdot L_m\cdot i_m(t_2)^2-\frac{1}{2}\cdot(L_{lk}+L_m)\cdot i_m(t_5)^2 = \frac{1}{2}\cdot C_S\cdot(v_s(t_5)-V_{in})^2-\frac{1}{2}\cdot C_S\cdot(v_s(t_2)-V_{in})^2 \quad (6)$$

where

$$i_{lk}(t_2)=\frac{I_o}{n}+i_m(t_2) \quad (7)$$

$$i_m(t_2)=i_m(t_3)=I_m^{+} \quad (8)$$

$$i_m(t_5)=I_m^{-} \quad (9)$$

$$v_s(t_2)=V_{in} \quad (10)$$

$$v_s(t_5)=V_{in}+V_c \quad (11)$$

When $\frac{I_o}{n} >> i_m$, we can simplify (6) to:

$$\frac{1}{2}\cdot L_m\cdot\left(I_m^{+}\right)^2-\frac{1}{2}\cdot L_m\cdot\left(I_m^{-}\right)^2\approx\frac{1}{2}\cdot C_S\cdot V_c^{\,2}-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \quad (12)$$

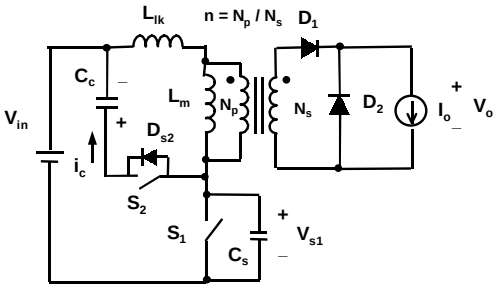


Fig. 4. Circuit diagram of the active-clamp forward converter with the equivalent parasitic capacitance C_s and the leakage inductance of the transformer L_{lk}.

B. *Negative dc bias of the magnetizing current*

Fig. 7 shows the steady state operation waveforms of the active-clamp forward converter with a negative dc bias of the magnetizing current. The negative dc bias of the magnetizing current happens when the energy stored in the leakage inductance L_{lk} is larger than that in the parasitic capacitance C_s. There are six stages during a switching cycle, in which stages 1, 2, 5, and 6 are the same as in the positive dc-bias current case. Only stage 3 and 4 are different, which are [T_2 - T_3] and [T_3 - T_4] intervals.

Stage 3 [T_2 - T_3]: After main switch S_1 is turned off and v_{s1} reaches V_{in} at T2, the secondary voltage becomes equal to zero, and the transformer is shorted. Since the current in the rectifier diode D_1 cannot be reduced to zero immediately due to the leakage inductance of the transformer, D_1 and D_2 are simultaneously conducting during this period. The leakage inductance i_{lk} resonates with C_s until C_s is charged to V_{in} + V_c at T_3.

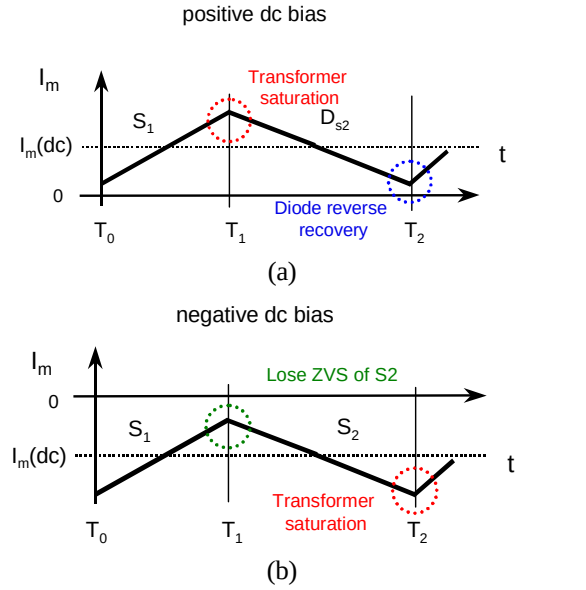


Fig. 5. Problems due to the dc bias of the magnetizing current of the transformer. (a) a large positive dc bias could saturate the transformer core or have diode reverse recovery problem. (b) a large negative dc bias could saturate the transformer core or lose ZVS of the active-clamp switch turn-on.

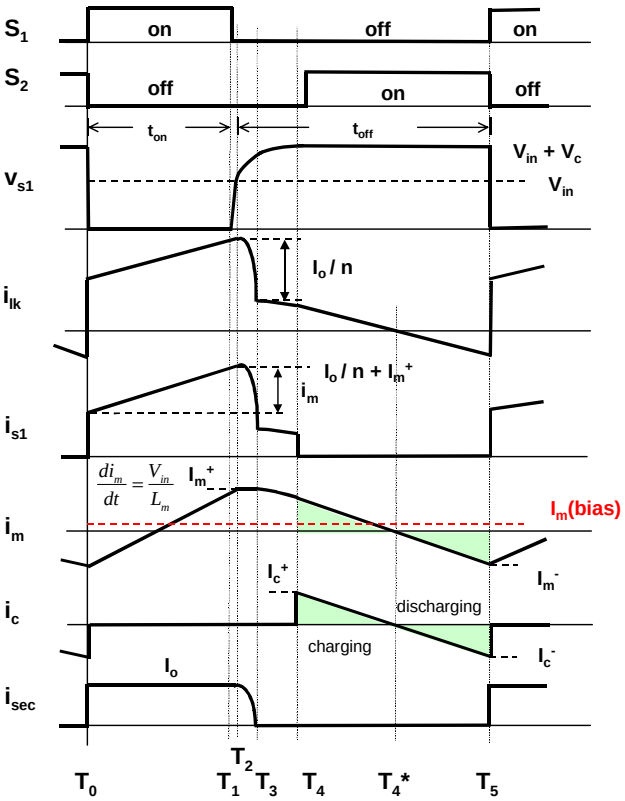


Fig. 6. Circuit operation waveforms with positive dc bias of the magnetizing current.

Since the energy stored in L_{lk} is larger than the energy in C_s, the leakage inductance current i_{lk} is larger than the magnetizing current i_m at T_3. During this stage, the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted.

Stage 4 [T_3 - T_4]: At T_3, current in the leakage inductance, which is larger than the magnetizing current, continues to flow through the anti-parallel diode of switch S_2 and resonate with the clamp capacitor C_c. D_1 and D_2 are still simultaneously conducting during this stage, and the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted. This stage terminates at t = T_4, when the leakage current i_{lk} is equal to the magnetizing current i_m. At T_4, D_1 disconnects, and the transformer is an open circuit. At the next stage, L_m and L_{lk} start to resonate with C_c, which is the same as discussed in the positive dc-bias current case.

According to the charge balance, the shaded area of i_c during [T_3 - T_4^*] interval is equal to [T_4^* - T_5] as shown in Fig. 7. During [T_3 - T_4], C_c is charged by leakage inductance i_{lk}. The magnetizing current i_m only follows i_c during [T_4 - T_5], the two shaded area of i_m is not equal. i.e., $I_m^+ < I_m^-$, where $I_m^+ = i_m(t_4)$ and $I_m^- = i_m(t_5)$. In order to maintain the flux balance, there is a negative dc bias of the magnetizing current in the transformer as shown in Fig. 7.

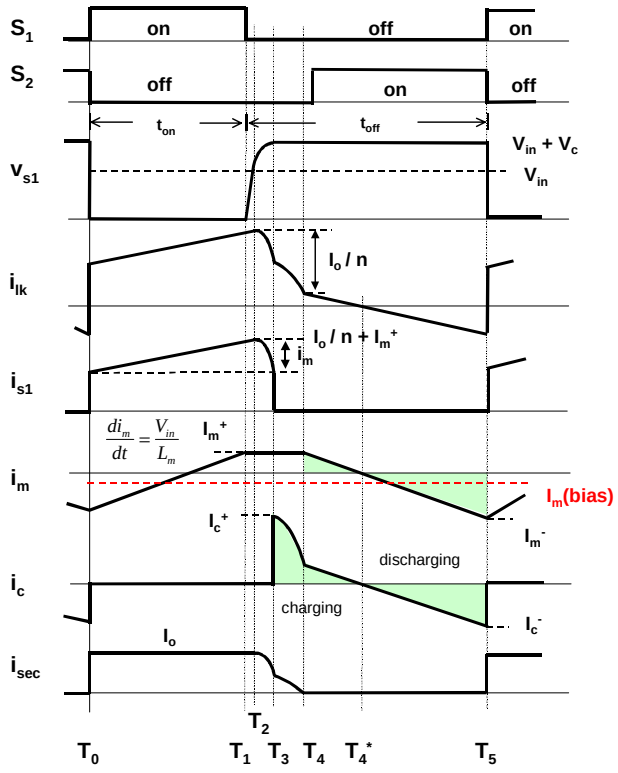


Fig. 7. Circuit operation waveforms of the negative dc bias of the magnetizing current.

If the dc bias of the magnetizing current is too large, I_m^+ is negative when v_{s1} reaches V_{in} + V_c at T_2. As a result, the current flows through the active-clamp switch, S_2, instead of the anti-parallel diode when S_1 is turned off and S_2 is turned on. In this condition, S_2 is turned on with hard switching, that increase the loss of the circuit.

According to the energy balance during [T_2 - T_5],

$$\frac{1}{2}\cdot L_{lk}\cdot i_{lk}(t_2)^2+\frac{1}{2}\cdot L_m\cdot i_m(t_2)^2-\frac{1}{2}\cdot(L_{lk}+L_m)\cdot i_m(t_5)^2 = \frac{1}{2}\cdot C_S\cdot(v_s(t_5)-V_{in})^2-\frac{1}{2}\cdot C_S\cdot(v_s(t_2)-V_{in})^2 \quad (13)$$

where

$$i_{lk}(t_2)=\frac{I_o}{n}+i_m(t_2) \quad (14)$$

$$i_m(t_2)=i_m(t_3)=i_m(t_4)=I_m^+ \quad (15)$$

$$i_m(t_5)=I_m^- \quad (16)$$

$$v_s(t_2)=V_{in} \quad (17)$$

$$v_s(t_5)=V_{in}+V_c \quad (18)$$

When $\frac{I_o}{n} >> i_m$, we can simplify (13) to:

$$\frac{1}{2}\cdot L_m\cdot(I_m^+)^2-\frac{1}{2}\cdot L_m\cdot(I_m^-)^2\approx\frac{1}{2}\cdot C_S\cdot V_c^2-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \quad (19)$$

IV. Derivation of the DC Bias of the Magnetizing Current

According to the energy balance equations (12) and (19), for both the positive and the negative dc-bias current, we get:

$$\frac{1}{2}\cdot L_m\cdot(I_m^+)^2-\frac{1}{2}\cdot L_m\cdot(I_m^-)^2=\frac{1}{2}\cdot C_S\cdot V_c^2-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \quad (20)$$

This equation can also be written as

$$\frac{1}{2}\cdot L_m\cdot(I_m^+ + I_m^-)\cdot(I_m^+ - I_m^-)=\frac{1}{2}\cdot C_S\cdot V_c^2-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \quad (21)$$

Since [T_1-T_2] interval is very short, the peak to peak magnetizing current can be approximated by

$$I_m(pp)=I_m^+-I_m^-=\frac{V_{in}\cdot D\cdot T_s}{L_m} \quad (22)$$

Let

$$I_m(bias)=\frac{1}{2}\cdot(I_m^+ + I_m^-) \quad (23)$$

$$E_{Cs}=\frac{1}{2}\cdot C_s\cdot V_c^2 \quad (24)$$

$$E_{Llk}=\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \quad (25)$$

where I_m(bias) is the dc bias of the magnetizing current, E_{cs} is the energy stored in the parasitic capacitance C_s, and E_{Llk} is the energy stored in the leakage inductance L_{lk}.

Replacing (21) with (22) - (25), the dc bias of the magnetizing current can be written as

$$I_m(bias) = \frac{E_{Cs} - E_{Llk}}{V_{in} \cdot D \cdot T_s} \quad (26)$$

In addition, the maximum magnetizing current is:

$$I_m(\max) = \left|I_m(bias)\right| + \frac{1}{2} \cdot I_m(pp) = \frac{\left|E_{Cs} - E_{Llk}\right|}{V_{in} \cdot D \cdot T_s} + \frac{V_{in} \cdot D \cdot T_s}{2 \cdot L_m} \quad (27)$$

The terms in the equations are defined as in Fig. 8. Fig. 9 shows the positive bias magnetizing current curves with different input voltages and the parasitic capacitances, C_s. The worst case of the positive dc bias occurs at low line, which has a larger duty cycle, and thus a higher clamp capacitor voltage, V_c.

Fig. 10 shows the negative dc bias magnetizing current curves with different loads and the leakage inductances, L_{lk}. The worst case of the negative dc bias occurs at full load and large L_{lk}, since more energy stored in the leakage inductance under this condition.

Fig. 11 shows the simulation and calculation results of the dc bias of the magnetizing current under different input voltage and load conditions. The circuit specification is: V_{in} = 100 - 400 V, V_o = 5 V, I_o = 0 - 20 A with L_{lk} = 5 uH and C_s = 600 pF. The simulated curves are dotted lines and the calculated curves are solid lines. The results match very well. Fig. 11 shows that the negative dc bias is more severe than the positive dc bias, due to the range of the parameter values. The negative bias magnetizing current is the major concern in an practical circuit design.

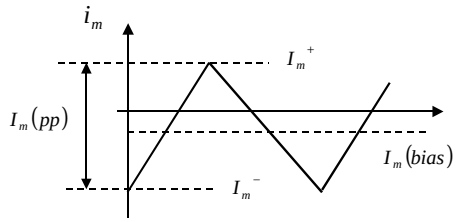


Fig. 8. Definition of the terms in the bias magnetizing current equations.

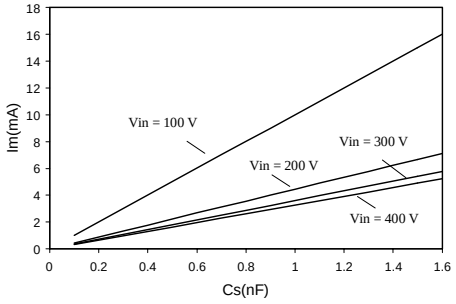


Fig. 9. The positive dc bias of the magnetizing current is related to the input voltage and the parasitic capacitance.

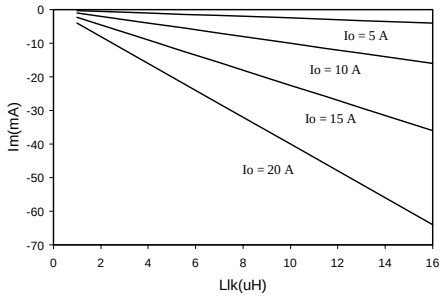


Fig. 10. The negative dc bias of the magnetizing current is related to the load current and the leakage inductance.

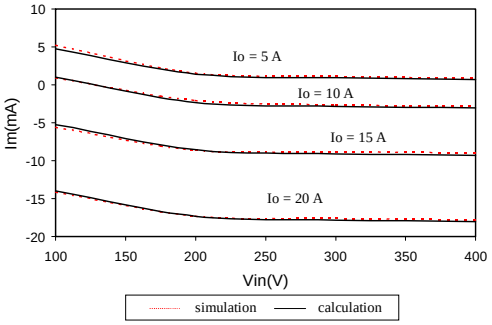


Fig. 11. Simulated and calculated dc bias curves with different loads and input voltages when L_{lk} = 5 uH and C_s = 600 pF.

V. Design Guideline

This section shows how to take into account the dc bias of the magnetizing current in the transformer design according to derived equations. In the following example, the circuit specification and parameters are: V_{in} = 100 - 400 V, I_o = 0 - 20 A, transformer turns ratio n = 10, switching frequency F_s = 100 kHz, and the equivalent parasitic capacitance C_s = 600 pF. The design procedure is as follows:

Step 1: Estimate the largest leakage inductance of the circuit and calculate the maximum dc bias of the magnetizing current.

Fig. 12 shows the calculated dc bias of the magnetizing current with L_{lk} = 5 uH according to (26). The largest dc bias occurs at no load and low line, and the largest negative dc bias occurs at full load and high line. The maximum dc bias is 18 mA at full load and high line as shown in Fig. 12.

Step 2: Design the transformer with the flux bias of the transformer core.

The flux bias of the transformer core due to the parasitic capacitance and the leakage inductance is:

$$B_{bias} = \mu \cdot \frac{N_p \cdot \max\left(\left|I_m(bias)\right|\right)}{l_e} \quad (28)$$

where $\max\left(\left|I_{m\_dc}\right|\right)$ is the maximum dc bias current, N_p is the primary winding turns, and l_e is the magnetic path length. The condition for not to saturate the transformer core is

$$\frac{1}{2}\cdot B_{pp} + B_{bias} < B_{sat} \tag{29}$$

where,

$$B_{pp} = \frac{V_{in}\cdot \Delta t}{N_p \cdot A_e}, \tag{30}$$

in which, A_e is the effective cross sectional area of the core.

Step 3: After the initial transformer design, verify that the bias magnetizing current is not too large to affect the normal steady state operation.

The condition for the circuit not to have diode reverse recovery problem and can reach ZVS of active-clamp switch is:

$$I_m(pp) > 2\cdot \max\left(\left|I_{m\_dc}\right|\right). \tag{31}$$

So the criteria of the magnetizing inductance is:

$$L_m < \frac{V_{in}\cdot \Delta t}{2\cdot\left|I_{m\_dc}\right|} \tag{32}$$

where,

$$L_m = \frac{\mu \cdot {N_p}^2 \cdot A_e}{l_e} \tag{33}$$

Step 4: Redesign the transformer when the criteria of (32) on step 3 is not satisfied.

Fig. 13 shows the maximum L_m vs. L_{lk} curve. The shaded area in Fig. 13 shows the magnetizing inductance, L_m, which can be used in the circuit with different leakage inductances, L_{lk}. If L_m is larger than the values in the shaded area, the transformer needs to be redesigned by tightly coupling the transformer to reduce the leakage inductance L_{lk}, or adding an air gap in the transformer core to reduce the magnetizing inductance L_m.

It is worth to mention that additional design consideration is recommended for the large-signal transient behavior of the active-clamp reset circuit [7], which is not covered in this paper.

VI. Conclusions

There is a positive or a negative dc bias of the magnetizing current of the transformer in steady state due to the parasitic capacitance, Cs, and the leakage inductance, Llk in the forward converter with active-clamp reset circuit.

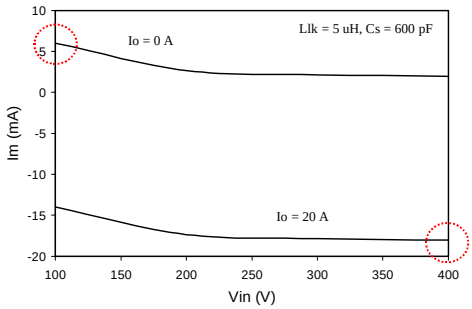


Fig. 12. Calculated maximum dc bias of the circuit when L_{lk} = 5 uH and C_s = 600 pF.

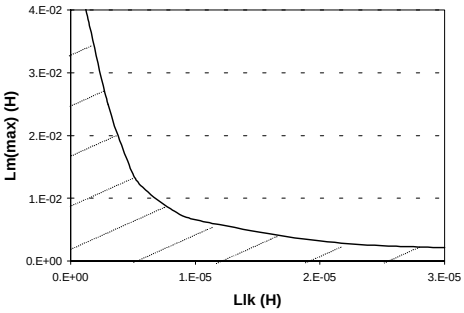


Fig. 13. The maximum L_m vs. L_{lk} curve. The shaded area shows the magnetizing inductance, L_m, which can be used in the circuit.

This dc bias of the magnetizing current could saturate the transformer, cause diode reverse recovery problem, and make the active clamp switch lose zero voltage turn-on. This paper provides a transformer design guideline regarding these issues. The explicit equations of the bias magnetizing current are derived in the paper.

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