Single-Stage Input-Current-Shaping Technique with Voltage-Doubler-Rectifier Front End

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Abstract - In this paper, a new single-stage input-current-shaping (ICS) technique that integrates the voltage-doubler-rectifier front end with a dc/dc output stage is introduced. Due to the voltage-doubler-rectifier front end, the reduction of line-current harmonics can be achieved with a higher conversion efficiency compared to the corresponding single-stage ICS circuit with the conventional wide-range full-bridge rectifier. In addition, the proposed technique requires energy-storage capacitors with a lower voltage rating and smaller total capacitance than the conventional single-stage ICS counterpart, which reduces the size and cost of the power supply. The performance of the proposed technique is evaluated on a 100-W (5-V/20-A) experimental prototype circuit.

I. INTRODUCTION

A number of single-stage input-current shaping (ICS) techniques have been introduced recently. In a single-stage approach, input-current shaping, isolation, and high-bandwidth control are performed in a single step, i.e., without creating an intermediate dc bus. Among the single-stage circuits, a number of circuits described in [1]-[10] seem particularly attractive because they can be implemented with only one semiconductor switch and a simple control. All these single-stage, single-switch input-current shapers (S^4ICSs) integrate the boost-converter front end with the forward-converter or the flyback-converter dc/dc stage.

Although it has been demonstrated that the S^4ICSs described in [1]-[10] can achieve the desired performance in a variety of applications, the S^4ICS power supplies have significant difficulties meeting performance expectations in universal-line (90-270 Vac) applications with a hold-up time requirement. For example, most of today's desktop computers and computer peripherals require power supplies that are capable of operating in the 90-270-Vac range and can provide a hold-up time of at least 10 ms. Generally, the hold-up time is the time during which a power supply must maintain its output voltage(s) within a specified range after a drop-out of the line voltage. The hold-up time is used to orderly terminate the operation of a computer or to switch over to an uninterruptible-power-supply (UPS) operation after a line failure. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor, C_B, which is used to handle the differences between the varying instantaneous input power and a constant output power. The difficulty of these S^4ICS circuits to deal with a wide line range and long hold-up time requirement stems from the fact that the voltage of the energy-storage capacitor, V_C, varies with the line voltage and load current [4]. In most applications, with a proper design, V_C can be kept in the 410-420 Vdc range, which warrants a use of a 450-V electrolytic capacitor. Since the value of C_B is determined from the hold-up time requirement at the minimum line (worst case), the S^4ICS approach requires a relatively bulky and expensive energy-storage capacitor. Moreover, due to a wide-range variation of V_C that is the input to the dc/dc output stage, the conversion efficiency of the dc/dc output stage is reduced. In contrast, the two-stage approach, in which V_C is independently regulated at approximately 380 Vdc, requires a much smaller and, therefore, cheaper electrolytic capacitor rated at 450 V, or even 400 V. In addition, due to a regulated V_C, the efficiency of the dc/dc output stage in the two-stage approach can be made higher compared to that in the single-stage approach.

Generally, the performance of conventional, universal-line-range power supplies without ICS can be improved by employing a voltage-doubler rectifier (VDR) [11]. The output voltage of a VDR front end is approximately the same for both the low-line range (100/120-Vac power line) and the high-line range (220/240-Vac power line). Specifically, for the universal-line range, the VDR output voltage varies from approximately 180 Vac to 270 Vac. Since this voltage range is much narrower than the corresponding voltage range of the conventional wide-range full-bridge rectifier (FBR), the conversion efficiency of the dc/dc output stage can be improved. In addition, because the minimum voltage of a VDR is twice as high as that of the wide-range FBR, the total capacitance required for a given hold-up-time specification is approximately one-half of that required in the wide-range FBR. Finally, energy-storage capacitors in a VDR need to be rated at only 250 Vdc, or even 200 Vdc. Usually, electrolytic capacitors with a lower voltage rating are significantly cheaper than their counterparts with a higher voltage rating.

In this paper, a new single-stage ICS technique that integrates the voltage-doubler-rectifier front end with a dc/dc output stage is introduced. Based on this concept, two families of voltage-doubler single-stage ICS (VDS^2ICS)

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converters are developed: a VDS^{2}ICS family with 2-terminal ICS cells and a VDS^{2}ICS family with 3-terminal ICS cells. In Section II, generalized circuit diagrams and principles of operation for both VDS^{2}ICS families are provided. Experimental results obtained on a 100-W (5-V/20-A) prototype circuit are given in Section III.

II. Principles of Operation

A. VDS^{2}ICS Family with 2-Terminal ICS Cells

Fig. 1 shows the generalized circuit diagram of the VDS^{2}ICS family with 2-terminal ICS cells. As shown in Fig. 1, two identical ICS cells are inserted between full-bridge rectifier FBR and energy-storage capacitors C_{B1} and C_{B2}, in both the positive and the negative rails. Each ICS cell includes a boost inductor and a high-frequency dither source [1] connected in series. The function of the dither sources 1 and 2 is to provide high-frequency charging and discharging of boost inductors L_{B1} or L_{B2}, respectively, so that their average inductor current (which is equal to the line current) follows the line voltage. The high-frequency dither sources are generated by utilizing a switching waveform in the dc/dc power stage. Fig. 2 shows a number of implementations of dither sources 1 and 2. Each dither source consists of two paths: a path for charging and a path for discharging the corresponding boost inductor. Each of the two paths includes a series connection of a winding (N_1 or N_2) inductively coupled to the transformer TR in the dc/dc power stage and at least one of the following components: a diode, an inductor, and a capacitor. The two paths of each dither source are connected in parallel; therefore, each dither source has two terminals. It should be noticed that topologically dither sources 1 and 2 are identical. The only difference between dither sources 1 and 2 is in the polarity of the terminals (X and Y). The dc/dc power stage in Fig. 1 can be any known isolated power conversion topology such as pulse-width-modulated (PWM) forward, flyback, half-bridge, and full-bridge topology, or any soft-switching topology.

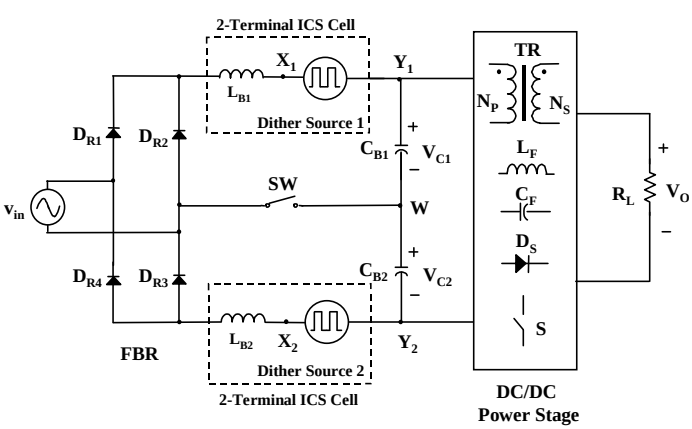

Fig. 1 Generalized circuit diagram of the VDS^{2}ICS family with 2-terminal ICS cells

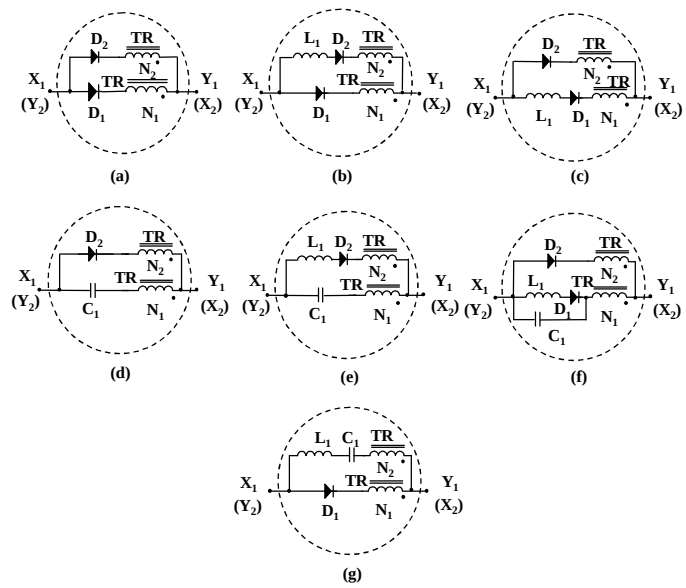

Fig. 2 Implementations of dither sources 1 and 2 in the 2-terminal ICS cells in Fig. 1: a) DCM source, (b) and (c) CCM current sources, (d) CCM voltage source, (e) and (f) CCM voltage-current sources, (g) resonant source. Polarity of terminals for dither sources 2 is given in parenthesis.

In all implementations of the dither sources in Fig. 2, the high-frequency signal is obtained by windings N_1 and N_2. If $N_2 < N_1$, the boost inductors charge through the path with winding N_1 (when the switch in the dc/dc power stage is closed) and discharge through the path with winding N_2 (when the switch in the dc/dc power stage is open). During the charging of boost inductors L_1 and L_2, the voltage across windings N_1 in dither sources 1 and 2 is in opposition to the voltage across bulk capacitors C_{B1} and C_{B2}, thereby enabling the voltage across the boost inductors to be positive. For proper operation, the number of turns of winding N_1 should be selected as $0 < N_1 \le N_P/2$. During the discharging of the boost inductors, the voltage across windings N_2 has the same direction as the voltage across the bulk capacitors. Therefore, windings N_2 effectively increase the reset voltage across the boost inductors. However, the circuit in Fig. 1 will also properly operate when $N_2 = 0$.

It should be noticed that for all implementations of the dither sources in Fig. 2, except for the discontinuous-conduction-mode (DCM) source in Fig. 2(a), boost inductors L_{B1} and L_{B2} operate in the continuous conduction mode (CCM). It should be also noticed that the DCM dither source in Fig. 2(a) can be implemented with a single charging/discharging path when $N_2 = N_1$.

Figs. 3 and 4 show the operation modes of the proposed circuit in Fig. 1 in the low-line and high-line ranges, respectively. In the low-line range, range-select switch SW is closed and the front end operates in the voltage-doubler mode. As shown in Fig. 3(a), during a positive half cycle of the line voltage, with switch S in the dc/dc power stage closed, voltage v_{D1} across dither source 1 is at its maximum [$v_{D1} = V_{D1max} > 0$, where $V_{D1max} < (V_{C1}+V_{C2})/2 \approx V_{C1}$]

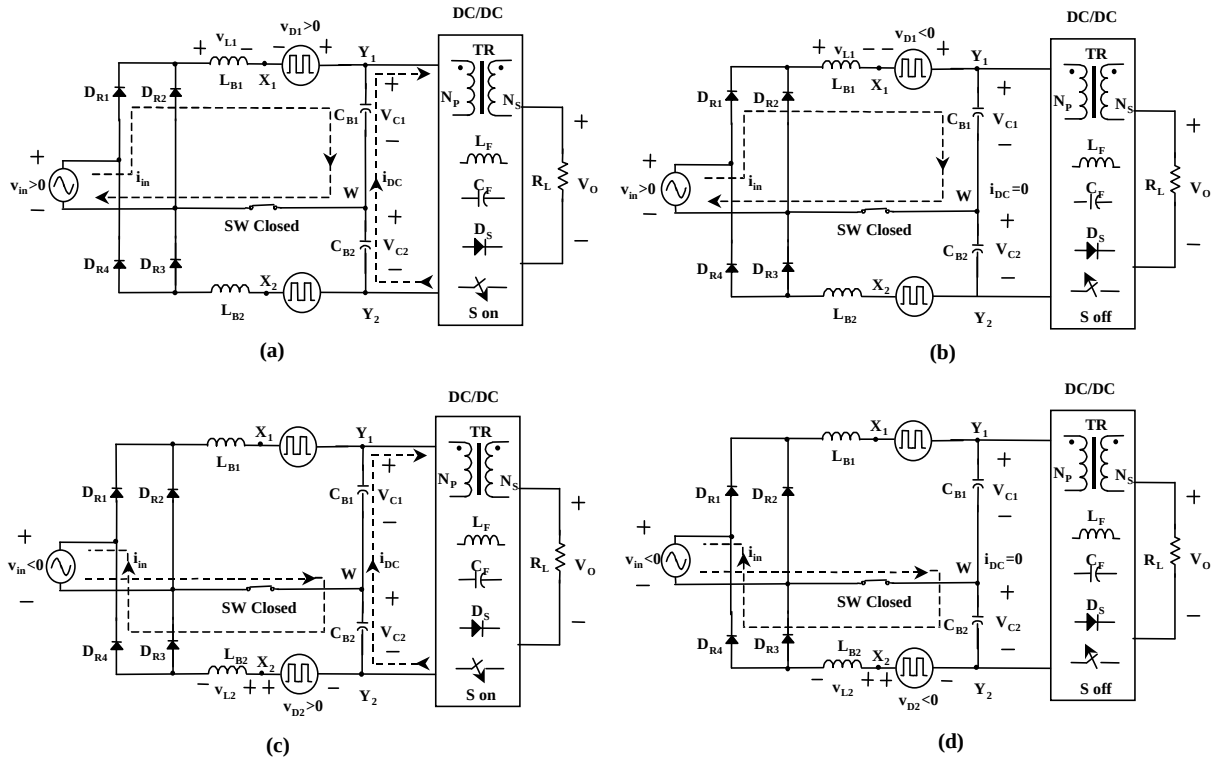

Fig. 3 Operation modes of the VDS^{2}ICS circuit with 2-terminal ICS cells at low-line range: (a) $v_{in}>0$, S on; (b) $v_{in}>0$, S off; (a) $v_{in}<0$, S on; (a) $v_{in}<0$, S off

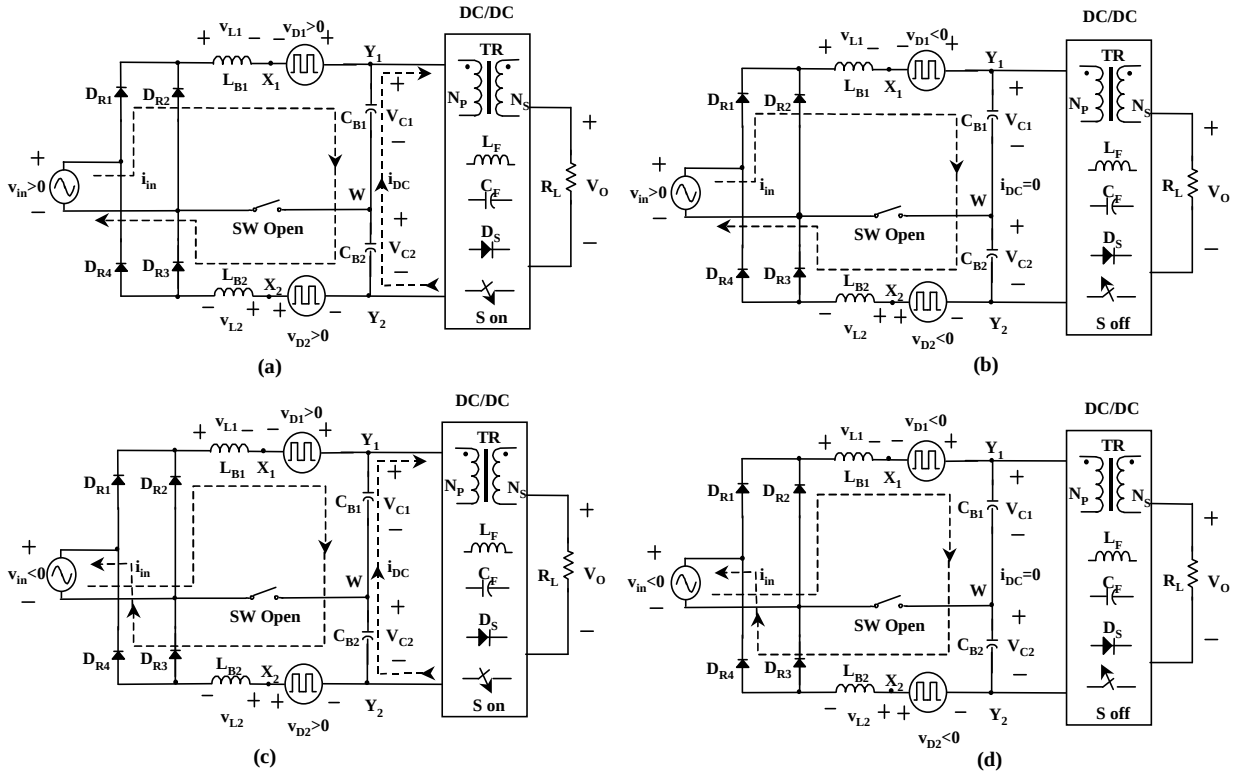

Fig. 4 Operation modes of the VDS^{2}ICS circuit with 2-terminal ICS cells at high-line range: (a) $v_{in}>0$, S on; (b) $v_{in}>0$, S off; (a) $v_{in}<0$, S on; (a) $v_{in}<0$, S off

and in opposition to voltage V_{C1}. If the instantaneous line voltage is larger than $V_{C1} - V_{D1max}$, then voltage v_{L1} across L_{B1} ($v_{L1} = v_{in} + V_{D1max} - V_{C1}$) is positive and line current i_{in} increases, thereby storing energy in the boost inductor. At the same time, input current i_{DC} of the dc/dc power stage is supplied from energy-storage capacitors C_{B1} and C_{B2}. When switch S in dc/dc power stage opens, Fig. 3(b), current i_{DC} falls to zero, and voltage v_{D1} across dither source 1 changes sign ($v_{D1} = V_{D1min} < 0$), thus increasing the total voltage opposing the line voltage. Consequently, voltage v_{L1} across L_{B1} ($v_{L1} = v_{in} - |V_{D1min}| - V_{C1}$) becomes negative, current i_{in} decreases, and the boost inductor discharges so that the energy stored in L_{B1} is transferred to C_{B1}. It should be noticed that since line current i_{in} cannot flow when v_{in} is smaller than $V_{C1} - V_{D1max}$, the line current is distorted around zero crossings. During a negative half cycle of the line voltage, the circuit in Fig. 1 operates in a similar manner as during a positive half cycle, except that diode D_{R4}, boost inductor L_{B2}, dither source 2, and bulk capacitor C_{B2} are active, as shown in Figs. 3(c) and (d).

When the circuit in Fig. 1 operates in the high-line range, range-select switch SW is open and the front end operates as a conventional full-bridge rectifier. As shown in Fig. 4, when operating as a conventional rectifier, boost inductors L_{B1} and L_{B2}, dither sources 1 and 2, and energy-storage capacitors C_{B1} and C_{B2} are connected in series. During a positive half cycle of the line voltage, when switch S in the dc/dc power stage is closed, Fig. 4(a), voltages v_{D1} and v_{D2} across dither sources 1 and 2 are each at their maximum [$v_{D1} = V_{D1max} > 0$ and $v_{D2} = V_{D2max} > 0$, where $V_{D1max} \approx V_{D2max} < (V_{C1}+V_{C2})/2$], opposing voltages V_{C1} and V_{C2} across energy-storage capacitors C_{B1} and C_{B2}, respectively. If the instantaneous line voltage is larger than $(V_{C1}+V_{C2}) - (V_{D1max}+V_{D2max})$, then the sum of voltages v_{L1} and v_{L2} across L_{B1} and L_{B2}, i.e., $v_{L1}+v_{L2} = v_{in} + (V_{D1max}+V_{D2max}) - (V_{C1}+V_{C2})$, is positive and line current i_{in} increases, thereby storing energy in the boost inductors. At the same time, dc/dc power stage draws current i_{DC} from the serially connected energy-storage capacitors C_{B1} and C_{B2}. When switch S in dc/dc power stage opens, Fig. 4(b), current i_{DC} falls to zero. Simultaneously, voltages v_{D1} and v_{D2} across the dither sources change signs, i.e., $v_{D1} = V_{D1min} < 0$ and $v_{D2} = V_{D2min} < 0$, thus increasing the total voltage opposing the line voltage. Consequently, the sum of the voltages across boost inductors L_{B1} and L_{B2}, $v_{L1} + v_{L2} = v_{in} - |V_{D1min} + V_{D2min}| - (V_{C1} + V_{C2})$, becomes negative, thus decreasing line current i_{in} and transferring the energy stored in the boost inductors to the energy-storage capacitors. It should be noticed that since line current i_{in} cannot flow when $v_{in} < (V_{C1}+V_{C2}) - (V_{D1max}+V_{D2max})$, the line current is distorted around zero crossings. During a negative half cycle of the line voltage, the operation of the circuit is similar to the operation during a positive half cycle, except that rectifiers D_{R2} and D_{R4} are conducting line current i_{in}, as shown in Figs. 4(c) and (d).

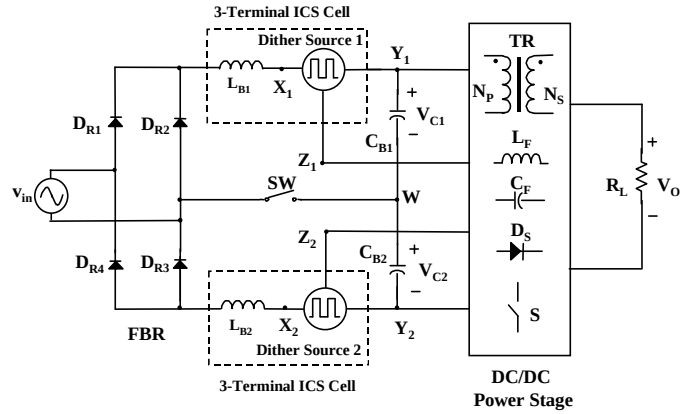

Fig. 5 Generalized circuit diagram of the VDS^{2}ICS family with 3-terminal ICS cells

It should be also noticed that, since windings N_1 and N_2 are magnetically coupled to the secondary winding of transformer TR in the dc/dc power stage, they can be used to directly transfer energy from the input (line) to the load. Winding N_1 provides direct energy transfer with the forward-type dc/dc power stages, while winding N_2 provides direct energy transfer with the flyback-type dc/dc power stages. Generally, direct energy transfer improves conversion efficiency.

B. VDS^{2}ICS Family with 3-Terminal ICS Cells

Fig. 5 shows the generalized circuit diagram of the VDS^{2}ICS family with 3-terminal ICS cells. As in the case of

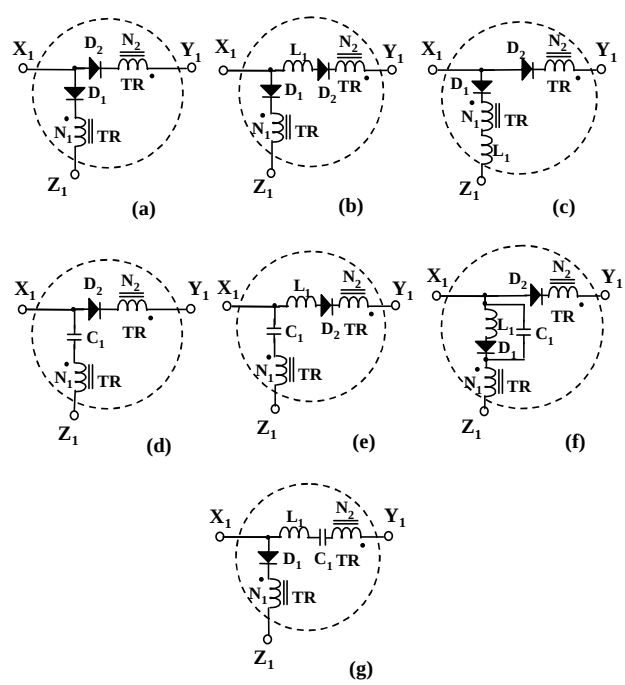

Fig. 6 Implementations of dither source 1 in the 3-terminal ICS cell in Fig. 5: a) DCM source, (b) and (c) CCM current sources, (d) CCM voltage source, (e) and (f) CCM voltage-current sources, (g) resonant source

the 2-terminal ICS cells, each 3-terminal ICS cell includes a boost inductor and a dither source connected in series. However, different from the 2-terminal ICS cell, the dither source in a 3-terminal ICS cell is connected to the dc/dc power stage at two terminals (Y and Z). Fig. 6 shows various implementations of dither source 1. Similarly to a dither source in the 2-terminal ICS cells, each dither source in Fig. 6 includes two paths: a path for charging and a path for discharging the boost inductor (L_{B1}). It should be noticed that topologically the two paths of a dither source in Fig. 6 are identical to those of the corresponding dither sources in Fig. 2, except that the polarity of winding N_1 is opposite. However, different from the 2-terminal ICS cell, the two paths of a dither source in the 3-terminal ICS cell are not connected in parallel. Only the discharging path (X_1Y_1) is connected to the energy-storage capacitor, while the charging path (X_1Z_1) is connected to a pulsating node, i.e., to the switch inside the dc/dc power stage, similarly to the implementation of the S^4ICS circuits in [8]. During the charging of boost inductor L_{B1}, the voltage across winding N_1 opposes the rectified line voltage, thereby decreasing the positive voltage across the boost inductor. This reduces the storage-capacitor voltage, as explained in [8]. For proper operation, the number of turns of winding N_1 should be selected as $0 \le N_1 < N_P/2$. The implementations of dither source 2 in the negative rail of the circuit in Fig. 5 are similar to those in Fig. 6 except that the polarity of all diodes and the polarity of windings N_1 and N_2 are opposite to those in Fig. 6.

Different from the VDS^2ICS circuit with 2-terminal ICS cells, the VDS^2ICS circuit with 3-terminal ICS cells can only be implemented with single-ended dc/dc power stages such as the forward and flyback power stages shown in Fig. 7. Because of the required symmetry of the power stage, the primary winding of the transformer is split in half and switch S is connected between the split windings. Nevertheless, the operation of the circuit in Fig. 5 is very similar to the operation of the circuit in Fig. 1.

Windings N_1 and N_2 in the dither sources in Fig. 6 can be implemented either as additional transformer windings of transformer TR in the dc/dc power stage or as portions of the

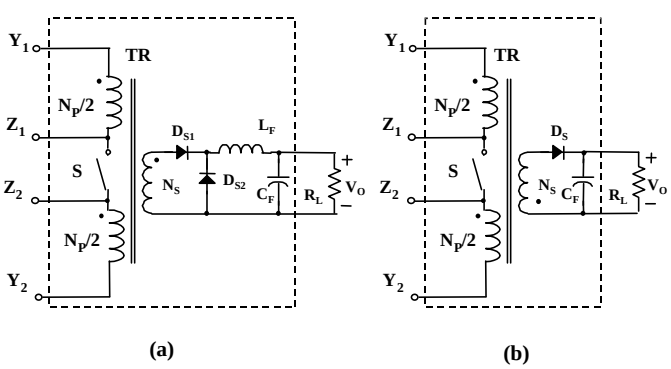

Fig. 7 Implementation of dc/dc power stage in Fig. 5: (a) forward converter, (b) flyback converter

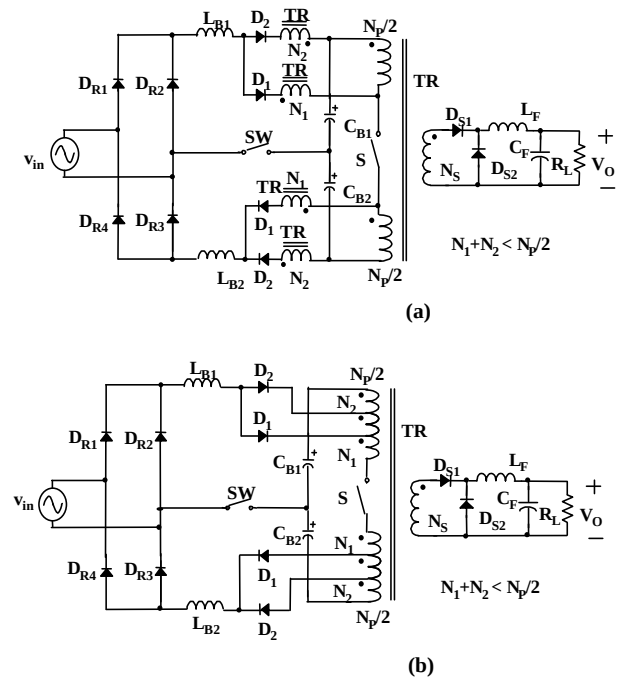

Fig. 8 Two implementations of windings N_1 and N_2 in the DCM dither source in Fig. 6(a)

split primary winding of transformer TR by employing tapping. As an example, Fig. 8 shows the two implementations of windings N_1 and N_2 in the DCM dither source in Fig. 6(a) combined with the forward dc/dc power stage from Fig. 7(a). Both implementations of windings N_1 and N_2 in Fig. 8 require the same number of pins of transformer TR. However, since the implementation of transformer TR in Fig. 8(b) does not require additional windings, the construction of transformer TR in Fig. 8(b) is simpler than that in Fig. 8(a).

Generally, the VDS^2ICS converters with 2-terminal and 3-terminal ICS cells exhibit similar performance. Differences between them relate to the transformer design and control implementation. As can be seen from Figs. 1 and 2, the 2-terminal ICS cell implementation requires at least two additional transformer windings to implement dither sources 1 and 2 compared to the implementation in Fig. 6 which implements the dither sources by the tapping of the split primary winding. However, the transformer with $N_1 \neq 0$ in the circuit in Fig. 5 requires one more pin compared to the transformer in Fig. 1. Consequently, the implementation in Fig. 1 may require a larger transformer, whereas the implementation in Fig. 5 may require a custom made transformer bobbin. Also, as can be seen from Figs. 5 and 7, in the 3-terminal ICS cell implementation, switch S and lower energy-storage capacitor C_{B2} do not have the same reference voltage, which may affect the design of the switch driver circuit and the control feedback implementation by requiring additional signal isolation.

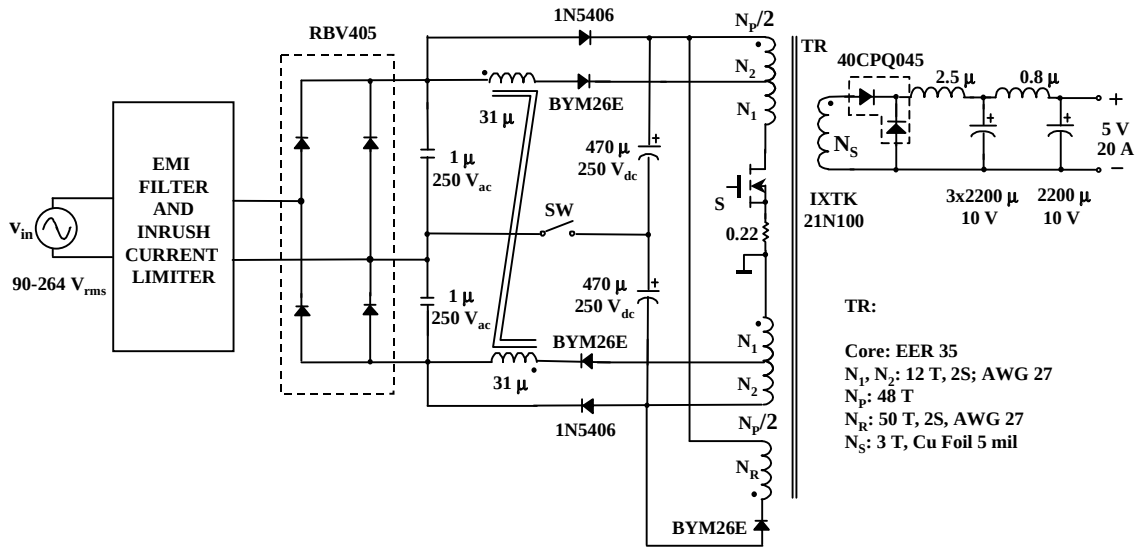

Fig. 9 Experimental circuit

Finally, in both VDS^{2}ICS converters, a single boost inductor can be placed on the ac-side of the rectifier bridge, or the two dc-side boost inductors can be coupled by winding them on the same magnetic core. In addition, in all implementations that use current-type dither sources, i.e., dither sources with inductor L_1 in Figs. 2 and 6, these inductors can be wound on a single core.

III. EXPERIMENTAL RESULTS

The performance of the proposed VDS^{2}ICS technique was verified experimentally on a 100-W (5-V/ 20-A) prototype circuit designed for the universal-line range (90-264 Vac). The circuit diagram of the power stage of the experimental circuit along with the values of the components is shown in Fig. 9. The experimental circuit is an implementation of the circuit in Fig. 8(b) with reduced number of components. Namely, the experimental circuit in Fig. 9 is obtained from the circuit in Fig. 8(b) by connecting together the two tapping points of each half of the split primary winding (N_1+N_2 = N_P/2) and by coupling the two dc-side boost inductors. The control circuit was implemented using the low-cost integrated controller UC3842. The switching frequency was 100 kHz. Measured line-voltage and line-current waveforms at nominal low line (V_{in} = 100 V_{rms}) and nominal high line (V_{in} = 230 V_{rms}), at full load (I_o = 20 A) are shown in Fig. 10. The measured individual line-current harmonics are well below the IEC1000-3-2 Class-D limits,

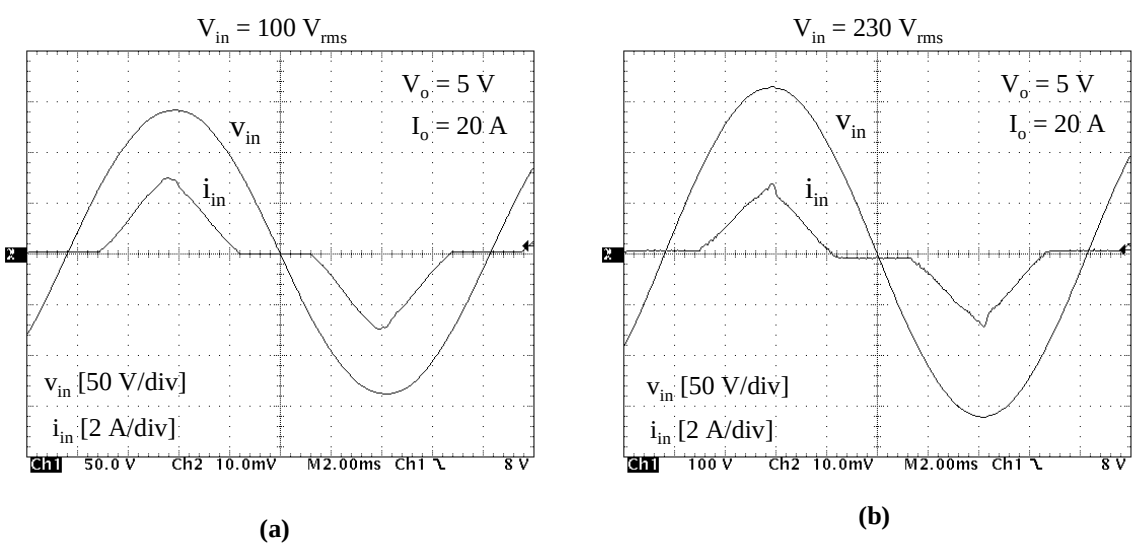

Fig. 10 Experimental line-voltage and line-current waveforms

i.e., they have more than 30% margin for both the nominal low line and high line. Table I summarizes the full-load power-factor (PF), total-harmonic-distortion (THD), bulk-capacitor-voltage ($V_C = V_{C1} + V_{C2}$), and efficiency measurements that include electromagnetic interference (EMI) filter and in-rush current limiter losses.

To illustrate the improved performance of the proposed VDS^{2}ICS technique, the experimental results in Table I were compared with the measurements obtained on the corresponding 100-W (5-V/20-A) S^{4}ICS circuit with the conventional wide-range full-bridge rectifier implemented with a DCM boost inductor, reported in [8]. It should be noted that the major components of the two single-stage ICS circuits are identical. The maximum bulk voltage of the VDS^{2}ICS circuit in Fig. 9 at full load ($I_o = 20$ A) is about 40 V smaller than the maximum V_C of the corresponding S^{4}ICS circuit in [8]. Also, the full-load efficiency of the VDS^{2}ICS circuit in Fig. 9 is around 4% higher than the efficiency of the corresponding S^{4}ICS circuit in [8]. These improvements are the consequence of the significantly narrower bulk-capacitor voltage range of the VDS^{2}ICS circuit in Fig. 9 compared to the S^{4}ICS circuit with the conventional wide-range full-bridge rectifier in [8].

TABLE I
MEASURED PF, THD, V_C, AND EFFICIENCY AT FULL LOAD

V_{in} [V_{rms}]	PF	THD [%]	$V_{C1}+V_{C2}$ [V]	η [%]
90	0.900	46.4	244	77.3
100	0.899	47.2	273	77.4
115	0.896	48.3	316	77.3
132	0.893	49.3	364	76.9
180	0.897	48.0	250	79.2
230	0.891	48.9	320	78.4
264	0.885	49.6	368	77.8

IV. SUMMARY

A new single-stage input-current-shaping (ICS) technique for power supplies with a voltage-doubler-rectifier front end is proposed. The proposed technique significantly improves the performance of single-stage ICS power supplies for universal-line (90-270 Vac) applications with a hold-up time requirement. Specifically, the variation range of the storage-capacitor voltage is reduced by approximately two times compared to the corresponding single-stage ICS circuits with a conventional wide-range full-bridge rectifier. Consequently, the total capacitance of the energy-storage capacitors can be significantly reduced. In addition, the efficiency of the dc/dc power stage can be improved.

The proposed ICS technique makes easy to modify existing power supplies with a voltage-doubler rectifier front end without input current shaping to meet IEC 1000-3-2 and similar line-current-harmonic standards.

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