An Improved CCM Single-Stage PFC Converter with a Low-Frequency Auxiliary Switch*

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ABSTRACT

In this paper, an improved continuous-current-mode, single-stage, power-factor-correction technique is proposed. The proposed technique employs an auxiliary low-frequency switch to achieve a good input power factor, low energy-storage-capacitor voltage stress, and high conversion efficiency. The improved performance was verified experimentally.

1. INTRODUCTION

In order to reduce the component count and improve the performance, a number of single-stage, single-switch PFC (S^4-PFC) techniques have been introduced recently [1]-[7]. In an S^4-PFC converter, input current shaping, isolation, and tight regulation of outputs are achieved in a simple single conversion step with only one switch. According to the shape of the input inductor current, the S^4-PFC circuits can be classified as discontinuous-current-mode (DCM) and continuous-current-mode (CCM) S^4-PFC converters. The DCM S^4-PFC converters normally have fewer components than the CCM S^4-PFC converters, but they suffer from a higher current stress, lower efficiency, and require larger EMI filters. As a result, in many applications, the CCM S^4-PFC converters are preferred over the DCM S^4-PFC converters.

Figure 1 shows a typical DCM S^4-PFC converter [4-[5]. In the circuit in Fig. 1, inductor L_B is the boost inductor which shapes the input current to meet the required harmonic-current standard [8]. Switch S integrates the DCM PFC front end and the output dc/dc converter into one stage. Since during one line cycle the duty cycle of switch S is approximately constant, the average input current of the DCM PFC front-end naturally has a low total harmonic distortion (THD). The tapped winding N_1 is the feedback winding used to limit the voltage stress on energy-storage capacitor C_B and to improve the overall efficiency [5]-[6]. Generally, a higher N_1 reduces the voltage stress of the semiconductor components and capacitor C_B, and improves efficiency. However, a larger N_1 also decreases the conduction angle of the line current and, consequently, increases the line-current harmonics.

To meet PFC requirements in a CCM S^4-PFC converter, the auxiliary inductor L_1, shown in Fig. 2, is required [1-2]. Generally, in the CCM S^4-PFC converter in Fig. 2 designed for universal-line applications, it is difficult to simultaneously maximize the efficiency, meet PFC specifications with acceptable margins, and keep the voltage stress on the energy-storage capacitor low. Specifically, the CCM S^4-PFC converter has difficulty meeting the PFC requirements at high line because of a reduced conduction angle of the line current. In fact, to reduce the line-current harmonics in the CCM S^4-PFC converters, N_1 needs to be significantly lower compared to the N_1 value for the DCM operation, which has a detrimental effect on the conversion efficiency.

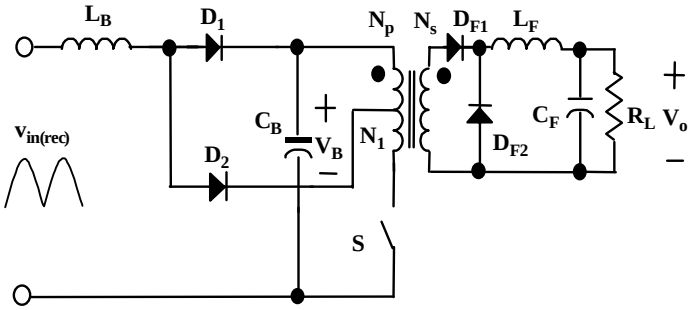

Fig. 1 DCM S^4-PFC converter with tapped primary winding [4].

This paper introduces a new technique which improves the performance of the CCM S^4-PFC converter. The technique employs a low-frequency, low-cost, and low-loss auxiliary switch to extend the conduction angle of the line current without a need to decrease N_1. As a result, in the improved circuit the required reduction of the line-current harmonics can be achieved without sacrificing the conversion efficiency.

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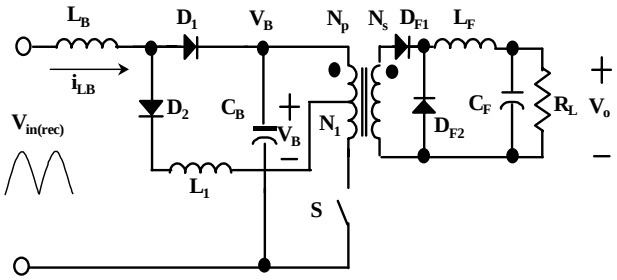

Fig. 2 CCM S^4-PFC converter with tapped primary winding [1].

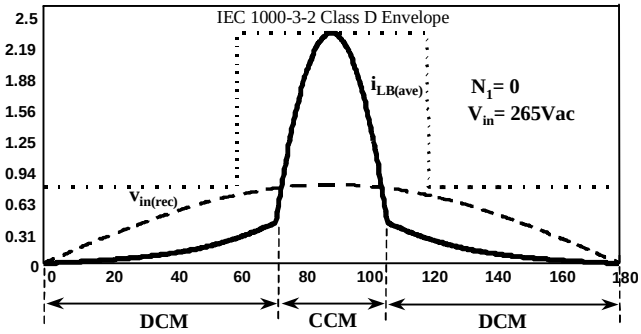

Fig. 4 Average input inductor current $i_{LB(ave)}$ of CCM S^4-PFC at V_{in} = 265 Vac. Calculated THD = 97.8%

2. ANALYSIS OF CCM S^4-PFC WAVEFORMS

To facilitate the explanation of the limitations of the S^4-PFC converter, Fig. 3 shows the calculated average value of boost-inductor current $i_{LB(ave)}$ at a low line of V_{in}=90 Vac and for N_1=0. As can be seen in Fig. 3, when the line voltage is close to the zero crossings, the boost inductor L_B operates in the DCM, and $i_{LB(ave)}$ is very low. For higher instantaneous line voltages, the boost inductor L_B operates in the CCM mode, and the $i_{LB(ave)}$ waveform shows a fast rise of $i_{LB(ave)}$. Since there is a significant current difference between $i_{LB(ave)}$ in the DCM and CCM mode, the line-current distortion is significant. Figure 4 shows the average boost inductor current at a high line of V_{in}=265 Vac. As can be seen from Fig. 4, the ratio of the DCM/CCM angles at the high line is even larger than at the low line. As a result, the current distortion at the high line is higher than that at the low line. To meet the IEC line-current harmonic requirements, it is critical that the values of L_B and L_1 are selected properly. However, even with the optimal selection of the L_B and L_1 values, it is not possible to simultaneously achieve a high efficiency, low voltage stress on the energy-storage capacitor, and desirable margin of the current harmonics.

The performance of both the DCM and CCM S^4-PFC converters can be improved by implementing winding N_1 as a part of the primary winding, as shown in Figs. 1 and 2. In fact, with a tapped winding N_1, the voltage stress on C_B can be reduced without a reduction of the conversion efficiency because a tapped N_1 provides a direct energy path from the input to the output, which enhances efficiency [3], [5]. Generally, if the taping ratio N_1/Np = 0.25 is selected, energy-storage-capacitor voltage V_B can be limited to below 400 V in the majority of applications. With V_B limited to around 400 V, a 450-V rated energy-storage capacitor can be safely used for C_B. Figure 5 shows the line-current waveform at the low line with N_1/Np=0.25 along with the corresponding waveform with N_1/Np=0, *i.e.*, along with the $i_{LB(ave)}$ waveform in Fig. 3. As can be seen from Fig. 5, with the tapping no current flows during the angle where the tapped-winding voltage $(N_1/N_P)V_B$ is lower than instantaneous rectified-line voltage $V_{in(rec)}$. This conduction dead angle that occurs around the zero crossings of the line voltage decreases the CCM conduction angle. As a result, the circuit with the tapping exhibits increased line-current distortion, as illustrated in Fig. 6 which shows the calculated comparison of the line-current harmonics with and without the tapping. As can be seen from Fig. 6, the converter with tapped winding cannot meet the IEC 1000-3-2 requirement. Moreover, even without the tapped winding, the harmonics of the line current are close to the IEC-standard limits.

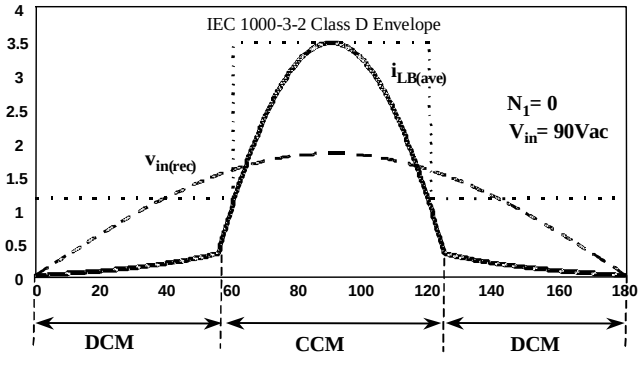

Fig. 3 Average input inductor current $i_{LB(ave)}$ of CCM S^4-PFC at V_{in} = 90 Vac. Calculated THD = 68.9% .

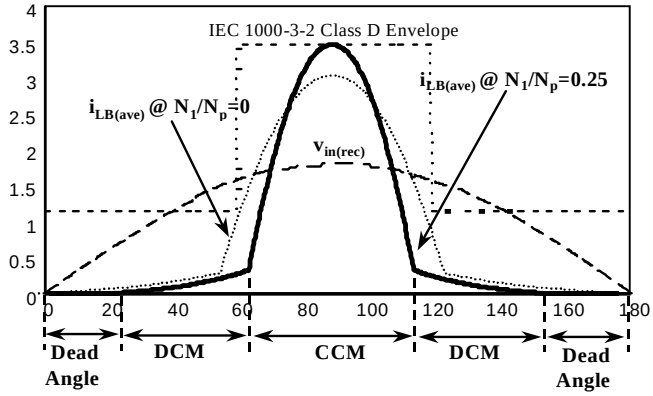

Fig. 5 Average input inductor current $i_{LB(ave)}$ of CCM S^4-PFC at V_{in} = 90 Vac with N_1/N_p=0.25.

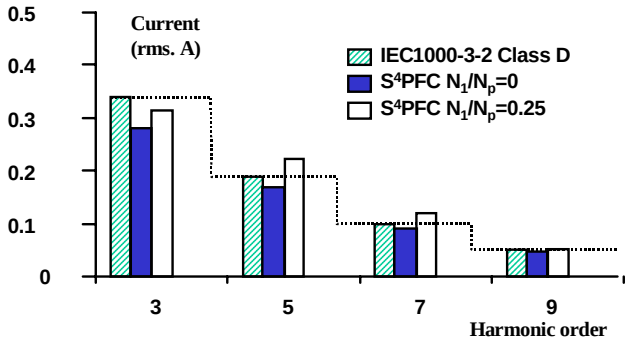

Fig. 6 Harmonic currents of CCM S^4-PFC with N_1/N_p=0 and N_1/N_p=0.25 at V_{in}=230 V_{ac}, Pin=100 W and Vo=5 V.

3. IMPROVED CCM S^4-PFC CONVERTER WITH AUXILIARY SWITCH

As can be concluded from the discussion in the previous section, the performance of the CCM S^4-PFC depends critically on the value of N_1. Specifically, to reduce the voltage stress on the energy-storage capacitor, as well as to maximize the conversion efficiency, N_1 should be maximized. However, to meet the line-current harmonic specifications with a desirable margin, N_1 should be minimized. Unfortunately, these two diametrically opposed requirements cannot be met without a major modification of the circuit.

As can be seen from Figs. 3 through 6, to reduce the line current distortion, it is necessary to increase the current around the zero crossings; *i.e.*, it is necessary to eliminate the dead angle of the current. With the dead angle eliminated, the line-current peak will be reduced and, therefore, a lower THD will be achieved. To eliminate the dead angle in the presence of an optimally selected N_1, it is necessary to modify the converter by adding an auxiliary switch as shown in Fig. 7.

3.1 Principle of Operation

In Fig. 7, switch S is the main power switch, whereas Sr is the auxiliary switch, which serves to improve the line- current waveform by eliminating the dead time of the line current. During each half line cycle when the instantaneous line voltage is around the zero crossings, Sr is turned on to disable the tapped winding N_1 and, thus, eliminate the dead angle. Figure 8(a) shows the synthesis of the timing waveform of the auxiliary switch Sr. The turn-on signal for S_r is generated by the comparator, which compares scaled, rectified-line voltage $K_V V_{in(rec)}$ with reference voltage $V_{ref.}$ When the scaled, instantaneous, rectified-line voltage is lower than the reference voltage, which occurs around the zero-crossings of the line voltage, Sr is turned on to bypass tapped winding N_1. Otherwise, auxiliary switch S_r is turned off so that winding N_1 actively participates in reducing the energy-storage-capacitor voltage and in providing the energy transfer from the input to the output for maximum efficiency.

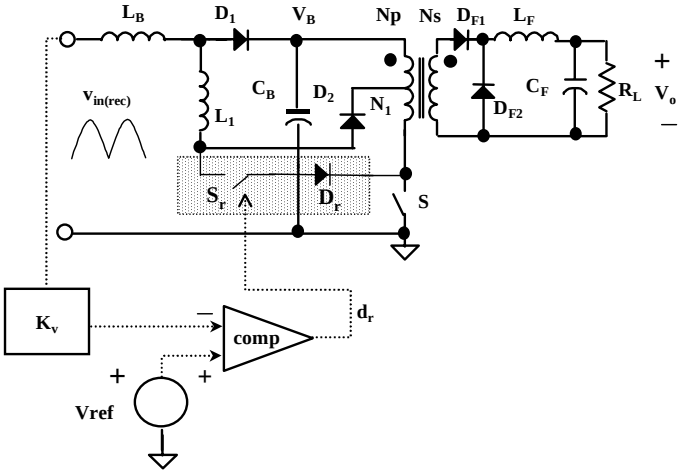

Fig. 7 Conceptual circuit diagram of improved CCM S4-PFC converter with auxiliary switch Sr.

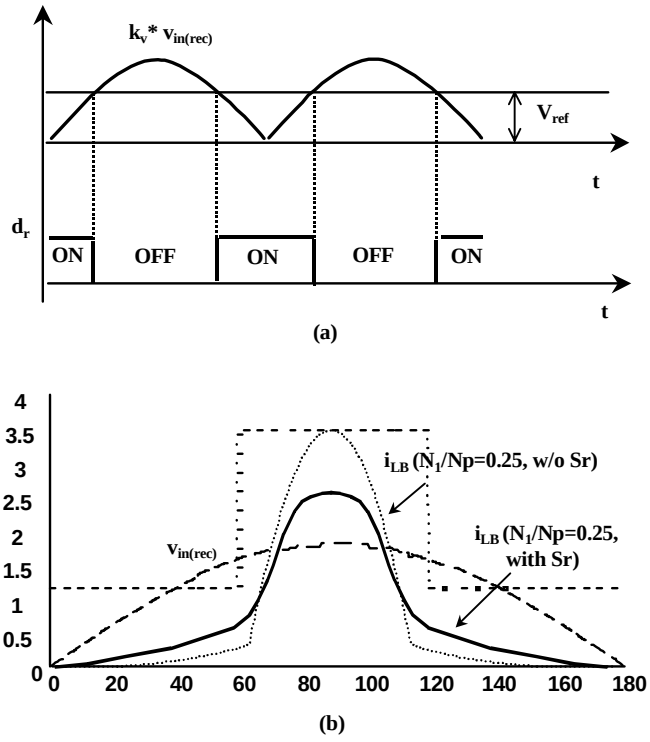

Fig. 8 Improved CCM S4-PFC converter with auxiliary switch Sr:
(a) synthesis of duty cycle d_r of auxiliary switch Sr;
(b) input current waveform with and without Sr.

The auxiliary switch Sr is a small, low-current-rated switch because it only conducts current around the zero crossings of the line voltage. In addition, S_r power dissipation is also very low because its conduction loss, as well the switching loss, is negligible since S_r carries a very small current and switches at twice of the line frequency. As shown in Fig. 7 the implementation of the control for Sr is simple, too. It requires only a comparator and a small number of passive components (resistors and capacitors) since the reference dc voltage can be derived from the energy-storage-capacitor voltage. Although, in such an implementation, the reference voltage varies with the load and line, this reference-voltage variation does not have a detrimental effect on the circuit performance. Furthermore, Sr does not require an isolated gate drive because it only needs to be turned on when S is on. Therefore, the additional cost of the proposed circuit is relatively small.

Figure 8(b) shows the average boost inductor current with and without auxiliary switch Sr. As can be seen from Fig. 8(b), with switch S_r, the current around zero crossings is increased, and the peak of the current is reduced significantly compared to the waveform of the circuit without the switch. Consequently, the line-current distortion in the implementation with the switch is reduced.

3.2. Experimental Performance Evaluation

To evaluate the effectiveness of the proposed concept, a 65-W, 100-kHz, three-output experimental converter for universal line range (90 Vac – 265 Vac) was built. The voltage and current ratings of the outputs were 5 V/9 A, 3.3 V/3 A , and 12 V / 0.9 A.

The circuit was built using the following components: L_B = 530 µH, L_1 = 250 µH, Np = 32 turns, N_1 = 8 turns (N_1/Np=0.25), Ns = 3 turns, C_B – 330 µF/450 V, S – IXTK21N100, Sr – IXYS IXTP 2N80.

Figures 9(a) and 9(b) show the measured boost-inductor current waveforms at V_{in}=230 Vac for the circuit with and without auxiliary switch Sr, respectively. Both implementations were designed with the same tapping ratio of N_1/Np = 0.25. As can be seen in Fig. 9(a), with S_r the boost-inductor current exhibits a conduction dead angle due to the tapped winding N_1, resulting in a THD of 91%. Figure 9(b) shows that auxiliary switch Sr eliminates the conduction dead angle of the boost-inductor current. In addition, with S_r the current around the zero crossing of the line voltage is increased, and the current peak is decreased, resulting in a reduced THD of 73%.

Figure 10 shows the line-current harmonic comparison at V_{in}=110 Vac for three implementations of the experimental S^4PFC: (a) without N_1 (N_1=0) and without S_r, (b) with N_1/Np=0.25 and without S_r, and (c) with N_1/Np=0.25 and S_r. The IEC 1000-3-2 harmonic current limits are also shown in Fig. 10. As can be seen from Fig. 10, at V_{in}=110 Vac all implementations meet the IEC limits with plenty of margin. However, at V_{in}=230 Vac, as shown in Fig.11, the implementation with N_1/Np=0.25 and without S_r does not meet the IEC specifications for the 5th and 7th harmonic. The implementation with N_1=0 and without S_r meets the specifications, but with a very small margin. Specifically, the margin on the 5th is less than 10% and the margin on 7th harmonic is about 5%. Finally, the proposed improved implementation with S_r and N_1/Np=0.25 meets the IEC harmonic current limits by a large margin.

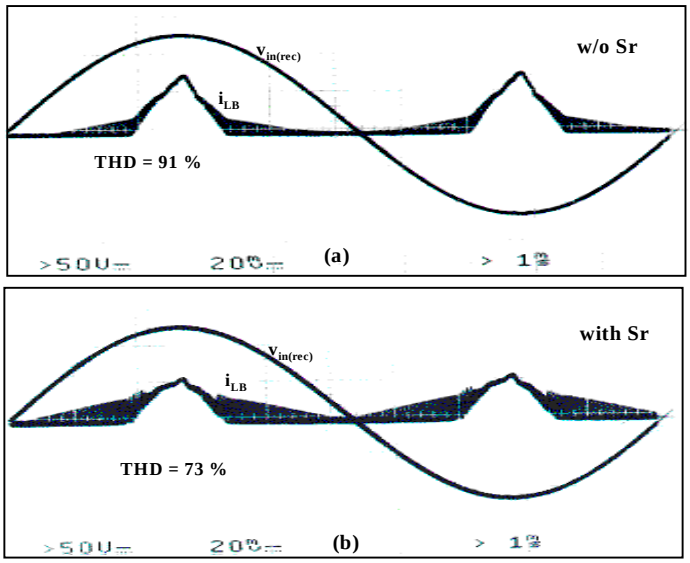

Fig. 9 Measured boost-inductor current i_{LB} at Vin = 230 Vac at full power:
(a) CCM S^4-PFC converter without Sr and N_1/N_p = 0.25;
(b) Improved CCM S4-PFC converter with Sr and N_1/N_p = 0.25.

Figure 12 shows the maximum energy-storage-capacitor voltage of the three implementations as a function of the line voltage. The proposed circuit with the auxiliary switch exhibits the lowest maximum voltage stress of 390 Vdc, which allows a safe use of a 450-Vdc rated energy-storage capacitor.

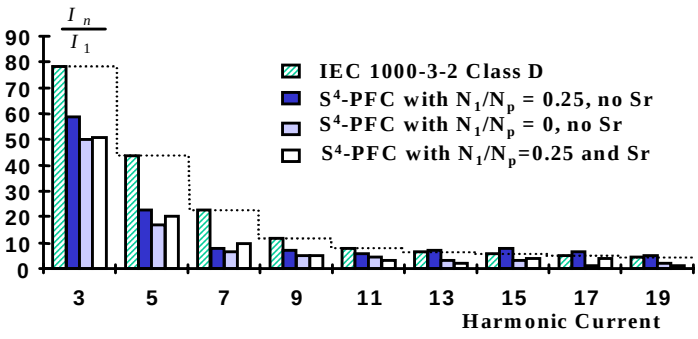

Fig. 10 Input-current harmonic comparison at Vin=110 Vac and full power.

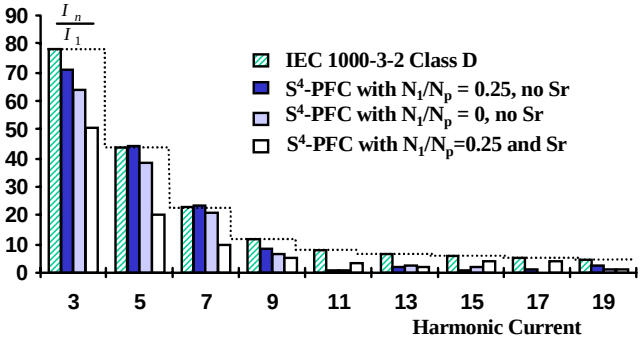

Fig. 11 Input-current harmonic comparison at Vin = 230 Vac and full power.

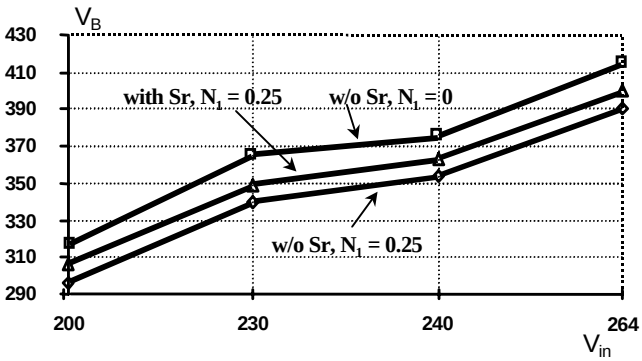

Fig. 12 Maximum energy-storage-capacitor voltage stress.

Figure 13(a) shows the measured THD, whereas Fig. 13(b) shows the measured power factor (PF) of the three circuits. As can be seen, the proposed circuit shows a significantly improved THD and PF compared with the implementations without the auxiliary switch. According to Fig. 13, the maximum improvement of the THD is more than 20%.

Figure 14 shows the efficiency comparison of the three implementations. The measured efficiency shown in Fig. 14 includes the power stage, the controller and the driver losses. As can be seen from Fig. 14, the designs with the tapped winding N_1, *i.e.*, implementations with $N_1/Np=0.25$, show no efficiency difference between the implementation with and without the auxiliary switch Sr. This implies that the loss of the additional circuitry in the proposed implementation with an auxiliary switch is negligible. At the low line, the implementations with $N_1/Np=0.25$ are approximately 1.5% more efficient than the implementation with $N_1=0$, whereas at the high line their efficiency is higher by about 0.5%. The efficiency improvement is higher at the low line because the input current is higher at the low line than it is at the high line. Therefore, the effect of the direct-energy-transfer of the feedback winding is more significant at the low line.

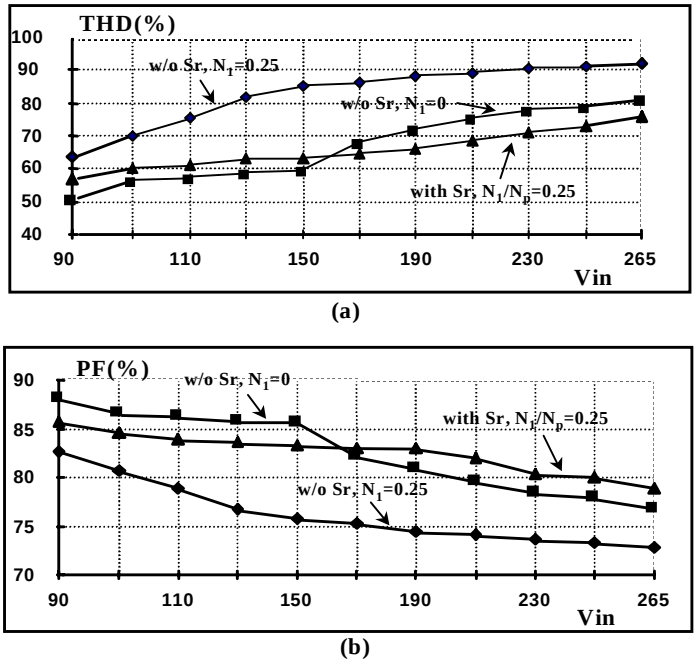

Fig. 13 Comparison of three CCM S^4-PFC implementations:
(a) THD comparison;
(b) power factor (PF) comparison.

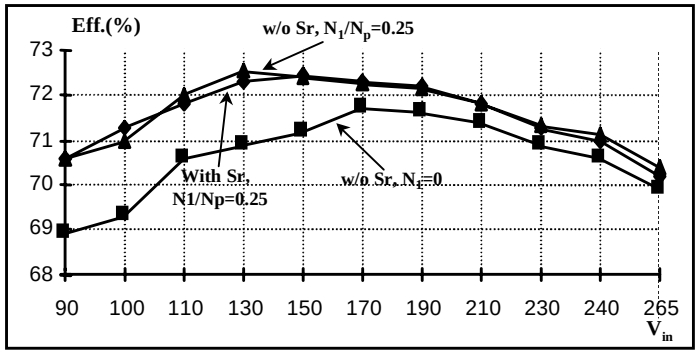

Fig. 14 Efficiency comparison of three CCM S^4-PFC implementations

In order to maximize the efficiency and decrease the energy-storage-capacitor voltage stress, N_1 should be maximized. In the original CCM S^4PFC circuit without Sr, N_1 is limited by the harmonic current constraint. However, when an auxiliary switch Sr is added in the circuit, the tapping ratio can be increased. Figure 15 shows the measured comparison of the harmonic currents of the implementations with the auxiliary switch and with $N_1/Np=0.25$ and $N_1/Np=0.37$. As can be seen from Fig. 15, the implementation with $N_1/Np=0.37$ has lower harmonic currents and, therefore, meets the IEC specifications with a higher margin than the $N_1/Np=0.25$ implementation. Figure 16 shows that the $N_1/Np=0.37$ tapping ratio also improves the efficiency over the full line-voltage range compared to the efficiency of the implementation with

N_1/Np=0.25. In addition, the maximum voltage on the energy-storage capacitor with N_1/Np=0.37 tapping is 390 V. However, it should be noted that an increased tapping ratio increases current through Sr. Therefore, the tapping ratio should be maximized so that a low current, low power, low cost auxiliary switch still can be used.

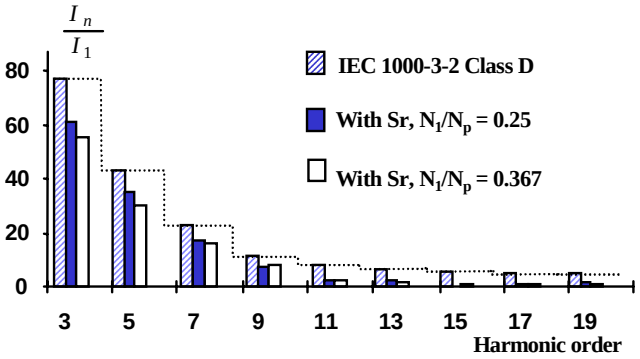

Fig. 15 Input-current harmonic comparison for implementations with different tapping ratios.

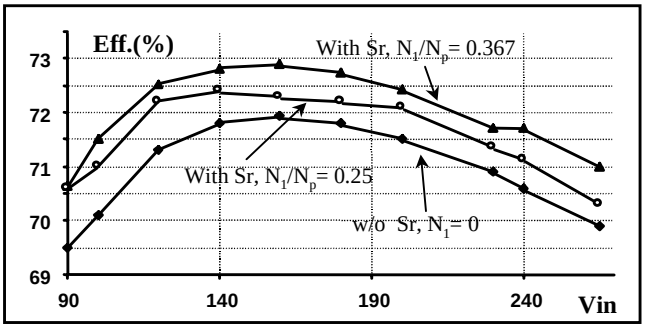

Fig. 16 Efficiency comparison.

3.3 Implementation Variations

The described concept with the auxiliary switch can be implemented in a variety of ways. For example, Fig. 17(a) shows the implementation which uses the proposed approach to disable auxiliary inductor L_1 instead of disabling winding N_1. While the disabling of L_1 increases the current in the DCM region around the zero crossings of the line voltage, this approach does not eliminate the dead angle. Consequently, the circuit in Fig. 17(a) exhibits a higher line-current THD than the proposed circuit in Fig. 7. Yet another implementation of the proposed concept is shown in Fig. 17 (b). In this implementation, both L_1 and N_1 are disabled around the zero crossings of the line voltage. This approach eliminates the dead angle completely and increases the line current in the DCM regions even more than the circuit in Fig. 7. As a result, the circuit in Fig. 17(b) has a lower THD than the THD in the circuit in Fig. 7. However, the circuit in Fig. 17(b) has a higher energy-storage-capacitor voltage stress than the original circuit in Fig. 7 because auxiliary inductor L_1, which helps in reducing the capacitor voltage, is disconnected from the circuit for a portion of the rectified-line period.

Another low-cost approach to improve the input current at high line is to replace the semiconductor switch Sr in Fig. 7 with an electro-mechanical switch (relay) or mechanical switch. In this implementation, the switch is permanently turned on at the low-line range and permanently turned off at the high-line range to eliminate the dead conduction angle at high line. While this approach reduces the line-current harmonics as effectively as the circuit in Fig. 7, it has a higher voltage stress on the energy-storage capacitor and lower efficiency because at high line winding N_1 is disabled permanently.

Finally, the proposed PFC concept can be extended to other DCM/CCM S^4PFC converter topologies. For example, Fig. 18 shows the implementation of the proposed concept in the DCM S^4PFC converter.

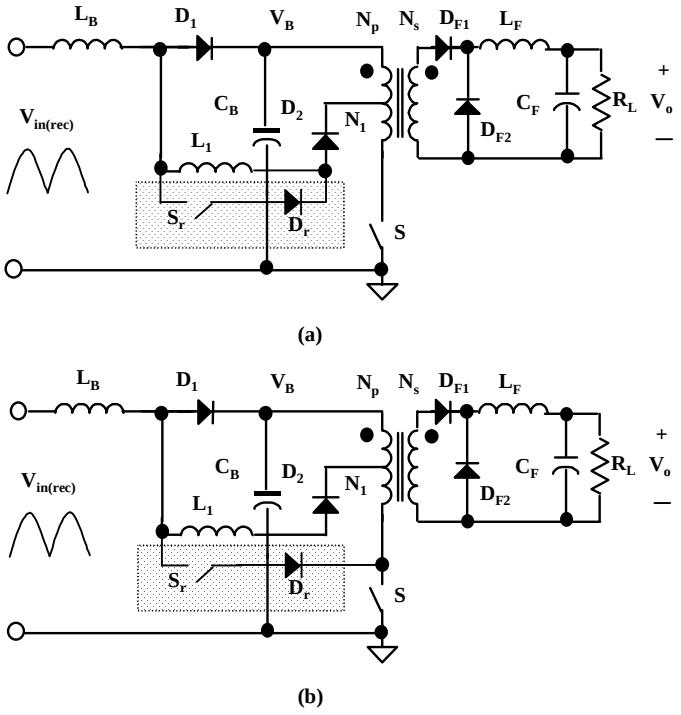

Fig. 17 Implementation variations:
(a) Disabling of L_1;
(b) Disabling of L_1 and N_1.

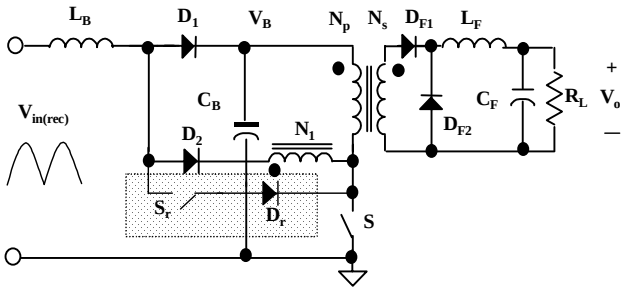

Fig. 18 DCM S^4-PFC with auxiliary switch Sr.

4. SUMMARY

An improved, cost-effective, single-stage PFC technique which employs an auxiliary switch is presented. The proposed technique improves the input power factor, reduces the stress on the energy-storage capacitor, and improves the overall efficiency. The performance of the proposed technique was verified experimentally on a 65-W, universal-line range, three-output converter.

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