Analysis, Design, and Evaluation of Forward Converter with Distributed Magnetics -- Interleaving and Transformer Paralleling*

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Abstract - Analysis, design, and evaluation of different interleaving techniques for the forward converter with distributed magnetics are presented. Specifically, the one-choke interleaving approach is compared with the two-choke interleaving approach. The results of the analysis are verified on two 5 V/20 A, interleaved dc/dc converters. In addition, different methods of achieving and maintaining the desirable current sharing of directly paralleled transformers in a forward converter are described and verified experimentally.

1. INTRODUCTION

Paralleling of converter power stages is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors. In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result, paralleling is a popular approach to eliminating "hot spots" in power supplies. In addition, the switching frequencies of paralleled, lower-power power stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because lower-power, faster semiconductor switches can be used in implementing the paralleled power stages. Consequently, paralleling offers an opportunity to reduce the size of the magnetic components.

In its basic form, the interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted over a switching period [1]. By introducing an equal phase shift between the paralleled power stages, the total inductor current ripple of the power stage seen by the output filter capacitor is lowered due to the ripple cancellation effect [1]. As a result, the size of the output filter capacitance can be minimized. Since the effect of interleaving is to increase the effective ripple frequency of the filter, the interleaving technique in topologies with inductive output filter can be implemented in two ways. The basic interleaving approach is to directly parallel the outputs of the individual power stages so that they share a common output filter capacitor [2]. The alternative approach is to parallel the power stages at the input of a common LC output filter. The former approach distributes the transformer and output filter magnetics, while the latter approach distributes only the transformer magnetics [2,3].

Due to its distributed-magnetics structure and minimum-size output filter, the interleaving approach is especially attractive in high-power applications that call for high power-density and low-profile packaging, for example, distributed power modules (both front-end and load converters). However, the increased number of power-stage and control-circuit components in an interleaved converter may also present an obstacle to achieving high packaging densities. The transformer magnetics can be distributed without increasing the number of power-stage and control-circuit components by resorting to direct paralleling of power transformers. However, the transformer paralleling is only viable if the current sharing between paralleled transformers can be maintained.

In this paper, the analysis, design, and evaluation of one-choke and two-choke approaches to interleaving of two forward converters are presented. The results of the analysis are verified on two 5 V/20 A interleaved forward converters. Also, a number of methods to achieve and maintain good current sharing of directly paralleled transformers are described and evaluated experimentally.

2. INTERLEAVED FORWARD CONVERTER

2.1 Two-Choke Approach

Two interleaved forward converters that utilize two complete forward converter modules (two-choke approach), are shown in Fig. 1. The two modules operate independently

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in anti-phase with duty cycles less than 50%. The current-sharing among the modules is ensured by employing the current-mode control. In the implementation in Fig. 1, reset of the transformers is achieved by the resonance between the magnetizing inductance of the transformers and the output capacitance of the MOSFETs (including external capacitance). The R-C-D networks only provide over-voltage protection for primary switches. The operation principle is identical to that of the standard resonant-reset forward converter [4], whose key waveforms are shown in Fig. 2.

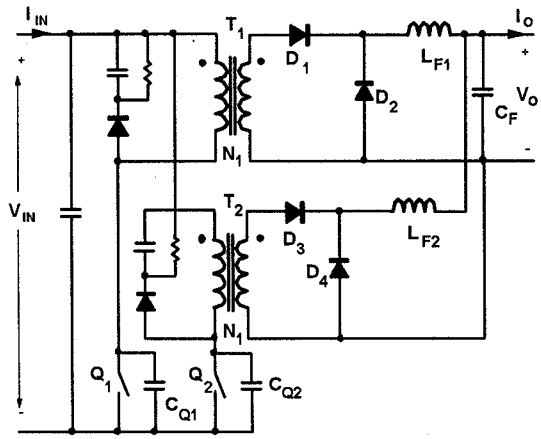


Fig. 1 Two-choke interleaved forward converter.

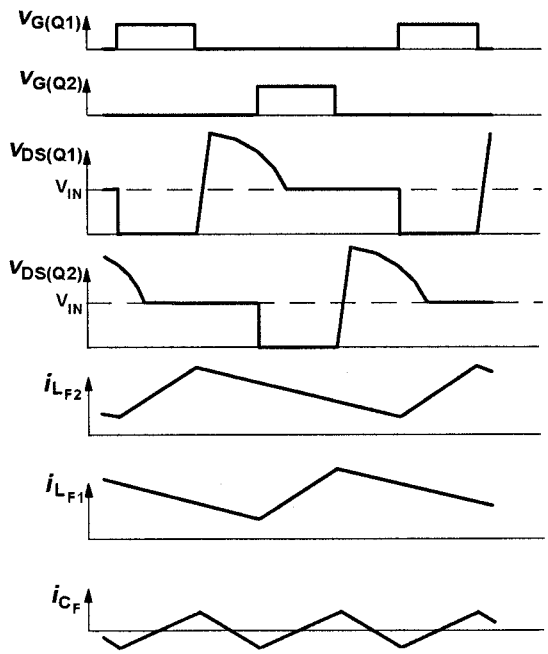


Fig. 2 Key waveforms of two-choke interleaved forward converter.

As can be seen from Fig. 2, interleaving reduces the ripple current through the common output filter capacitor.

2.2 One-Choke Approach

The one-choke approach, shown in Fig. 3, uses only one output inductor for the purpose of saving a magnetic component. Its operation principle is quite different from that of the two-choke interleaved converter.

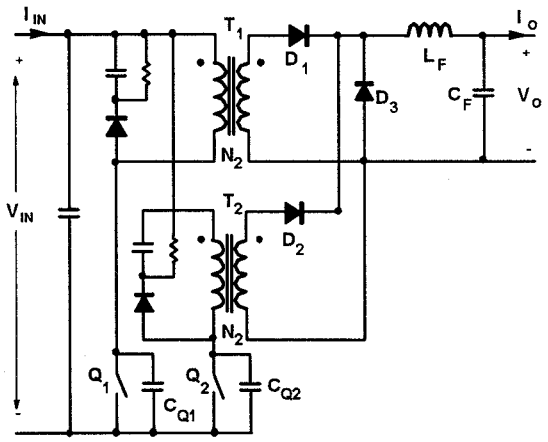


Fig. 3 One-choke interleaved forward converter.

Because in the one-choke interleaved forward converter, the two modules share the same freewheeling diode D_3 and output filter, these two modules do not work independently. The key waveforms of the one-choke interleaved converter are shown in Fig. 4.

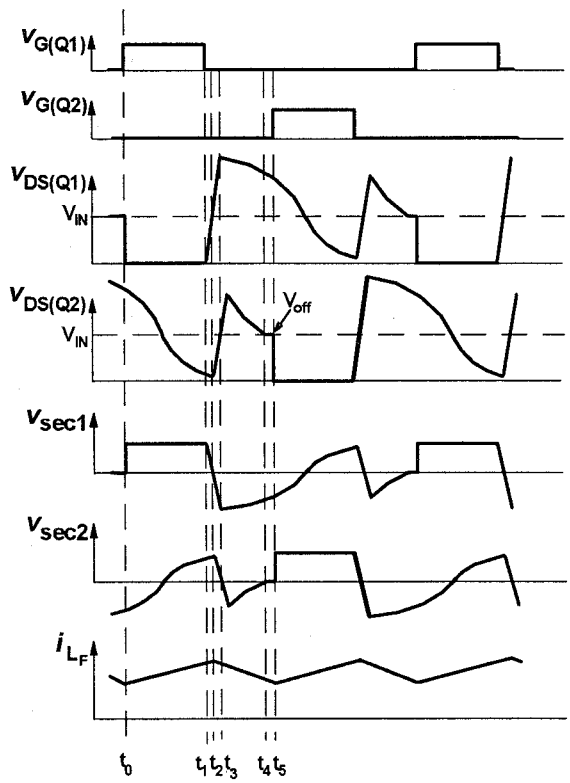


Fig. 4 Key waveforms of one-choke interleaved forward converter.

For the simplicity of the analysis of the operation principles, the output inductor, L_F, is assumed to be large enough for the output to be considered as a current source, I_o. In stead-state, the topological stages are shown in Figs. 5(a)-5(e).

(a)$t_0 - t_1$: Switch Q_1 turns on at t_0 and diode D_1 conducts. Diode D_3 is reverse biased at the voltage $\frac{V_{IN}}{N_2}$, which also blocks diode D_2. Due to the anti-phase operation, transformer T_2 is in the reset period. In the conventional resonant-reset forward converter operation, the drain-to-source voltage of the primary switch $V_{DS(Q)}$ never goes below input voltage V_{IN} because of the clamping action of the forward diode [5]. In the one-choke interleaved converter, diode D_2 is reverse biased at $\frac{V_{IN}}{N_2}$ and this clamping action is not present. Therefore, the reset process continues after $V_{DS(Q2)}$ reaches V_{IN}, i.e., $V_{DS(Q2)}$ becomes smaller than V_{IN}. This stage lasts until Q_1 turns off at t_1, with $V_{DS(Q2)} < V_{IN}$.

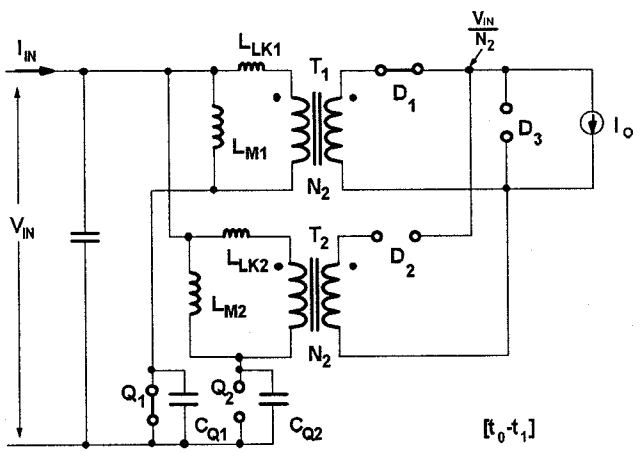


Fig. 5(a) Topological stage (a).

(b)$t_1 - t_2$: Q_1 turns off at t_1. The output capacitor of Q_1, C_{Q1}, is linearly charged by the reflected output inductor current, $\frac{I_o}{N_2}$. Transformer T_2 is still in the resonant-reset phase and $V_{DS(Q2)}$ continues to drop below V_{IN}. This interval lasts until t_2, when $V_{DS(Q1)}$ ramps up to V_{IN}. The forward diode D_1 is turned off and the freewheeling diode D_3 starts to conduct.

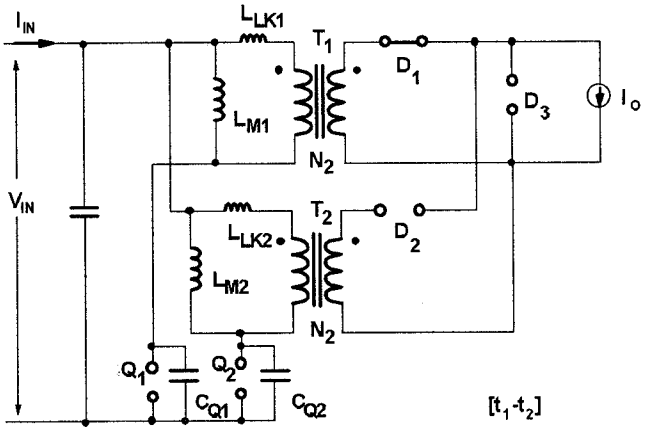


Fig. 5(b) Topological stage (b).

(c)$t_2 - t_3$: The output current, I_o, freewheels through diode D_3. Since $V_{DS(Q2)} < V_{IN}$, diode D_2 is forced to conduct and transformer T_2 is shorted. Resonance formed by L_{LK2} and C_{Q2} charges C_{Q2} and increases voltage $V_{DS(Q2)}$. At the same time, the energy stored in the leakage inductance L_{LK1} charges C_{Q1} at a very fast rate. Diode D_2 turns off at t_3, when the current in L_{LK2} goes to zero and $V_{DS(Q?)}$ is above V_{IN}.

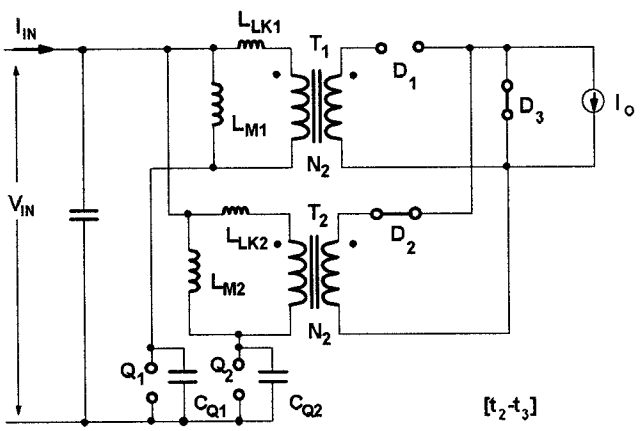


Fig. 5(c) Topological stage (c).

(d)$t_3 - t_4$: Transformer T_1 is reset through the resonance formed by the output capacitor C_{Q1} and the magnetizing inductance L_{M1}. The magnetizing inductance L_{M2} discharges the output capacitance C_{Q2} and $V_{DS(Q2)}$ drops in a resonant fashion. This interval ends at t_4, when $V_{DS(Q2)}$ reaches the input voltage V_{IN}.

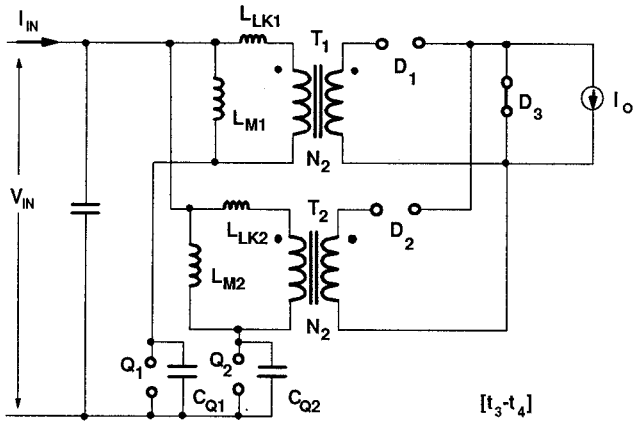


Fig. 5(d) Topological stage (d).

(e) $t_4 - t_5$: $V_{DS(Q2)}$ stays at V_{IN} and the magnetizing current of L_{M2} remains constant by flowing through diode D_2. This stage lasts until t_5, when Q_2 turns on.

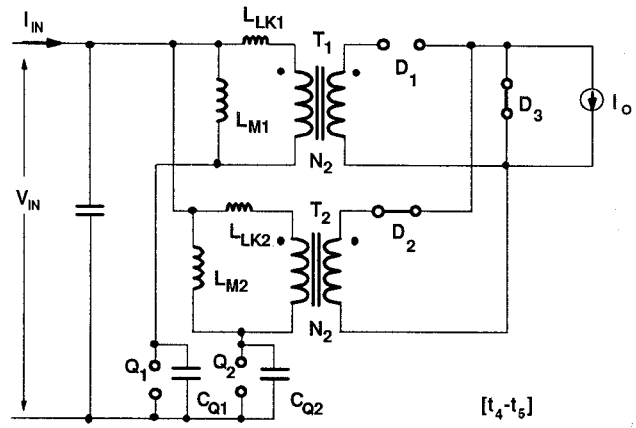


Fig. 5(e) Topological stage (e).

For the other half of the switching cycle, the devices in the two modules exchange the roles.

From the above analysis and waveforms, it can be clearly seen that during on-time, the entire output current flows through one of the modules instead of sharing current in two modules. Also the transformer flux excitation is different: two positive volt-secs exist in one switching cycle, which cause a small additional B-H loop.

The effective duty cycle on the secondary side is doubled due to the sharing of the freewheeling diode and the output filter. This provides the advantage of implementing higher turns-ratio for the transformers (twice as high as that of the two-choke interleaved converter).

2.3 Loss Analysis

In the two-choke approach, the conduction loss of the transformers and the primary switches is:

$$2[(\frac{I_o}{2})^2 R_1 + (\frac{I_o}{2N_1})^2 R_{DS(on)}]D. \qquad (1)$$

where I_o is the output current, R_1 and N_1 are the transformer winding resistance and turns-ratio, and $R_{DS(on)}$ is the on-resistance of the primary switches.

In the one-choke approach, because the output current flows through only one module during on-time, the conduction loss is:

$$2[I_o^2 R_2 + (\frac{I_o}{N_2})^2 R_{DS(on)}]D. \qquad (2)$$

Since the two converters have the same duty cycles, $N_2 = 2N_1$, the primary switch conduction loss is the same. The conduction loss differences in forward diodes and output inductors are negligible. Core loss of the transformers in the one-choke approach is slightly higher due to the small additional B-H loop.

The turn-on loss of the MOSFETs is:

$$2(\frac{1}{2} C_Q V_{off}^2) f_s \qquad (3)$$

where V_{off} is the drain-to-source voltage of the MOSFETs at the end of the off-period. In the one-choke converter, V_{off} is usually the capacitor voltage during resonance of L_{LK} and C_Q (stage (c)). V_{off} changes as V_{IN} changes because different off-period determines different voltage swing level. Thus the turn-on loss varies as input voltage, so does the power-stage efficiency. While in the two-choke converter, V_{off} is always clamped at V_{IN} after reset period.

Therefore, the turn-on switching loss in the one-choke converter is generally higher than that in the two-choke converter and the resulting efficiency is lower.

3. TRANSFORMER PARALLELING

Generally, the interleaving technique requires an increased number of components in the power stage. However, if the interleaving approach is used solely to distribute magnetics, i.e., to use simpler, low-power, low-profile transformers instead of one bulky transformer, then transformer paralleling is the approach that requires the smallest number of power stage components.

3.1 Direct Paralleling

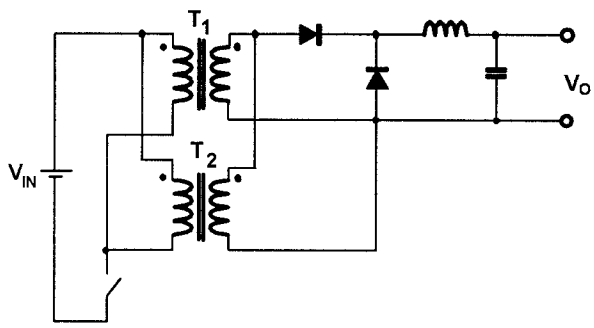


Fig. 6 Direct transformer paralleling.

In Fig. 6, T_1 and T_2 are two low-profile transformers connected directly in parallel and have the same secondary circuitry. For proper operation of the circuit, the transformers need to share the output current. The equivalent circuit of the two transformers in parallel is shown in Fig. 7.

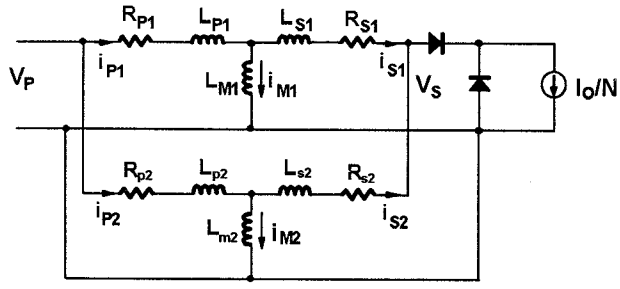


Fig. 7 Equivalent circuit of direct transformer paralleling.

R_p, L_p and L_m are primary winding resistance, leakage inductance, and magnetizing inductance of the transformers, respectively. L_s and R_s are secondary leakage inductance and winding resistance reflected to the primary side. In steady state, $\frac{di}{dt}=0$; assuming $i_{m1}=i_{m2}=0$, it can be shown that:

$$\frac{i_{s1}}{i_{s2}}=\frac{R_{p2}+R_{s2}}{R_{p1}+R_{s1}}. \qquad (4)$$

The current sharing depends on the parasitics of the transformers. This approach works only with well-matched transformers. The transformer parasitic resistance is usually comparable with trace resistance. At the connecting ends of the transformers, the trace layout of the transformer connection should be symmetrical to introduce balanced trace resistance.

3.2 Paralleling With Separate Forward Diodes

A modification can be made by using separate forward diodes to reduce the parasitic effect, as shown in Fig. 8.

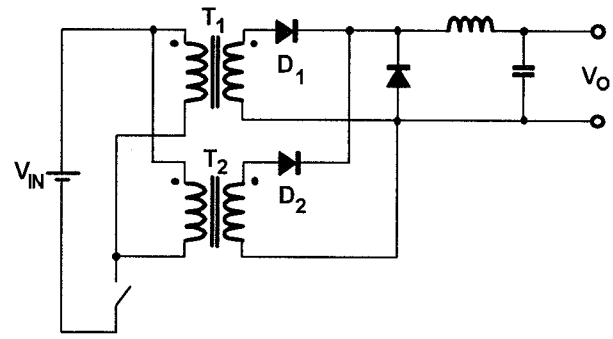


Fig. 8 Transformer paralleling using separate forward diodes.

Then the current sharing is governed by:

$$\frac{i_{s1}}{i_{s2}}=\frac{R_{p2}+R_{s2}+R_{D2}}{R_{p1}+R_{s1}+R_{D1}}\approx\frac{R_{D2}}{R_{D1}}. \qquad (5)$$

Thus, current sharing depends on the diode on-resistance instead of the parasitics. Since the diode on-resistance is more uniform, this is a better solution for current sharing.

3.3 Paralleling With Common Heat Sink

On-resistance of diodes has negative temperature coefficient, i.e., on-resistance decreases as temperature rises. This results in a potential problem for current sharing: if one diode starts with higher current due to a slight mismatch between the diode on-resistance, its on-resistance will get smaller because of higher temperature by larger power dissipation. This makes the heated diode draw even more current by Eq. (5). In this runaway scenario, all the current will end up flowing through single diode and transformer.

Using the positive temperature coefficient characteristic of MOSFET on-resistance, replacing the diodes with synchronous rectifier [6] can solve the thermal runaway problem. Synchronous rectifiers always exhibit good current sharing; thus no current hogging is possible. However, the complexity of the circuit increases, which contradicts the simplicity of transformer paralleling.

The simplest solution is to use a common heat sink for the two forward diodes. This forces the temperature of the diodes to be the same, and furthermore enforces the same on-resistance to ensure current sharing.

4. EXPERIMENTAL EVALUATIONS

Evaluations of the discussed one-choke and two-choke interleaved forward converters were performed on 300 kHz, 5 V/40 A power stages designed to operate in the 40-60 Vdc input voltage range. The power stage with two chokes, shown in Fig. 1, consists of the following components:

Q_1, Q_2 - IRF640 (International Rectifier);
$D_1 - D_4$ - 82CNQ30 (International Rectifier);
T_1, T_2 - core: TDK PC30LP23/8Z-12;
primary: 9 turns of 4 stands of #26 wire;
secondary: 3 turns of 3 mils Cu foil;
$L_M = 108\mu H$, $L_{LK} = 200nH$ on primary-side;
$R = 6.7m\Omega$ on secondary-side;
C_{Q1}, C_{Q2} - $1nH$ ceramic;
L_{F1}, L_{F2} - inductance: $10.5\mu H$;
core: Magnetics MPP55304;
winding: 10 turns of 2 stands of #17 wire;
C_F - $4400\mu F$ electrolytic.

The power stage with one-choke, shown in Fig. 3, consists of the following components:

Q_1, Q_2 - IRF640 (International Rectifier);
$D_1 - D_3$ - 82CNQ30 (International Rectifier);
T_1, T_2 - core: TDK PC30LP23/8Z-12;
primary: 12 turns of 3 stands of #26 wire;
secondary: 2 turns of 3 mils Cu foil;
$L_M = 214\mu H$, $L_{LK} = 325nH$ on primary-side;
$R = 3.4m\Omega$ on secondary-side;
C_{Q1}, C_{Q2} - $3.3nH$ ceramic;
L_{F1}, L_{F2} - inductance: $3.85\mu H$;
core: Magnetics Kool $M\mu^{TR}$ 77310;
winding: 4 turns of 5 stands of #17 wire;
C_F - $4400\mu F$ electrolytic.

The higher turns of the transformer primary winding in the one-choke approach give higher leakage inductance L_{LK}. In order to sustain the reset voltage, external capacitance C_Q is correspondingly increased.

Figures 9 and 10 show the experimental waveforms of the interleaved forward converters with one and two chokes, respectively. By comparing the two figures, the difference of operations can be seen clearly. Also in the one-choke converter, the resonance amplitude is affected by the output current level. This is because heavy load current causes higher energy stored in L_M and L_{LK}, and consequently higher amplitude resonance, as illustrated in the comparison of case (a) and case (b) in Fig. 10.

The result of different operation principles is reflected in the power-stage efficiency measurement, illustrated in Fig. 11. It can be seen that the efficiency of the one-choke interleaved forward is lower than that of the two-choke interleaved forward converter. The reasons of lower efficiency in the one-choke approach are: higher conduction loss in the transformers and higher capacitive turn-on switching loss in the primary switches.

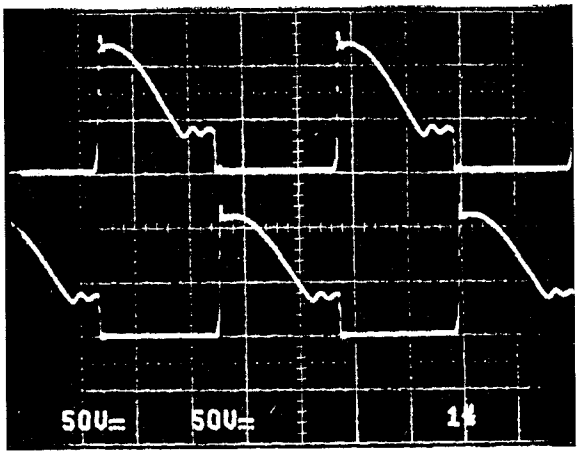
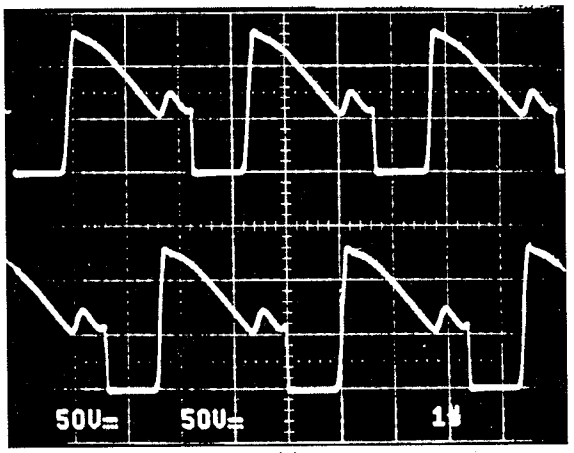
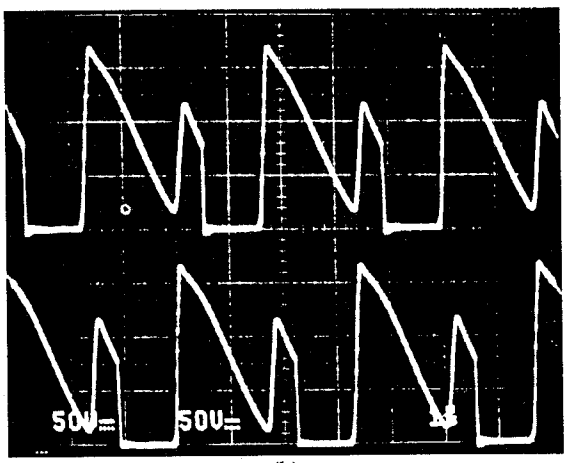


Fig. 9 Experimental waveforms of $V_{DS(Q1)}$ and $V_{DS(Q2)}$ in the two-choke approach.



(a)



(b)

Fig. 10 Experimental waveforms of $V_{DS(Q1)}$ and $V_{DS(Q2)}$ in the one-choke approach:
(a) light load ($I_o = 20A$)
(b) heavy load ($I_o = 40A$).

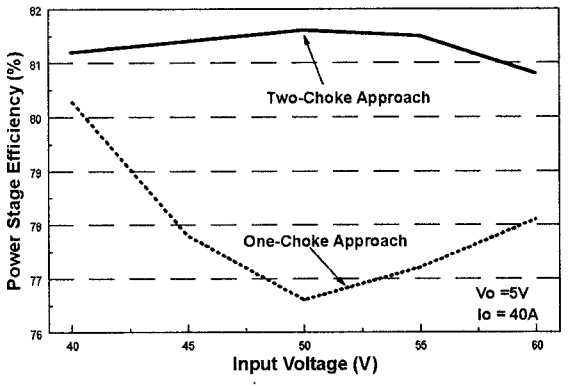


Fig. 11 Measured efficiencies of the one-choke and two-choke converters.

At the nominal line ($V_{IN}=50\ V$, $D=30\%$), the conduction loss increase in the one-choke approach, from Eqs. (1) and (2), is:

$$\Delta P_C = 2\cdot(40^2\cdot 0.0034)\cdot 30\% - 2\cdot(20^2\cdot 0.0067)\cdot 30\% = 1.7\ W \quad (6)$$

For the switching loss in the one-choke converter, The measured V_{off} increases from $50\ V$ at low line and reaches $125\ V$ at $V_{IN}=50\ V$. Then V_{off} drops to $100\ V$ at high line. From Eq. (3), this corresponds to that the switching loss increases from 2.5 W at low line to 15.5 W at nominal line, and then drops to 9.9 W at high line. This explains the measured efficiency curvature for the one-choke converter. Compared with the two-choke converter, the switching loss increase at the nominal line is:

$$\Delta P_C = 2\cdot(\frac{1}{2}3.3n\cdot 125^2)\cdot 300k - 2\cdot(\frac{1}{2}\cdot 1n\cdot 50^2)\cdot 300k = 14.7\ W \quad (7)$$

Thus the total power consumption increase is about 16 W, which fits well with the measured efficiency drop from 81.5% to 76.6% at $V_{IN}=50\ V$ (a power dissipation increase of 15.5 W).

Table 1 Current sharing measurements.

Measurement Setup	Current Sharing
Single forward diode and symmetrical trace layout	1:1.3
Single forward diode and asymmetrical trace layout	1:2
Separate forward diodes and separate heat sinks	1:1.2
Separate forward diodes and common heat sink	1:1.1

Table 1 shows the current sharing measurements of the discussed transformer paralleling with different transformer connections and heat sink configurations. It can be seen that using separate forward diodes with common heat sink results in the best current sharing.

5. CONCLUSIONS

For interleaved forward converters, the two-choke approach is better than the one-choke approach in terms of efficiency and power management. Distributed magnetic can be utilized to design high-power, low-profile converters by using a number of low-power, low-profile transformers. For good current sharing, the resistance of the transformers (including trace resistance) should be matched. Using a common heat sink and/or synchronous rectifiers can ensure good current sharing.

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