

# A TECHNIQUE FOR REDUCING RECTIFIER REVERSE-RECOVERY-RELATED LOSSES IN HIGH-VOLTAGE, HIGH-POWER BOOST CONVERTERS

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**Abstract** – A circuit technique that reduces the boost-converter losses caused by the reverse-recovery characteristics of the rectifier is described. The losses are reduced by inserting an inductor in the series path of the boost switch and the rectifier to control the  $di/dt$  rate of the rectifier during its turn-off. The energy from the inductor after the boost switch turn-off is returned to the input or delivered to the output via an active snubber. The same technique can be extended to any member of the PWM-converter family.

## I. Introduction

In recent years, significant research and development efforts have been made to come up with a cost-effective soft-switching technique to improve the performance of the boost converter. The main reason for such a keen interest in the boost topology stems from the fact that the continuous-conduction-mode (CCM) boost converter is the preferred topology for implementing the front-end converter for active input-current shaping at higher power levels.

When the boost converter is used as an input-current shaper, its input is the rectified mains voltage, which, depending on applications, can be in the 90 Vac to 480 Vac range. Since the dc-output voltage of the boost converter must be higher than the peak input voltage, the output voltage of the boost input-current shaper is generally high. Due to the high output voltage, the converter requires the use of a fast-recovery boost rectifier. At high switching frequencies, fast-recovery rectifiers produce significant reverse-recovery-related losses when switched under “hard-switching” conditions [1]. As a result, “hard-switched” boost input-current shapers need to be operated at relatively low switching frequencies to avoid a significant deterioration of their conversion

efficiencies. Employing a soft-switching technique, the switching frequency and, therefore, the power-density of the boost, front-end converter can be increased.

So far, a number of soft-switched boost converters and their variations have been proposed [2] - [5]. All of them employ an auxiliary active switch with a few passive components (inductors and capacitors) to form an active snubber [6] that is used to control the  $di/dt$  rate of the rectifier current and to create conditions for zero-voltage switching (ZVS) of the main switch and the rectifier.

The boost converter circuits proposed in [2] and [3], use a snubber inductor connected to the common node of the boost active switch and the rectifier to control the rectifier  $di/dt$ . As a result of the snubber inductor location, the main switch and rectifier in the circuits proposed in [2] and [3] possess the minimum voltage and current stresses. In addition, the boost switch turns on and the rectifier turns off under zero-voltage (soft-switching) conditions. However, the auxiliary switch is turned on while its voltage is equal to the output voltage, and subsequently turned off while carrying a current greater than the input current. As a result of the auxiliary switch “hard” turn-on and turn-off, it dissipates more power than it would if it were switched under soft-switching conditions. Nevertheless, the power dissipation of the auxiliary switch in a properly designed converter is much smaller than that of the main switch because the auxiliary switch conducts only during switching transitions. The major drawback of the boost converter in [2] and [3] is caused by the undesirable resonance of output capacitance of the auxiliary switch  $C_{oss}$  and the snubber inductor, which occurs when the auxiliary switch is open and after the current in the snubber inductor falls to zero. This parasitic resonance generates an undesirable current through the snubber inductor which increases the conduction losses and upsets the normal operation of the circuit. To reduce the effect of this resonance, it is necessary to add a rectifier and a

saturable inductor in series with the snubber inductor [3], which increases the component count and cost of the circuit.

In the circuits introduced in [4] and [5] the  $di/dt$  rate of the rectifier current is controlled by a snubber inductor connected in series with the boost switch and the rectifier. Because of this placement of the inductor, the voltage stress of the main switch is higher than that of the circuits described in [2] and [3]. This increased voltage stress can be controlled by the size of clamp capacitor  $C_C$ . A larger  $C_C$  results in a reduced stress. Both the boost and auxiliary switches in the circuits in [4] and [5] operate under ZVS conditions. However, to achieve ZVS of the boost switch with the implementation in [4], a significant energy needs to be circulated in the resonant circuit consisting of the snubber inductor and clamp capacitor  $C_C$ . This circulating energy also increases the current stress of the rectifier. The implementation in [5] does not circulate the energy, but the boost rectifier in this circuit suffers from an increased voltage stress caused by the parasitic resonance between the junction capacitance of the rectifier and the snubber inductor used to control its  $di/dt$  rate. As reported in [5], even with a heavy RCD snubber across the rectifier, the voltage stress of the rectifier is more than 600 V for a converter with a 400-V output. As a result, the implementation in [5] requires a rectifier with a higher voltage rating, which has a detrimental effect on the conversion efficiency and cost.

The technique described in this paper reduces the reverse-recovery related losses of the boost rectifier by controlling the  $di/dt$  rate of the rectifier current with a snubber inductor connected in series with the boost switch and rectifier in the same way as in [4] and [5]. The series connection of the auxiliary switch and the clamp capacitor, which is used to provide the discharging path of the snubber inductor current (energy) when the main switch is turned off, can be connected to any dc point such as output, input, or ground. The connection to the converter input or output requires an n-type MOSFET, while the ground connection needs to be implemented with a p-type MOSFET. The parasitic ringings caused by the interaction of the junction capacitance of the rectifier and the snubber inductor used to control its  $di/dt$  rate are eliminated by a clamp diode connected between the anode of the boost rectifier and ground. As a result, the voltage stress on the rectifier in the proposed technique is limited to the output voltage. Finally, this technique can be extended to any other non-isolated or isolated converter topology.

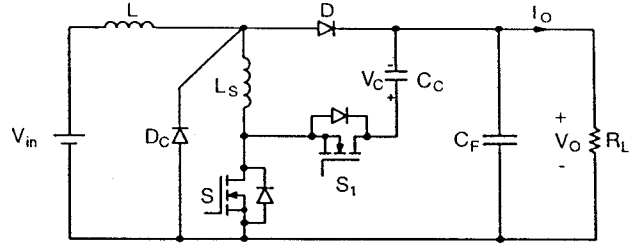


Fig. 1: Proposed boost power stage.

## II. Principle of Operation

The circuit diagram of the boost converter which employs the new technique for reverse-recovery-loss reduction is shown in Fig. 1. The circuit in Fig. 1 uses n-type-MOSFET auxiliary switch S1 and clamp capacitor  $C_C$  connected in series to discharge the energy stored in snubber inductor  $L_S$  to the output after S1 is turned off. Diode  $D_C$  is employed to eliminate the parasitic ringings between the junction capacitance of D and inductor  $L_S$  by clamping the anode of D to ground.

To simplify the analysis of operation, it is assumed that the inductance of boost inductor L is large so that it can be represented by constant-current source  $I_{in}$ , and that the output-ripple voltage is negligible so that the voltage across the output filter capacitor can be represented by constant-voltage source  $V_O$ . The circuit diagram of the simplified converter is shown in Fig. 2. In addition, it is assumed that in the on-state, semiconductors exhibit zero resistances, *i.e.*, they are short circuits. However, the output capacitances of the MOSFETs and the reverse-recovery charge of the rectifier are not neglected in this analysis. To further facilitate the explanation of operation, Fig. 3 shows topological stages of the circuit in Fig. 2 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms. It should be noted that because the junction capacitance of boost rectifier D has been neglected for the time being, clamp diode  $D_C$  is not shown in Fig. 3 since it never conducts.

As can be seen from the timing diagrams for the boost and auxiliary switches in Fig. 4, the switches never conduct simultaneously. In fact, the proper operation of the power stage requires appropriate dead times between the turn-off of boost switch S and turn-on of auxiliary switch S1, and vice versa.

Before boost switch S is turned off at  $t = T_O$ , the entire input current  $I_{in}$  flows through inductor  $L_S$  and switch S. At the same time, rectifier D is off with a reverse voltage across its terminals equal to output voltage  $V_O$ . Auxiliary switch S1 is also off, blocking the voltage  $V_O + V_C$ , where  $V_C$  is the voltage across the clamp

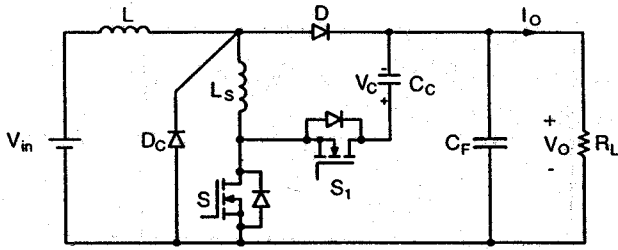


Fig. 2: Simplified circuit diagram of boost power stage showing reference directions of currents and voltages.

capacitor.

After switch S is turned off at  $t = T_0$ , the current which was flowing through the channel of the MOSFET is diverted to the output capacitance of the switch,  $C_{oss}$ , as shown in Fig. 3(a). As a result, the voltage across switch S starts linearly increasing due to the constant charging current  $I_{in}$ . During this stage, auxiliary-switch voltage  $v_{S1}$  decreases from  $V_O + V_C$  towards zero, while boost-switch voltage  $v_S$  increases from zero towards  $V_O + V_C$  (Fig. 4). When voltage across switch S reaches  $V_o$ , rectifier D starts conducting, and the current through inductor  $L_S$  starts decreasing due to a negative voltage across its terminals, as shown in Fig. 4. This topological stage ends at  $t = T_1$ , when voltage  $v_S$  reaches  $V_O + V_C$ , and the antiparallel diode of switch S1 starts conducting. At that moment, the remaining inductor current  $i_L$  is diverted into clamp capacitor  $C_C$ , and switch voltage  $v_S$  is clamped to  $V_O + V_C$ , as shown in Fig. 3(b).

During the topological stage shown in Fig. 3(b), inductor current  $i_L$  continues to decrease as it discharges to clamp capacitor  $C_C$  (Fig. 4). If the capacitance of  $C_C$  is large, capacitor voltage  $v_C$  is almost constant, and inductor current  $i_L$  decreases linearly. Otherwise,  $i_L$  decreases in a resonant fashion. As  $i_L$  decreases, rectifier current  $i_D$  increases at the same rate because the sum of  $i_L + i_D$  is equal to constant input current  $I_{in}$ . This topological stage ends at  $t = T_3$ , when  $i_L$  reaches zero and the antiparallel diode of auxiliary switch S1 stops conducting. To achieve ZVS of S1, it is necessary to turn on the transistor of switch S1 before  $t = T_3$ , i.e., while its antiparallel diode is conducting. In Fig. 4, the MOSFET of switch S1 is turned on at  $t = T_2$ .

If the transistor of switch S1 is turned on prior to  $t = T_3$ , inductor current  $i_L$  will continue to flow after  $t = T_3$  in the opposite direction through the closed transistor, as shown in Fig. 3(c). At the same time, rectifier current  $i_D$  will continue to increase at the same rate, ex-

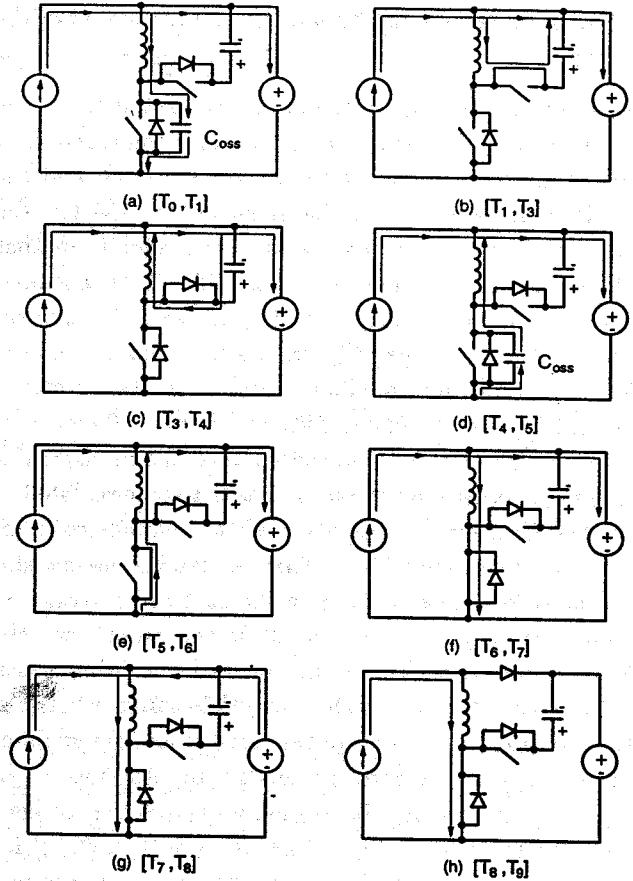


Fig. 3: Topological stages of boost power stage.

ceeding the input-current level  $I_{in}$ , Fig. 4. During this topological stage, the energy stored in clamp capacitor  $C_C$  during interval  $[T_1 - T_3]$  is returned to the inductor in the opposite direction. This interval ends at  $t = T_4$  when auxiliary switch S1 is turned off.

After S1 is turned off, inductor current  $i_L$  cannot flow anymore through clamp capacitor  $C_C$ . Instead, it continues to flow through output capacitance  $C_{oss}$  of boost switch S, as shown in Fig. 3(d). Since  $i_L$  discharges  $C_{oss}$ , boost-switch voltage  $v_S$  decreases from  $V_O + V_C$  towards zero. At the same time,  $i_L$  increases toward zero and  $i_D$  decreases toward  $I_{in}$ , as shown in Fig. 4.

Whether  $v_S$  will decrease all the way to zero depends on the energy stored in inductor L at  $t = T_4$ . If this energy is larger than the energy required to discharge  $C_{oss}$  from  $V_O + V_C$  down to zero, i.e., if

$$\frac{1}{2}L[i_L(t = T_4)]^2 \geq \frac{1}{2}C_{oss}(V_O + V_C)^2, \quad (1)$$

then  $v_S$  will reach zero. Otherwise,  $v_S$  will not be able to fall to zero, and will tend to oscillate around the  $V_{in}$

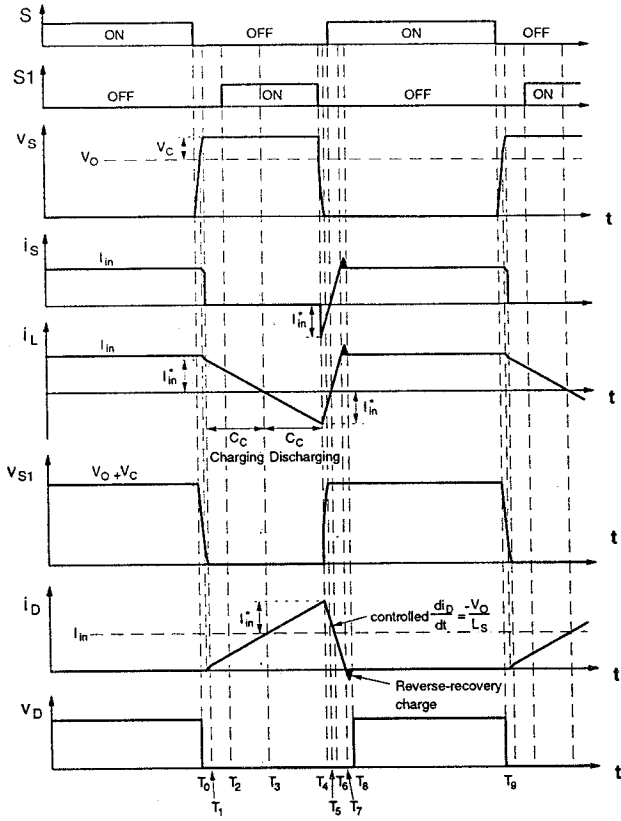


Fig. 4: Key waveforms of boost power stage.

level if boost switch S is not turned on immediately after  $v_S$  reaches its minimum.

Assuming that inductor energy is more than enough to discharge  $C_{oss}$  to zero,  $v_S$  will reach zero at  $t=T_5$ , while inductor current  $i_L$  is still negative. As a result, the antiparallel diode of S will start conducting as shown in Fig. 3(e). Because of the simultaneous conduction of the antiparallel diode of S and rectifier D, constant output voltage  $V_O$  is applied to inductor  $L_S$  so that inductor current  $i_L$  increases linearly toward zero (Fig. 4). To achieve ZVS of switch S, it is necessary to turn on the transistor of switch S during the time interval  $[T_5 - T_6]$  when the antiparallel diode of S is conducting. If the transistor of S is turned on during this interval,  $i_L$  will continue to increase linearly after  $t=T_6$ , as shown in Fig. 3(f). At the same time, rectifier current  $i_D$  will continue to decrease linearly. The rate of  $i_D$  decrease is determined by the value of  $L_S$  inductance because

$$\frac{di_D}{dt} = -\frac{V_O}{L_S}. \quad (2)$$

To reduce the rectifier-recovered charge and the associated losses, a proper  $L_S$  inductance needs to be selected. Generally, a larger inductance, which gives a

lower  $di_D/dt$  rate, results in a more efficient reduction of the reverse-recovery-associated losses [1].

The linear increase of  $i_L$  should stop at  $t=T_7$ , when  $i_L$  reaches the input-current level  $I_{in}$ , and rectifier current  $i_D$  falls to zero (Fig. 4). However, due to the residual stored charge, rectifier current  $i_D$  starts flowing in the reverse direction, as shown in Fig. 3(g), producing an overshoot of the switch current over the  $I_{in}$  level, as shown in Fig. 4. Without  $L_S$ , this reverse-recovery current would be many times larger. Once the rectifier has recovered at  $t=T_7$ , the entire input current  $I_{in}$  flows through switch S (Fig. 3(h)), until the next switching cycle is initiated at  $t=T_9$ .

Besides the stored charge that needs to be recovered before a fast-recovery rectifier can block voltage, the rectifier possesses a junction capacitance. This capacitance was neglected in the previous analysis of operation. However, in a practical boost circuit, this undesirable, parasitic capacitance has detrimental effect on the characteristics of the circuit because it increases the voltage stress of the rectifier [5].

The junction capacitance of the rectifier affects the circuit operation after rectifier D in Fig. 2 has recovered at  $t=T_8$  (Fig. 4). Namely, after stored charge has been removed from D, junction capacitance  $C_D$  of D needs to be charged to the steady-state voltage  $V_O$ . However, because  $C_D$  and  $L_S$  form a series-resonant circuit, as shown in Fig. 5(a), the voltage across  $C_D$  (rectifier voltage) and the current through  $L_S$  will resonate as shown in Fig. 5(b). The resonance is damped by the on resistance of the MOSFET of switch S and losses in inductor  $L_S$ . The amplitudes of the voltage and current oscillations are given by

$$V_{D(pk)}^{osc} = V_O, \quad (3)$$

$$I_{L(pk)}^{osc} = \frac{V_O}{Z_n} = \frac{V_O}{\sqrt{L_S/C_D}}, \quad (4)$$

where  $Z_n = \sqrt{L_S/C_D}$  is the characteristic impedance of the  $L_S-C_D$  resonant circuit. Generally, the characteristic impedance is large because of a relatively small  $C_D$ , which is typically in a ten-picofard range. As a result, the energy stored in the  $L_S-C_D$  resonant circuit is also small. However, the resonance doubles the voltage stress of the rectifier because it pulls node A in Fig. 5(a) to  $-V_O$ .

The parasitic resonance of the  $L_S-C_D$  circuit can be eliminated by clamping the voltage of node A to the ground by diode  $D_C$ , as shown in Fig. 6(a). In Fig. 6(a), when the voltage of node A reaches zero, i.e., when the reverse voltage on rectifier D reaches  $V_O$  at  $t=T_8^*$ , diode

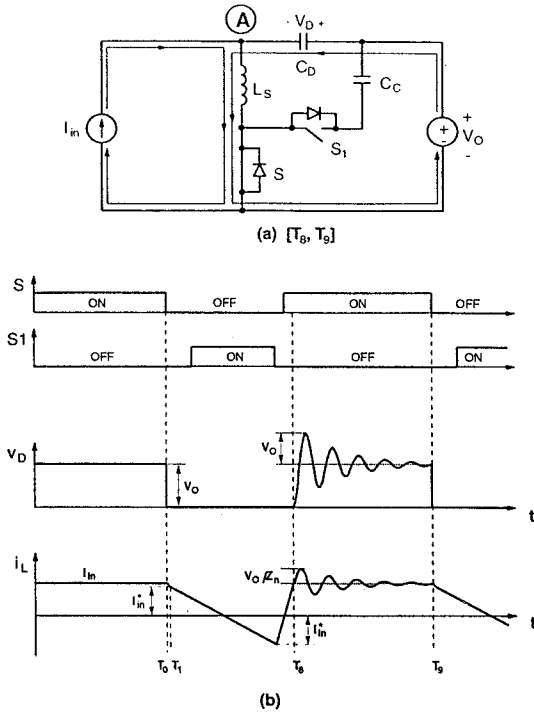


Fig. 5: Effect of junction capacitance of rectifier D: (a) topological stage of converter immediately after  $t=T_8$ ; (b) rectifier voltage  $v_D$  and inductor current  $i_L$  waveforms.

$D_C$  clamps the voltage of node A to zero by taking over current flowing through  $L_S$ , as shown in Fig. 6(b). In an ideal (lossless) power stage, current  $i_L$ , which circulates in the  $L_S$ - $D_C$  loop, will stay constant at the value given by Eq. 4 until the main switch is turned off at  $t=T_9$ , Fig. 6(c). However, in a practical converter, current  $i_L$  will decay according to

$$di_L/dt = -[V_{F(DC)} + (R_{DS(on)} + R_{LS})i_L], \quad (5)$$

where  $V_{F(DC)}$  is the forward voltage drop of clamp diode  $D_C$ ,  $R_{DS(on)}$  is the on resistance of the MOSFET of switch  $S$ , and  $R_{LS}$  is the winding resistance of inductor  $L_S$ . Generally, the power dissipated during  $i_L$  circulation through the  $L_S$ - $D_C$  loop is negligible because of a small value of circulating current. With diode  $D_C$ , the reverse voltage of main rectifier  $D$  is the same as in the "hard-switched" converter, i.e., it is equal to output voltage  $V_O$ .

### III. Design Considerations

As described in the previous section, to achieve ZVS of switches  $S$  and  $S_1$ , it is necessary to turn on the transistors of the switches during the intervals in which their antiparallel diodes are conducting. To make the antiparallel diode of  $S_1$  conduct after switch  $S$  is turned

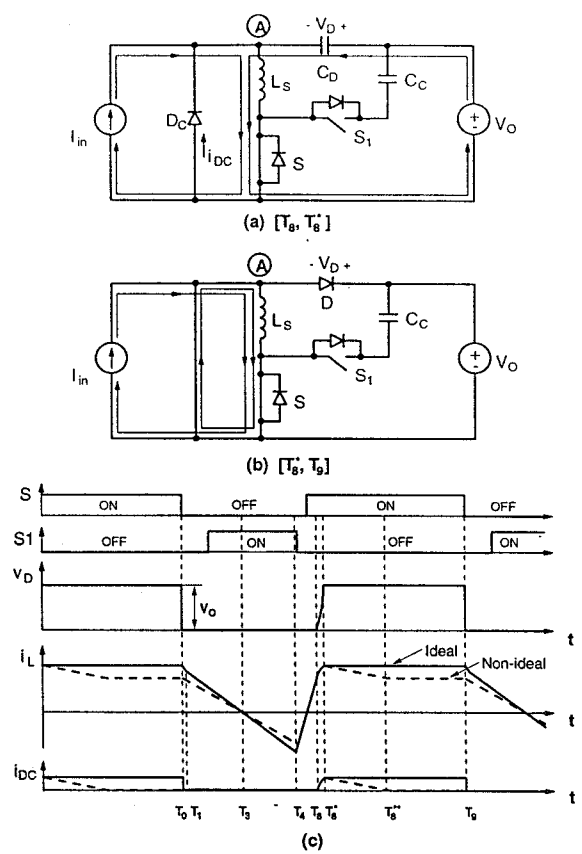


Fig. 6: Elimination of junction-capacitance effect of rectifier D: (a) topological stage of converter with clamp diode  $D_C$  during  $[T_8 - T_8^*]$  interval; (b) topological stage of converter with clamp diode  $D_C$  during  $[T_8^* - T_8^{**}]$  interval; (c) rectifier voltage  $v_D$ , inductor current  $i_L$ , and clamp-diode current  $i_{DC}$  waveforms.

off at  $t=T_9$  in Fig. 4, voltage  $v_S$  needs to increase to  $V_O + V_C$ . Since  $C_{oss}$  of switch  $S$  is charged through a series connection of a large boost inductor (represented by current source  $I_{in}$ ) and inductor  $L_S$  (Fig. 1), there is plenty of energy to charge  $C_{oss}$  up to  $V_O + V_C$  even for very low input currents. However, to discharge  $C_{oss}$  to zero and subsequently achieve ZVS of switch  $S$  after  $S_1$  is turned off ( $t=T_4$  in Fig. 4), only energy stored in  $L_S$  is available because the boost inductor current  $I_{in}$  at  $t=T_4$  flows through rectifier  $D$ . According to Eq. 1, the energy in the inductor can be increased by increasing the inductance of  $L_S$  or inductor current  $i_L(t = T_4)$ . Since  $i_L(t = T_4) = i_L(t = T_1) = I_{in}^*$  due to the required charge balance on clamp capacitor  $C_C$ , and since  $i_L(t = T_1) = I_{in}^* \approx I_{in}$  if duration of the commutation interval  $[T_0-T_1]$  is short compared to the off-time interval  $[T_0-T_6]$ , the only design variable for the stored energy is  $L_S$ . The minimum  $L_S$  is determined from the desired  $di_D/dt$  rate to control the rectifier recovered charge ac-

according to Eq. 2. Therefore, to achieve ZVS at light loads, *i.e.*, for small  $I_{in}$ , a relatively large value of  $L_S$  is required. If  $L_S$  is too large, the  $di/dt$  rate of the inductor current will be very slow, which will limit the maximum switching frequency and/or maximum output power. Therefore, in a practical design,  $L_S$  should be selected to be larger than the minimum  $L_S$  which gives the desired  $di_D/dt$  rate, but not too large to limit the switching frequency and/or maximum output power. Although, for such an  $L_S$  selection, no ZVS of S may be possible, the switching loss of S would be reduced because S would be turned on with a voltage lower than  $V_O + V_C$ .

As can be seen from Fig. 4, the voltage stresses of switches S and S1 are the same and equal to  $V_O + V_C$ . Compared to the "hard-switched" boost converter, the boost-switch stress in the proposed converter is higher for the amount of clamp voltage  $V_C$ . To keep the voltage stress of switches S and S1 within reasonable limits, it is necessary to select properly clamp-voltage level  $V_C$  by selecting a proper value of clamp-capacitor  $C_C$ .

From Fig. 4, it can be seen that clamp capacitor  $C_C$  is charged with current  $i_L$  from  $t=T_1$  to  $t=T_3$ . Since  $i_L(t=T_1) = I_{in}^* \approx I_{in}$ , and since the duration of the time interval  $[T_1-T_3]$  is approximately one-half of the off-time of main switch S, the relationship between clamp voltage  $V_C$ , inductor current  $i_L$ , and clamp-capacitor value  $C_C$  can be expressed as

$$V_C = L_S \frac{I_{in}}{(1-D)T_S/2} = \frac{2L_S f_S I_{in}}{1-D}, \quad (6)$$

where  $D$  is the duty-cycle of main switch S,  $T_S$  is the switching period, and  $f_S$  is the switching frequency. Since for a lossless boost power stage,

$$\frac{V_O}{V_{in}} = \frac{I_{in}}{I_O} = \frac{1}{1-D}, \quad (7)$$

Eq. 6 can be expressed as

$$V_C = 2L_S f_S I_O \left( \frac{V_O}{V_{in}} \right)^2. \quad (8)$$

According to Eq. 8,  $V_C$  is maximum at full load  $I_O^{max}$  and low line  $V_{in}^{min}$ . Therefore, for known  $V_O$ ,  $I_O^{max}$ ,  $V_{in}^{min}$ ,  $L_S$ , and  $f_S$ , the value of  $C_C$  can be determined for the desired maximum clamp-voltage level  $V_C$ .

Finally, in input-current-shaping applications the input voltage of the boost power stage is the rectified line voltage, while the output voltage is a dc voltage greater than the peak of the line voltage. Due to the varying input voltage and constant output voltage, the duty cycle of a boost converter used in these applications varies in

a wide range. It is maximum at close to 100% when line voltage is low (around zero), and it is minimum at the peak of the line voltage. However, when the line voltage is around zero, the energy in the boost inductor is small even with the switch duty cycle close to 100%. As a result, after switch S in Fig. 1 is turned off, the stored energy in the boost inductor is insufficient to charge output capacitance  $C_{oss}$  of S up to  $V_O + V_C$  and conduct the antiparallel diode of auxiliary switch S1. Consequently, when the MOSFET of switch S1 is turned on, clamp capacitor  $C_C$  discharges to  $C_{oss}$ . Because  $C_C \gg C_{oss}$ ,  $C_C$  discharge is small during a switching cycle. However, the voltage of  $C_C$  can discharge significantly if the described conditions persist for many switching cycles. Since the proper operation of the circuit in Fig. 1 requires that clamp voltage  $V_C$  be always positive so that it can reset the core of  $L_S$ , voltage  $V_C$  must be prevented from becoming negative. To accomplish this, a diode (typically the Schottky type) may need to be added across clamp capacitor  $C_C$ .

## IV. Topology Variations

Generally, the series connection of auxiliary switch S1 and clamp-capacitor  $C_C$  can be connected to any dc-voltage point in the circuit. As a result, the proposed technique for reduction of the reverse-recovery-related losses can be incorporated in a number of different ways. Figure 7(a) shows the implementation with the clamp circuit connected to the input, whereas Fig. 7(b) shows the implementation with the clamp circuit connected to the ground. Both implementations in Fig. 7 control the reverse-recovery-related losses by controlling the  $di_D/dt$  rate of rectifier D in the same fashion as the implementation in Fig. 1. However, the implementation in Fig. 7(a) returns the energy of inductor  $L_S$  to the input, and also reduces the current stress of the filter capacitor  $C_F$  because current  $i_L$  does not flow through  $C_F$ .

The implementation in Fig. 7(b) uses a P-type MOSFET for auxiliary switch. Since this MOSFET is referenced to the ground, non-isolated gate drive can be used for both switches. However, this implementation requires a clamp capacitor with a substantially higher voltage rating than the implementations in Figs. 1 and 7(a). The maximum voltage across capacitor  $C_C$  in N-type MOSFET implementations in Figs. 1 and 7(a) is  $V_C$ , whereas the corresponding voltage in the P-type implementation in Fig. 7(b) is  $V_O + V_C$ .

Figure 8 shows the boost converter implementation with inductor  $L_S$  in the rectifier D branch (lead) in-

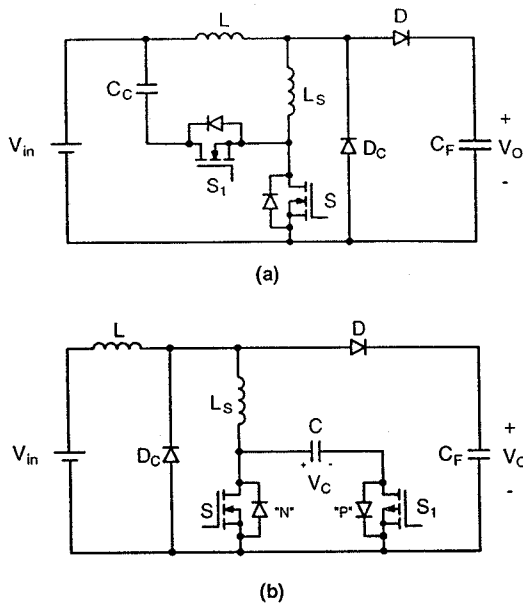


Fig. 7: Variations of boost converter implementations: (a) clamp circuit connected to input; (b) clamp circuit connected to ground.

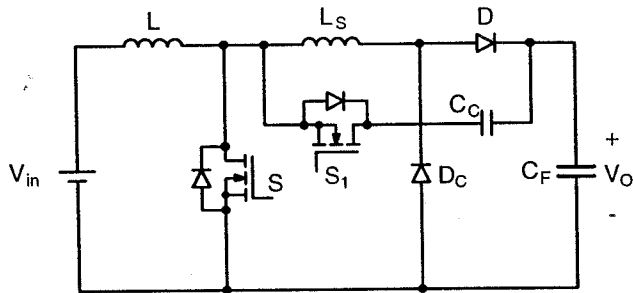


Fig. 8: Boost converter implementations with inductor  $L_S$  shifted from switch  $S$  branch (lead) to rectifier  $D$  branch (lead).

stead of in the switch  $S$  branch (lead) as in Fig. 1. The operation of this circuit is the same as that of Fig. 1, except that inductor current  $i_L$  is the same as rectifier current  $i_D$  (when  $D$  is conducting), instead of being the same as  $i_S$  (when  $S$  is conducting), as in the circuit in Fig. 1. The circuit in Fig. 8 can also be implemented with the clamp circuit connected to the input or ground, as in Fig. 7.

## V. Experimental Results

To verify the operation and evaluate the performance of the proposed technique a 500-W (400 V/ 1.25 A), prototype dc-dc converter for an input-voltage range from 120 Vdc to 350 Vdc was built using the follow-

ing components: switch  $S$  - IRFP460 (Harris); rectifier  $D$  - MUR860 (Motorola) or RHRP860 (Harris); auxiliary switch  $S_1$  - BUZ80A (Motorola); boost inductance  $L=0.475\text{mH}$  (Philips 783E-608 core, 3F3 material, 4 mm gap, 80 turns of AWG#17); snubber inductance  $L_S=14\ \mu\text{F}$  (Micrometal T106-2 toroidal core, 31 turns of AWG#17), clamp capacitance  $C_C=2\times 0.47\ \mu\text{F} / 400\ \text{V}$  (polypropylene); and output filter capacitance  $C_F=470\ \mu\text{F} / 450\ \text{V}$ . The control circuit was implemented with the UC3842 IC PWM controller and the Harris HIP2500 driver which is used to provide the proper gate-drive signals for the main and auxiliary switches.

Figure 9 shows the measured key waveforms at full power for input voltage  $V_{in}=150\ \text{Vdc}$ . From the  $i_S$  waveform in Fig. 9, it can be seen that at turn-on, the reverse-recovery-induced current spike through the switch is completely eliminated. Also, from waveform  $V_{DS}$ , it can be seen that for the operating conditions of Fig. 9, the switch is turned on at zero voltage. The maximum voltage of the main switch is approximately 440 V, implying that the clam-capacitor voltage is approximately 40 V. It also should be noted that rectifier-voltage waveform  $v_D$  is ringing free because of the effective clamping action of clamp diode  $D_C$ . As a result, the maximum reverse voltage across rectifier  $D$  is equal to the output voltage, *i.e.*, 400 V. Generally, due to the absence of ringings and abrupt transitions in the semiconductor voltage and current waveforms, the EMI performance of the converter is expected to be improved.

The solid lines in Fig. 10 show the measured efficiencies of the experimental, boost power stage at full power as functions of the input voltage for implementations with two rectifiers with different reverse-recovery characteristics. The RHRP860 (Harris) rectifier exhibits a faster reverse-recovery characteristic than the MUR860 (Motorola) rectifier. For comparison purposes, Fig. 10 shows the measured efficiencies for the two rectifiers without the active snubber (dashed lines). As can be seen from Fig. 10, without the active snubber, the efficiency of the implementation with the MUR860 rectifier is the lowest, ranging from 92.4% at low line to 98% at high line. The corresponding efficiency of the implementation with the faster RHRP860 rectifier is slightly higher, *i.e.*, it is in the 94.2%-98.3% range. For both implementations, the efficiency at low line, where the input current is maximum, is the lowest because the reverse-recovery-related losses as well as conduction losses of semiconductor components are the highest. With the active snubber, the efficiencies of both implementations are significantly improved (96% to 99% range). More-

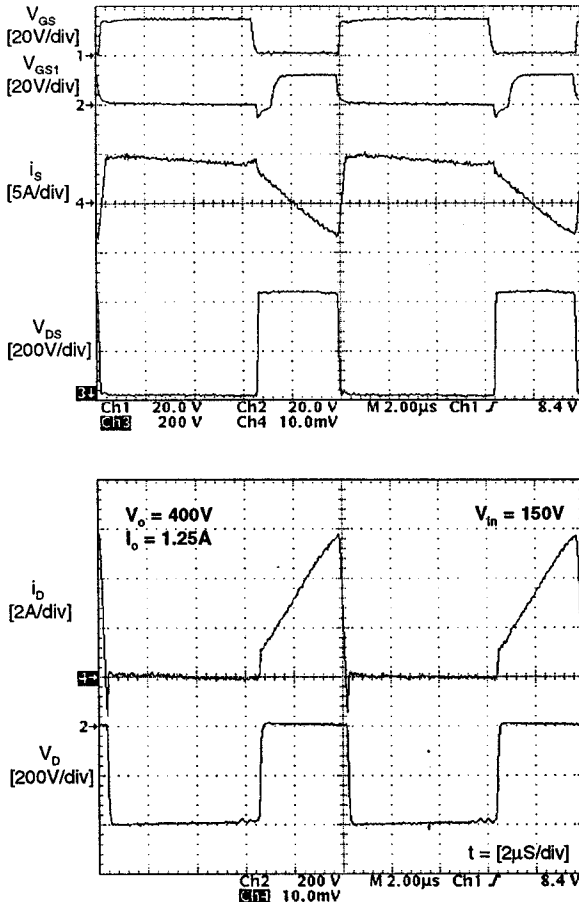


Fig. 9: Measured key waveforms of experimental converter with MUR860 rectifier at  $P_O=500$  W and  $V_{in}=150$  Vdc.

over, the differences between the efficiencies with the two rectifiers are less than 0.4% throughout the entire input-voltage range. In fact, with the active snubber, the effect of the reverse-recovery speed of the rectifier on the efficiency is practically eliminated. A slightly higher efficiency of the RHRP860 implementation with the active snubber compared to that with the MUR860 rectifier can be attributed to a slightly lower forward-voltage drop of the RHRP860 rectifier.

## VI. Summary

Operation and design guidelines for an active-snubber technique which reduces the reverse-recovery-related losses in high-voltage, high-power boost converters are presented. The technique employs a snubber inductor connected in series with the boost switch and rectifier to control the di/dt rate of the rectifier current during its turn-off. The energy from the snubber inductor after the boost switch turn-off is returned to the input or deliv-

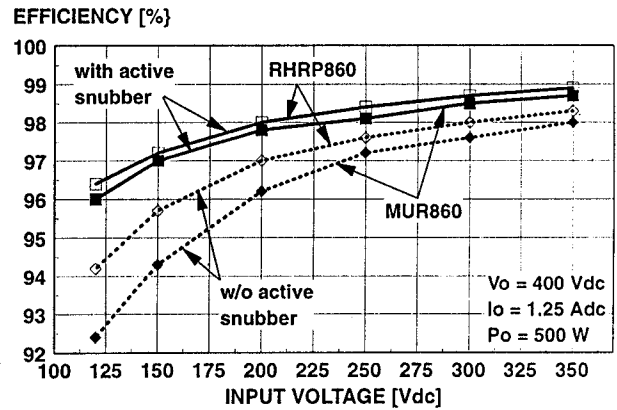


Fig. 10: Measured, full-power efficiencies of experimental converter with (solid lines) and without (dashed lines) active snubber as functions of output power for implementations with MUR860 and RHRP860 rectifiers.

ered to the output via the active snubber. By connecting a clamp diode between the anode of the boost rectifier and ground to eliminate the parasitic ringing between the junction capacitance of the rectifier and the snubber inductor, the stress of the rectifier is minimized. The proposed technique was verified on a 500-W (400-V / 1.25-A) prototype boost converter. The same technique can be extended to any member of the PWM-converter family.

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