

Design Trade-offs in Continuous Current-Mode Controlled Boost Power-Factor Correction Circuits

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Abstract

The design trade-offs in the boost power-factor correction (PFC) circuits with peak and average current-mode control are presented. The effects of slope compensation in peak current-mode control and current-amplifier compensation in average current-mode control on line current distortions are discussed. A PSPICE program that employs a simplified PFC small-signal model to facilitate the design optimization of the current loop in the average current-mode control is also provided.

1. Introduction

With the ever-increasing demand for power from the ac line and more stringent requirements for power quality, power-factor correction (PFC) is becoming an integral part of switching power supplies. To meet the needs of the power supply industry, a number of power-factor correction control ICs were introduced on the market in the past few years [1,2,3,4].

A variety of circuit topologies are available for PFC. These include continuous-mode boost converters with peak, average, and hysteretic control, and discontinuous-mode boost and flyback converters. Discontinuous-mode boost and flyback PFC circuits are basically voltage-mode controlled converters that operate with a constant on-time of the switch within each line cycle. In these circuits, the line current follows the line voltage automatically. While the discontinuous-mode converters are well suited for low-power applications, peak and average current-mode controlled boost converters operating in continuous mode are still the primary choice for many medium and high-power applications.

In many recently published scholarly papers, new PFC topologies and elaborate small-signal models were presented. At the same time, IC manufacturers' application notes do not offer explanations of general design problems, but rather address the specific issues concerning the implementation of their control ICs. As a result, the performance optimization of PFC circuits is becoming a difficult task for many design engineers.

In this paper, the effort is concentrated on detailed explanations of the design trade-offs in the peak and average current-mode controlled boost PFC circuits. A simplified PFC small-signal model is derived from the PWM switch model and is applied in the current-feedback loop design. Finally, a PSPICE program for the design optimization of the current loop in the average current-mode control is provided.

The locations of PFC power-stage poles and zeros change as the line varies from zero to its peak amplitude. To analyze this time-varying system behavior, the method of quasi-static analysis [5] can be applied. In this approach, the line voltage is assumed to be constant within each high-frequency switching cycle since the switching frequency is much higher than the line frequency. Because the system poles and zeros are moving as the instantaneous line voltage changes, a feedback circuit with a time-varying gain will be the best choice for PFC circuit control [6]. However, a time-varying-gain feedback circuit may be complex and difficult to implement in practice, and, therefore, fix-gain feedback circuits are usually used. For a fix-gain feedback circuit, the worst-case circuit operating point must be determined and the circuit properly compensated to ensure the system stability over the entire line-voltage range.

A current-mode controlled PFC circuit possesses a current-regulation inner loop and a voltage-regulation outer loop. To minimize the input current distortions, the bandwidth of the voltage-feedback loop is very low, well

below 60 Hz. The voltage-feedback loop design was extensively analyzed by a number of authors [7,8], and, therefore, is not discussed in this paper. Only the current-loop design trade-offs are presented in the following sections.

2. Peak Current-Mode Control

Figure 1 shows a schematic diagram of a constant-frequency, peak current-mode controlled boost PFC circuit. In this circuit, the switch is turned on until the inductor current intersects a scaled line voltage. The scaling factor is determined by the resistive divider and the error voltage from the output-voltage feedback loop. As the ac line voltage changes from zero to its peak amplitude, the duty cycle also varies from its maximum value (usually 95%) to its minimum value near the peak of the line voltage. Therefore, the problem of current-loop instability over the 50% duty cycle, which is present in constant-frequency, PWM dc-to-dc converters, also occurs in this circuit. In fact, this problem becomes even more difficult to deal with because of the varying line voltage.

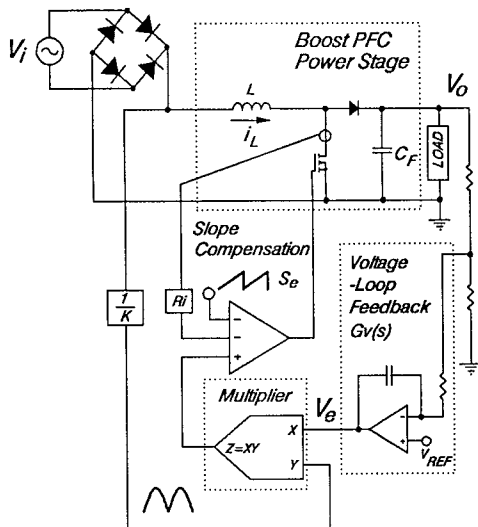


Figure 1. Conceptual circuit diagram of peak current-mode controlled boost PFC circuit.

In a number of papers [9,10], it was shown that by adding a slope compensation to the sensed inductor current waveform the system stability over the 50% duty cycle can be achieved. Figures 2(a) through 2(d) show that by properly adding slope compensation, the unstable regions of the inductor current are eliminated. A closer examination of the inductor current waveform without slope compensation in Fig. 2(a) shows the unstable regions near the zero crossings of the line voltage. The unstable region

that occurs at the rising slope of the sinusoidal current waveform in Fig. 2(a) extends to higher current levels than the unstable region that occurs at the falling slope. In fact, when a slope compensation is introduced, instability may occur only on the rising slope, as shown in Fig. 2(b). If the external ramp is increased enough, the current-loop stability can be achieved at all line voltages (Figs. 2(c) and 2(d)). A properly selected external ramp should be large enough to stabilize the current loop at the worst-case operating point (Fig. 2(c)) but not too large to introduce unnecessary distortions of the current waveform (Fig. 2(d)).

The effect of the external ramp on the line current-distortions is clearly shown in Fig. 3. Current reference I_{ref} is obtained by scaling down the line voltage through a resistive divider with scaling factor K and multiplying it with error voltage V_e from the output of the voltage error amplifier. Without an external ramp, during a few cycles following the zero-voltage crossing of the line voltage, the inductor current is unable to reach the current reference with the maximum on-time due to the small voltage applied to the inductor. During this period, the circuit operates in discontinuous mode. If an external ramp is added to the current waveform, as shown in Fig. 3(a), the duration of the discontinuous mode increases, since the ramp shortens the on-time of the switch and further slows down the inductor current build-up. As a result, the line current waveform shows more severe zero-crossover distortions when a compensation ramp is used. As the ramp increases, the distortion period lengthens. The effect of the external ramp on the distortions of the line current near the zero crossing of the line voltage can be calculated mathematically as outlined below.

According to Fig. 3(a), instantaneous peak switch current $i_p(t)$ is

$$i_p(t) = I_{ref} - S_e t_{on} = \frac{V_p \sin \omega t}{K} V_e - S_e t_{on}, \quad (1)$$

where V_p is the peak amplitude of the line voltage, K is the scaling factor, V_e is the output voltage of the voltage-feedback-loop error amplifier, ω is the line frequency, S_e is the slope of the external ramp, and t_{on} is the on-time of the switch.

In the continuous-conduction region, t_{on} can be derived from the dc gain of the boost converter:

$$\frac{V_o}{V_p \sin \omega t} = \frac{1}{1 - t_{on}/T_s}, \quad (2)$$

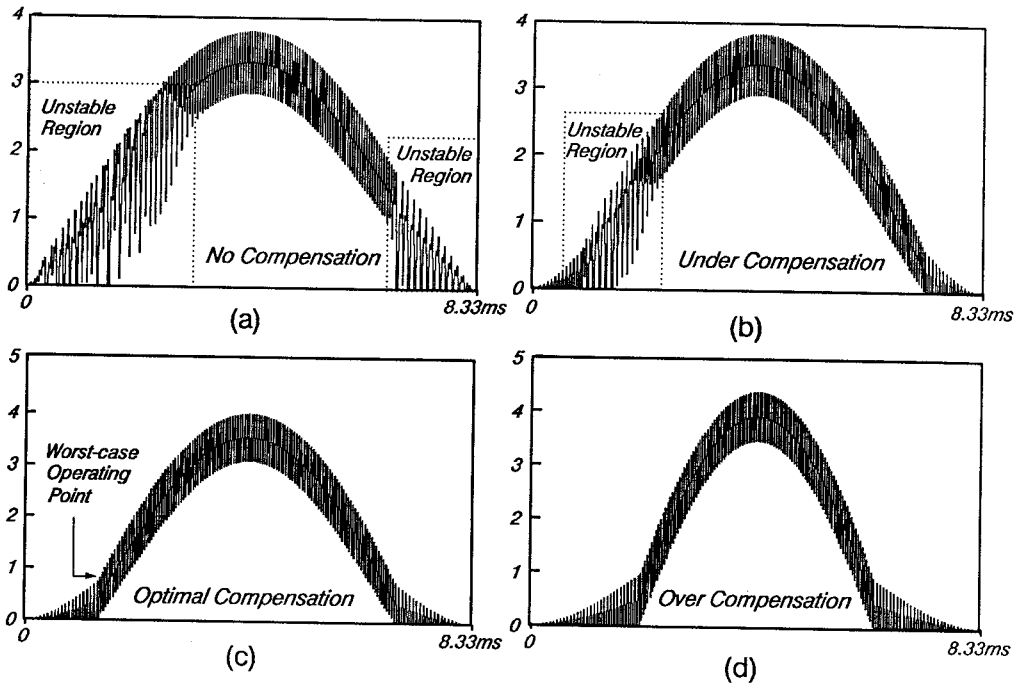


Figure 2. Inductor current of peak current-mode controlled boost PFC circuit with different compensations: (a) no compensation; (b) under compensation; (c) optimal compensation; (d) over compensation.

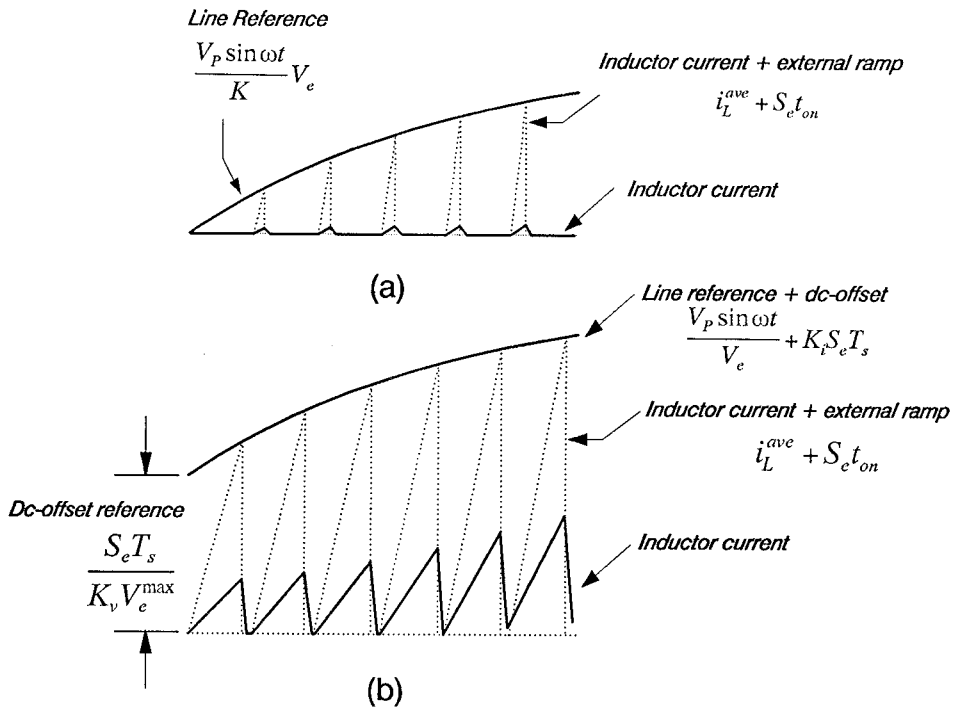


Figure 3. Inductor current waveform near zero crossing of line voltage: (a) without dc-offset (b) with dc-offset.

where T_s is the switching frequency, and V_o is the output voltage. From Eqs. (1) and (2), $i_p(t)$ can be expressed as

$$i_p(t) = \left(\frac{V_p V_e}{K} + \frac{S_e T_s V_p}{V_o} \right) \sin \omega t - S_e T_s. \quad (3)$$

Average inductor current $i_L^{ave}(t)$ during a switching cycle is related to peak current $i_p(t)$ and ripple current $\Delta i_L(t)$ by the following expression:

$$i_L^{ave}(t) = i_p(t) - \frac{1}{2} \Delta i_L(t). \quad (4)$$

Since ripple current $\Delta i_L(t)$ is

$$\Delta i_L(t) = \frac{V_p \sin \omega t}{L} t_{on}, \quad (5)$$

where L is the choke inductance, the average line current is given as:

$$i_L^{ave}(t) = \left(\frac{V_e V_p}{K} + \frac{S_e T_s V_p}{V_o} - \frac{T_s V_p}{2L} \right) \sin \omega t + \frac{T_s V_p^2}{2L V_o} \sin^2 \omega t - S_e T_s. \quad (6)$$

In Eq. (6), all parameters except the error voltage V_e are constant once the external ramp S_e is selected. The value of V_e is dependent on the input voltage and load current, and the extend of its relative variations can be determined from the energy balance stated in the following expression:

$$V_i \frac{V_i}{K} V_e = V_o I_o, \quad (7)$$

where V_i is the rms line voltage, V_o is the output voltage, and I_o is the load current. The maximum error voltage occurs at low line and full load, i.e.,

$$V_e^{max} = K V_o \frac{I_o^{max}}{V_i^{min2}}, \quad (8)$$

where V_i^{min} is the low-line rms voltage and I_o^{max} is the full-load current. The ratio of the error voltage at any line and load to the maximum error voltage is represented by scaling factor K_e :

$$V_e = K_e V_e^{max}, \quad (9)$$

where

$$K_e = \left(\frac{I_o}{I_o^{max}} \right) \left(\frac{V_i^{min}}{V_i} \right)^2. \quad (10)$$

As can be seen from Eq. (10), K_e is proportional to the load current and inversely proportional to the square of the rms line voltage. In Eq. (10), two scaling factors can be further defined: K_i - the ratio of load current to full-load current I_o/I_o^{max} and K_v - the square of the ratio of low-line rms voltage over rms line voltage $(V_i^{min}/V_i)^2$.

According to Eq. (10), for a PFC circuit operating with a universal input voltage (90 Vac to 270 Vac), the error voltage V_e at 270 Vac and 25% of full load is thirty six times smaller than the corresponding voltage at 90 Vac and full load. Thus, as the rms line voltage increases or the load decreases, the current reference decreases, causing large line current distortions near the zero crossings of the line voltage.

As an example, Fig. 4 shows the plots of the average inductor current (normalized to the peak amplitude of the line voltage reference) for various rms line voltages at full load obtained from Eq. (6) for an experimental circuit with parameters given in Table 1. As can be seen, a dead-angle period is generated near the zero crossing of the current waveform. This is the period when the switch is turned off early due to the presence of the external ramp. Since very little energy is stored in the inductor during this period, the average inductor current is virtually zero. The existence of the dead angle has detrimental effects on the power factor and harmonic distortion, as discussed in Ref. [2].

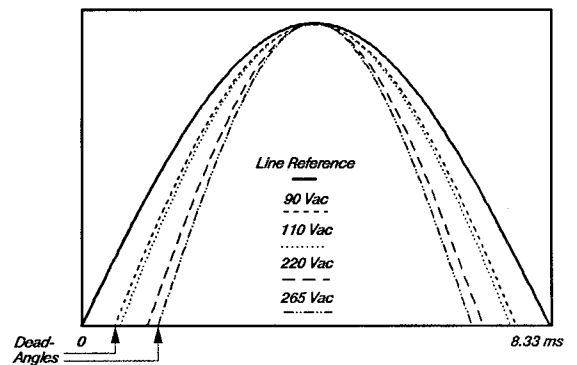


Figure 4. Normalized average inductor currents at full load for different rms line voltages.

TABLE 1
Circuit Component Values and Parameters
for Experimental Converter

V_i^{\min}	90 Vac	V_o	380 Vdc
V_i^{\max}	265 Vac	L	2 mH
I_o^{\max}	0.4 Adc	f_s	50 kHz
I_o^{\min}	0.0 Adc	S_e	90000 A/S

Once the optimal slope of the compensation ramp is selected, reduction of the input-current distortions can be achieved by introducing a dc offset in the current reference signal, as shown in Fig. 3(b). According to Eq. (6), the dead angle in the input-current waveform can be eliminated by adding a constant dc offset equal to $S_e T_s$. The best point to add this dc offset would be the input of the PWM comparator, as shown in Fig. 5(a).

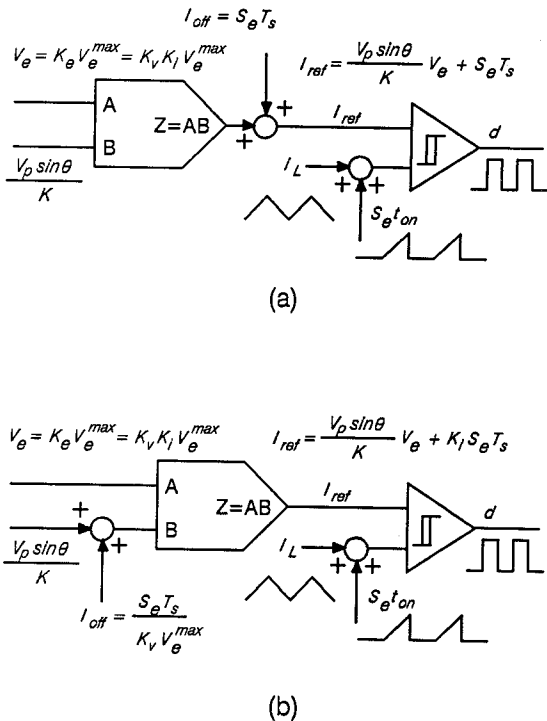


Figure 5. Conceptual block diagram of dc-offset implementation: (a) constant dc-offset injection; (b) variable dc-offset injection.

Although this scheme would work nicely at full load, as shown in Fig. 6, it may suffer from the output-voltage run

away at light loads because at light loads the converter may become uncontrollable. Namely, to control the converter down to very light loads, it is necessary that the current reference I_{ref} decreases as the load decreases. This assures that the duty cycle decreases as the load becomes lighter. With a constant dc offset in the current reference, this does not happen because the dc offset determines the minimum of the current reference. As a result, in the presence of a dc offset, the minimum duty cycle may be increased to the point where the converter cannot regulate the output voltage at light loads. To eliminate this problem the dc offset injection point should be moved to the input of the multiplier, as shown in Fig. 5(b). In this case, the injected dc offset $S_e T_s / K_v$ does not affect the minimum duty cycle since at the output of the multiplier the dc offset decreases as the load current decreases ($K_i \rightarrow 0$ as $I_o \rightarrow 0$). Since the injected offset $S_e T_s / K_v$ is only depends on the line voltage ($\propto V_i^2$), it does not eliminate the dead angle completely because it does not cancel $S_e T_s$ in Eq. (6) for all load conditions as shown in Fig. 7. Although the input-current distortions at light loads are present, the implementation of this approach is relatively easy [2].

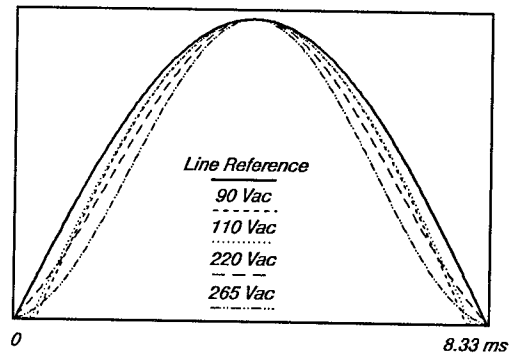


Figure 6. Normalized average inductor currents at full load for different rms line voltages with dc offset.

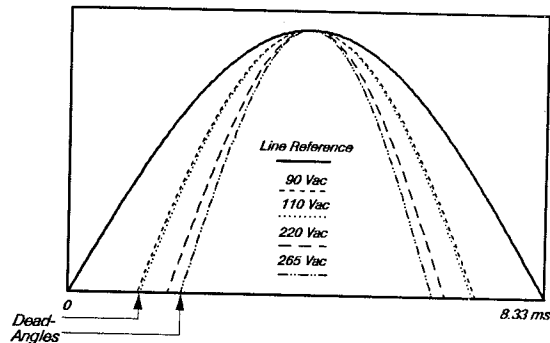


Figure 7. Normalized average inductor currents at 25% full load for different rms line voltages with dc offset.

3. Modelling of Peak Current-Mode Controlled Boost PFC

In the previous section, the external ramp is shown to have a significant effect on the stability and distortions of the inductor current. To minimize the current distortions, the external ramp should be selected just enough to stabilize the inductor current at the worst-case operating point near the zero crossings of the line voltage. To evaluate the stability margin with various values of the slope compensation, loop gain of the current-feedback loop has to be examined. Figure 8 represents the small-signal block diagram of the peak current-mode controlled boost converter. The current loop consists of power-stage duty-cycle to inductor-current gain G_{id} , modulator gain F_m , sampling gain $H_c(s)$, and the gain of the current-sense network R_i [10]. $G_v(s)$ represents the low-frequency output voltage-feedback transfer function.

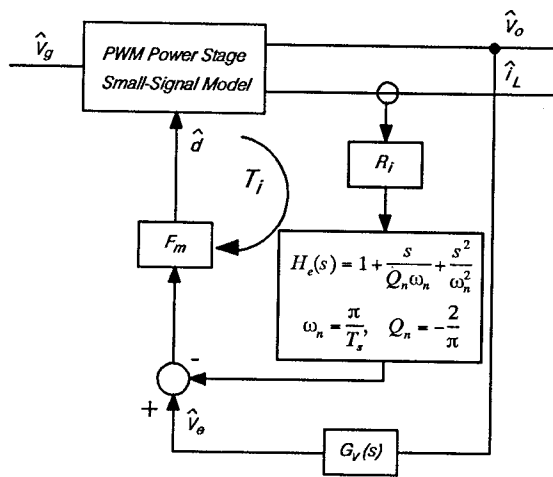


Figure 8. Small-signal block diagram of peak current-mode controlled boost PFC.

A. Power Stage Transfer Function

Due to the varying line voltage, the power stage transfer function, G_{id} , is determined using the quasi-static analysis [5], which assumes that the line and output voltages are constant within each switching cycle. By applying the PWM switch model [11] to the boost converter, the small-signal equivalent circuit shown in Fig. 9(a) is obtained. As can be seen, the power stage dc gain, poles, and zero are moving as the instantaneous line voltage changes (D changes with the line). In a PFC circuit, the

output filter capacitor is usually large in order to meet the holdup-time requirement and to reduce the 120 Hz ripple. As a result, the filter capacitor can be assumed to be a constant voltage source. At high-frequencies, the filter capacitor is a short circuit, as shown in Fig. 9(b).

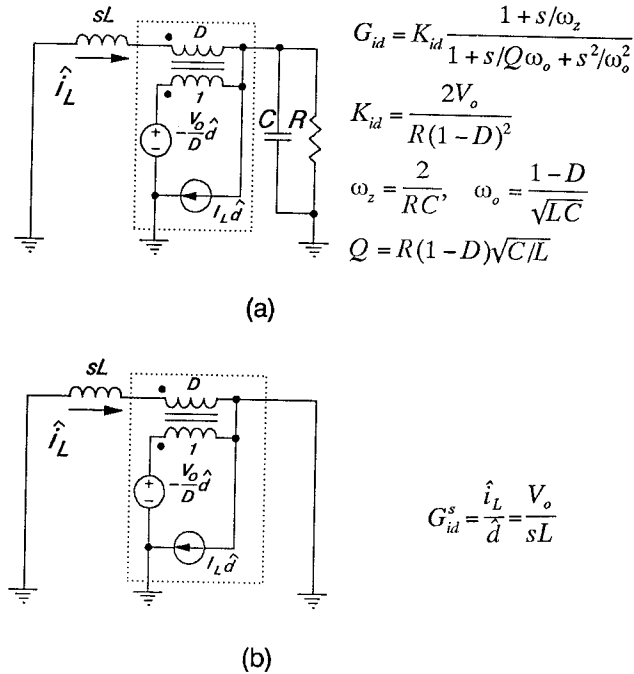


Figure 9. Small-signal models of the boost power stages: (a) exact; (b) simplified.

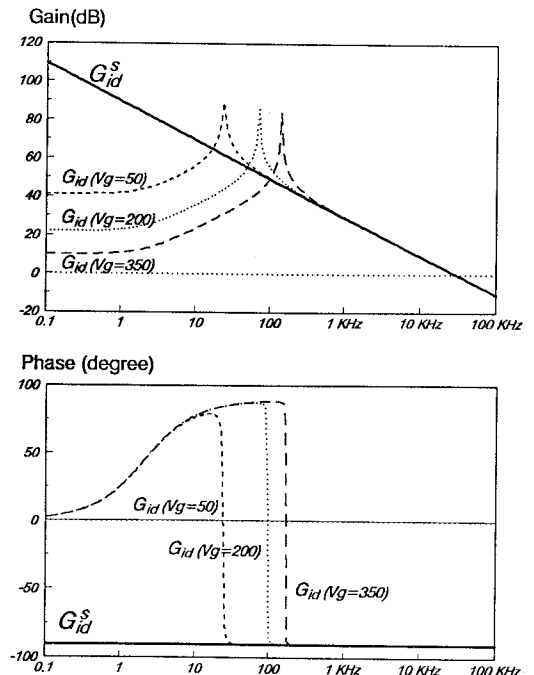


Figure 10. Duty-cycle to inductor-current transfer functions, G_{id} and G_{id}^s .

Figure 10 shows the plots of transfer function G_{id} at selected instantaneous line voltages, along with simplified transfer function G_{id}^s . It can be seen that although the power-stage dc gain, poles, and zero are changing with the line, the high-frequency portions of the responses are identical, and can be well represented by the simplified transfer function G_{id}^s . This simplified power-stage gain G_{id}^s is used in the subsequent derivations of the current-loop gain transfer function.

B. Modulator Gain

The modulator gain of the peak current-mode boost dc-to-dc converter [10] is modified for PFC circuits to include the effect of the varying slope of the scaled line reference (Fig. 3). The modulator gain is

$$F_m = \frac{1}{(S_e + S_N - S_L) T_s R_i}, \quad (11)$$

where

$$S_L = \frac{d}{dt} \left(\frac{V_p \sin \omega t}{K} \right) = \frac{\omega V_p}{K} \cos \omega t, \quad (12)$$

and S_e is the slope of external ramp compensation, S_N is the inductor current slope during the switch on-time and S_L is the slope of the scaled line reference.

The region of the positive slope of the current reference corresponds to the region where the line voltage rises from zero to its peak value. In this region, the positive slope of the current reference tends to cancel the effect of the compensation slope. In the region where the input voltage falls from the peak value to zero, the current-reference slope is negative. This negative slope effectively increases the compensation slope.

In fact, the current-loop instability shown in Fig. 2(b), where the unstable region only appears at the rising slope of the current waveform, can be attributed to the effect of the current-reference slope. The effect of S_L is stronger in PFC circuits running at low switching frequencies. At high switching frequencies, due to a small inductor value, inductor current on slope S_n is much bigger than S_L , so that the effect of the current-reference slope is negligible.

C. Current-Loop Gain

From the small-signal block diagram of Fig. 8, the simplified current-loop gain transfer function is

$$T_i(s) = F_m R_i G_{id}^s H_c(s) = \frac{F_m R_i V_o}{sL} \left(1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \right). \quad (13)$$

Although the high-frequency portion of the boost power-stage duty-cycle to inductor-current transfer function does not depend on the instantaneous line voltage, the inductor current on-time slope depends strongly on the line voltage. As the line voltage varies from zero to its maximum value in a 60 Hz line cycle, the crossover frequency, gain, and phase margin of T_i change. Figure 11 shows a plot of the current-loop gains at different instantaneous line voltages without slope compensation. The gain margins and phase margins are listed in Table 2. The effect of the double zero and the phase lag of $H_c(s)$ at one-half of switching frequency is obvious. At low line voltage, current loop gain $T_i(s)$ never crosses the zero dB axis. As the instantaneous line voltage increases, modulator gain F_m decreases, moving the loop gain curve down. Above a certain line voltage, the loop-gain curve crosses the zero dB axis with a sufficient phase margin.

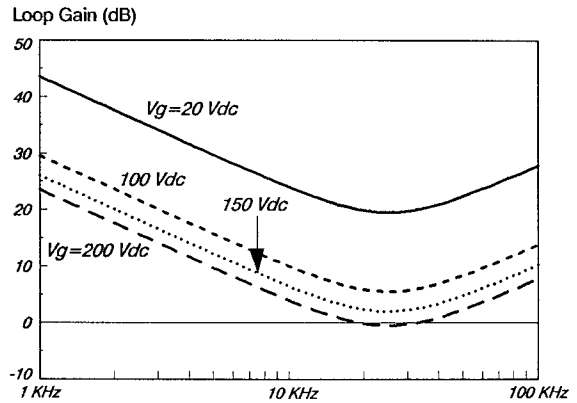


Figure 11. Current-loop gains for different instantaneous line voltages without external-ramp compensation.

TABLE 2
Current-Loop Gains and Phase Margins
Without Slope Compensation

V_g	Gain Margin	Phase Margin
20 V	-19.5 dB	-
100 V	-5.6 dB	-
150 V	-2.0 dB	-
200 V	+0.5 dB	18 °
300 V	+4.0 dB	51 °
350 V	+5.3 dB	57 °

From Fig. 11, it can be seen that without a properly selected slope compensation, the current loop gain is too high at low voltage, causing the system to be unstable. The worst-case instability point is at the line voltage when the inductor current moves from discontinuous to continuous. For a given output voltage, V_o , the worst case line voltage, V_g^{wc} , is

$$V_g^{wc} = (1 - D_{max})V_o. \quad (14)$$

For an off-line boost PFC circuit, the output voltage is usually 380 V. With a maximum duty-cycle of 95%, the worst-case line voltage from Eq. (14) is

$$V_g^{wc} \approx 20 \text{ Vdc}. \quad (15)$$

At the worst-case operating point, the external ramp should be selected large enough to ensure the current stability but not large enough to distort the current waveform. By using the current-loop gain transfer function of Eq. (13), a table of the external ramp S_e as a percentage of inductor current down slope S_f versus the phase margin is generated for the experimental converter, as shown in Table 3.

For example, when the external ramp S_e equals to one-half of the inductor current down slope (90000 A/s), the current loop has a phase margin of 20° and a crossover frequency of 19 kHz at the worst-case operating point. A plot of current-loop gains at various instantaneous line voltages for $S_e = 90000$ A/s is shown in Fig. 12.

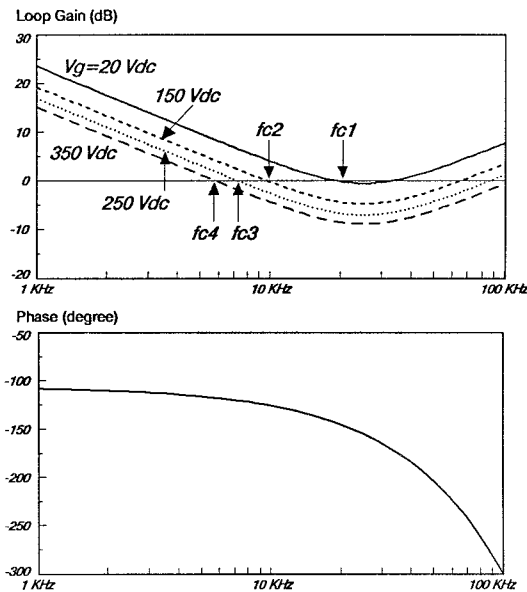


Figure 12. Current-loop gains and phases for different instantaneous line voltages with external-ramp compensation ($S_e = 90000$ A/s).

TABLE 3
Current-Loop Gains and Phase Margins
for Different Slope Compensations

S_e	Gain Margin	Phase Margin
0	-19.5 dB	-
$0.25 S_f$	-4.7 dB	-
$0.5 S_f$	+0.5 dB	20°
$0.75 S_f$	+3.7 dB	50°
$1.0 S_f$	+6.0 dB	60°

4. Average Current-Mode Control

The recently proposed average current-mode control has been widely used in power-factor correction applications [4]. Figure 13 shows the conceptual circuit diagram of the boost PFC circuit with average current-mode control, whereas Fig. 14 shows the corresponding small-signal block diagram [12].

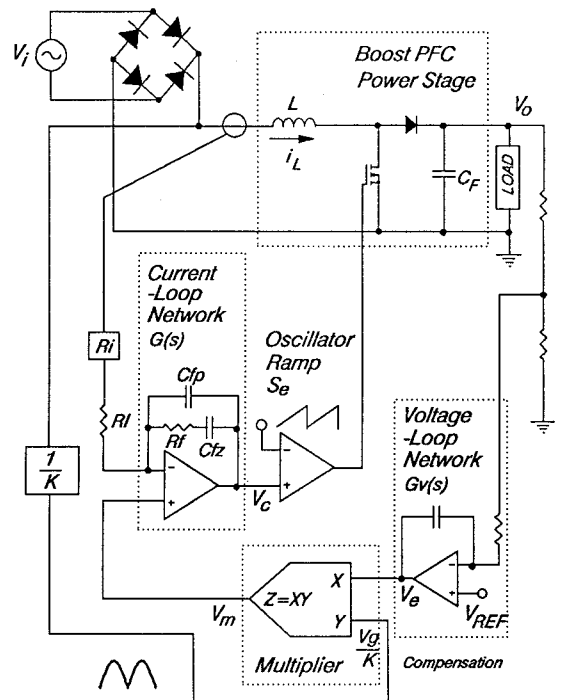


Figure 13. Conceptual circuit diagram of average current-mode controlled boost PFC circuit.

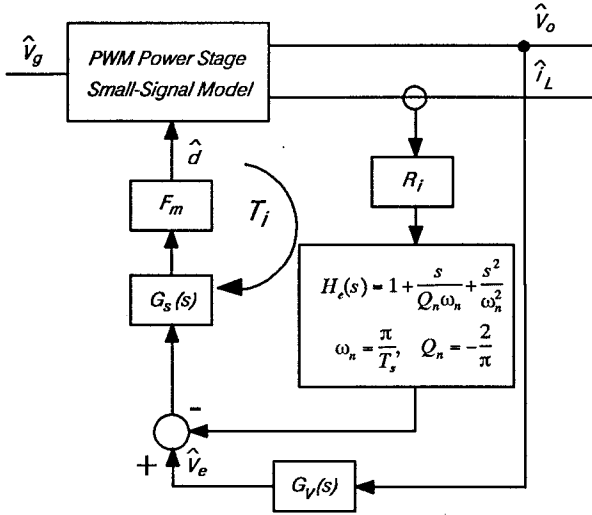


Figure 14. Small-signal block diagram of average current-mode controlled boost PFC.

The main feature of the average current-mode control is the presence of a current amplifier (block $G(s)$ in Fig. 13) that is used to average the inductor current. The error voltage of the current amplifier is compared with a fixed ramp to generate a proper drive of the switch. Therefore, in this control, it is the average inductor current rather than the peak current that is controlled to follow the line voltage.

Another important feature of the average current-mode control when it is used in PFC applications is that, near the zero crossings of the line voltage, the converter operates with the maximum duty cycle. As a result, the dead-angle period, which is encountered in the peak current-mode control, is greatly reduced.

In the average current-mode control, the current amplifier with a two-pole, one zero compensation network, shown in Fig. 15, is used. The small-signal transfer function of the amplifier is [12,13]:

$$G(s) = \frac{\omega_i (1 + s/\omega_z)}{s (1 + s/\omega_p)}, \quad (16)$$

where

$$\omega_i = \frac{1}{R_i(C_{FP} + C_{FZ})}, \quad (17)$$

$$\omega_z = \frac{1}{R_F C_{FZ}}, \quad (18)$$

$$\omega_p = \frac{C_{FZ} + C_{FP}}{R_F C_{FZ} C_{FP}}. \quad (19)$$

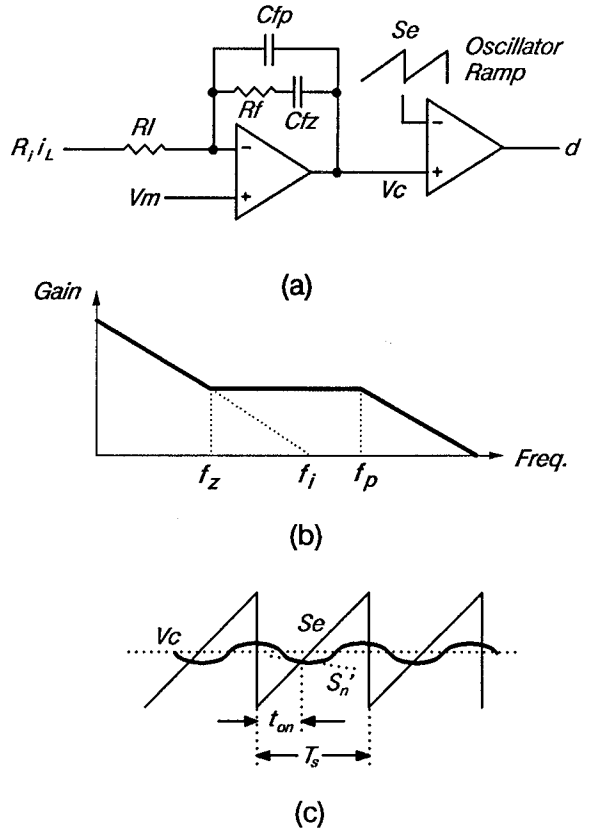


Figure 15. Current-loop compensator and modulator: (a) circuit diagram; (b) gain response; (c) modulator input waveforms.

Modulator gain F_m of the average current-mode control is defined as [12]

$$F_m = \frac{1}{(S_e + S_n') T_s R_i}, \quad (20)$$

where S_e is the external-ramp slope and S_n' is the inductor current on-slope at the output of the current amplifier as shown in Fig. 15(c). Since the slope of external ramp S_e is much higher than the integrated inductor current on-slope S_n' , the modulator gain can be approximated as:

$$F_m \approx \frac{1}{S_e T_s R_i} = \frac{1}{V_{se}}, \quad (21)$$

where V_{se} is the peak-to-peak amplitude of the external ramp.

It was shown that if the high-frequency pole ω_p is placed at or after one-half of the switching frequency to filter out the switching ripple of the sensed inductor current, it has no effect on the gain and phase of the current-loop gain before one half of the switching frequency [12]. There-

fore, only the integrator gain ω_i and zero ω_z are affecting the current-loop gain below one-half of the switching frequency. Using Eq. (21) together with the sampling gain and simplified duty-cycle to inductor-current transfer function G_{id}^s , the loop gain transfer function of the average current-mode controlled boost PFC is:

$$T_i = \frac{\omega_i R_i V_o}{V_{sc} L s^2} \left(1 + \frac{s}{\omega_z} \right) \left(1 + \frac{s}{Q_n \omega_n} + \frac{s^2}{\omega_n^2} \right). \quad (22)$$

There are several differences between loop gain transfer function $T_i(s)$ of Eq. (22) and the loop gain transfer function of Eq. (13). In the peak current-mode control, the loop gain crossover frequencies decreases as the line voltage increases from zero to maximum, whereas in the average current-mode control, the loop gain crossover frequency does not depend upon the line voltage variations due to the presence of a large external ramp slope.

To optimize the average current-mode control, the current loop should be designed to have the maximum low-frequency gain and acceptable phase margin at the crossover frequency to minimize the input current distortions. Reference [13] gives the selection criteria for the placement of the compensation zero, pole, and integrator gain. According to the guidelines, the zero should be placed at least one decade below the switching frequency and the pole should be placed at one-half of the switching frequency. Although this design guarantees the stability of the current-loop feedback circuit, it may not be optimal. Namely, at light loads, when the PFC circuit starts running in the discontinuous mode, the dc gain of the power stage drops significantly. As a result, the loop gain decreases, causing higher input current distortions. Since the implementation of a load-dependent variable gain feedback circuit is not easy, the only alternative is to maximize the dc current loop gain at full load. The dc gain can be increased by moving the locations of the integrator gain ω_i and zero ω_z towards high-frequency pole ω_p . However, placing the zero at higher frequencies results in a smaller phase margin. To optimize this trade-off, current-loop transfer function of Eq. (22) can be used to determine the compensation network that results in a stable system with a maximum dc gain. To facilitate this design, a PSPICE program that implements Eq. (22) is given in the Appendix.

Table 4 summarizes the effects of different compensations on the stability and current distortions of the experimental power stage (Table 1) at high line (265 Vac) and 25% of full load (0.1 Adc). The 3rd to 13th odd-harmonic currents are measured as a percentage of the fundamental current with an ac power analyzer (Voltech

PM1000). The middle column in Table 4 corresponds to the compensation network selected according to Ref. [13]. In this case, the phase margin (PM) of 30° is obtained at a crossover frequency f_c of 8.0 kHz. The total harmonic distortions (THD) are 15.2%. By moving the integrator gain to 72.5 kHz and zero to 7.2 kHz, and by lowering the feedback capacitor C_{FZ} to 1 nF, the crossover frequency is increased to 8.7 kHz, but the phase margin is decreased to 22°. The total harmonic distortions decrease to 12.5%, while the power factor (PF) increases to 89.5%. We found that in this PFC design, a 22 degree phase margin of the current loop was quite satisfactory.

TABLE 4
Line Current Harmonic Distortions and Power Factor at Different Compensations

	$C_{FZ}=3.3\text{nF}$	$C_{FZ}=1.5\text{ nF}$	$C_{FZ}=1\text{ nF}$
f_c	7.1 kHz	8.0 kHz	8.7 kHz
f_i	25.0 kHz	51.4 kHz	72.5 kHz
f_z	2.2 kHz	4.8 kHz	7.2 kHz
PM	47 °	30 °	22 °
$I_{3\text{th}}$	17.0 %	11.8 %	8.8 %
$I_{5\text{th}}$	7.1 %	6.0 %	5.3 %
$I_{7\text{th}}$	6.1 %	3.3 %	1.0 %
$I_{9\text{th}}$	1.2 %	2.6 %	2.2 %
$I_{11\text{th}}$	2.2 %	1.9 %	3.0 %
$I_{13\text{th}}$	1.1 %	1.0 %	2.2 %
THD	20.3 %	15.2 %	12.5 %
PF	85.2 %	88.2 %	89.5 %

Finally, for $C_{FZ} = 3.3\text{ nF}$ (first column in Table 4), the integrator gain moves to 25 kHz, and the zero moves to 2.2 kHz. As a result, the phase margin is increased to 47°, while the crossover frequency is decreased to 7.1 kHz. The total harmonic distortions also are increased to 20.3%. A plot of current-loop gains and phases for the three different compensations is shown in Fig. 16.

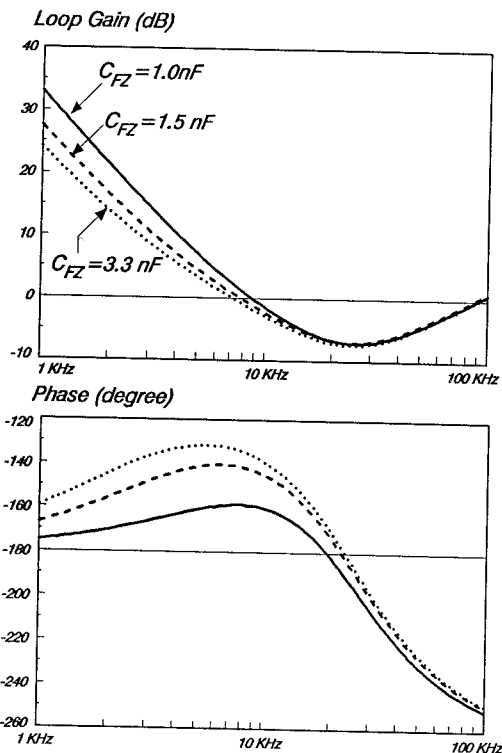


Figure 16. Current-loop gains and phases for three different compensations.

5. Summary

The design trade-offs in the boost power-factor correction (PFC) circuits with peak and average current-mode control are discussed. The effect of the compensation ramp on the input-current distortions is explained. It was shown that a properly added dc offset to the current reference can reduce the distortions. Merits and limitations of a number of approaches in implementing the dc offset are discussed. A simplified expression for the current-loop gain of the boost PFC circuit with average current-mode control is given. A PSPICE program that implements this expression is employed in the design optimization of the current-amplifier compensation.

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