

# Evaluation of Flyback Topologies for Notebook AC/DC Adapter/Charger Applications

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**Abstract** - Design optimization issues for the flyback converter for the next generation of notebook high-power density ac/dc adapters/chargers are discussed. Size, cost, efficiency, and temperature comparisons of a 30-W RCD-clamp and active-clamp flyback power stage with constant-voltage / constant-power / constant-current charging profile are presented. Design trade-offs between the bulk-capacitor and flyback-transformer sizes and the switching frequency and conversion efficiency are also discussed. Finally, design guidelines for an RCD-clamp flyback adapter/charger using a Mathcad-based design optimization software are given.

## I. INTRODUCTION

The ever present trend of reducing the size and weight of the portable data-processing equipment has created new challenges related to the design of their power systems. Specifically, power-density requirements for notebook ac/dc adapters/chargers have changed dramatically in the recent years. While adapters with power densities below 1 W/in.<sup>3</sup> were prevalent a couple of years ago, today's adapters have power densities in the 3-4 W/in.<sup>3</sup> range. Moreover, it is expected that in the near future internal and/or external adapters/chargers with power densities exceeding 6 W/in.<sup>3</sup> will be widely used. In addition, recent advancements in the battery technology have put more stringent requirements on the battery-charging profile (constant-voltage / constant-power / constant-current) [1], resulting in even higher performance expectations of the next generations of notebook ac/dc adapters/chargers.

The notebook ac/dc adapters/chargers are required to operate with extremely high efficiencies because the heat dissipation from adapters is removed by natural convection only. In fact, external adapters are packaged in completely enclosed cases without any vent holes. Besides high efficiencies, power dissipation in adapters should be distributed throughout the adapter packages to avoid creating "hot spots." According to our experience, the efficiency of 30-40 W notebook ac/dc adapters/chargers with 4-6 W/in.<sup>3</sup>

power densities should be between 83 and 86% in the entire ac input voltage range from 90 to 275 V<sub>rms</sub>.

Generally, the notebook ac/dc adapter/charger designs have evolved around the flyback and the forward power stages. Except for higher power (> 45 W) adapters or lower output-voltage (< 7.5 V) adapters, the flyback topology has been almost exclusively used in the adapter/charger applications. Due to a relatively small output power (30-50 W) of adapters/chargers, the power stage optimization cannot be successfully done by using cut-and-try approaches. In fact, at power densities of 6 W/in.<sup>3</sup> and higher, the adapter/charger design becomes a formidable task that can only be accomplished by using analytical-based analysis and design optimization tools. These tools are needed to accurately estimate and optimize component power losses so that the adapter efficiency can be maximized in the entire (universal) line-voltage range, thus allowing high-power density packaging. Recognizing the need for such a design tool, we have developed a Mathcad-based design optimization software, structured so that it allows the designer to observe trends and more trade-offs in order to achieve the desired circuit performance.

The objective of this paper is to present design optimization guidelines for the flyback converter for the next generation of high-power density ac/dc adapters/chargers. Specifically, the evaluation results of the RCD-clamp and active-clamp flyback power stages with constant-voltage/constant-power/constant-current charging profile are discussed. Design trade-offs between the bulk-capacitor and flyback-transformer sizes and the switching frequency and conversion efficiency are also considered. Design guidelines for the RCD-clamp flyback adapter/charger using the Mathcad-based design optimization software are given.

## II. TOPOLOGY EVALUATION

At lower power levels (below 45 W) and higher output voltages (typically above 7.5 V), the flyback topology is the prevalent choice in the

adapter/charger applications because of its low parts count (hence low cost) and good efficiency.

There are two flyback topologies of interest. The flyback converter with RCD clamp is shown in Fig. 1(a), and the flyback converter with active clamp is shown in Figs. 1(b),(c). The active-clamp circuit provides the following benefits [2]:

- recycling of the transformer leakage energy,
- lower turn-off voltage stress on the power switch,
- lower EMI noise due to the “smooth” voltage waveform across the power switch (unlike the drain-to-source voltage waveform in Fig. 6(b), there are no additional voltage spikes, and there is no superimposed high-frequency ringing due to the oscillation between the transformer leakage inductance and the power switch’s capacitance), and
- possibility for achieving zero-voltage-switching (ZVS) for the power switch and subsequent lowering of the output rectifier  $di/dt$ , which results in decreased output switching noise.

However, the active-clamp circuit compared to the RCD-clamp circuit requires an active switch with associated gate drive circuitry instead of a simple clamp diode. The active switch can be either an N-channel MOSFET which needs a pulse transformer for isolation (Fig. 1(b)) or a P-channel MOSFET which can be directly driven when its source is

connected to the supply voltage of the control circuit (Fig. 1(c)). In the PMOS active-clamp circuit a high-voltage capacitor is required instead of the low-voltage capacitor used in the NMOS active-clamp as well as in the RCD-clamp circuit. Furthermore, to achieve ZVS, a resonant inductor usually needs to be added in series with the primary winding. Therefore, if the input and output specifications can be satisfied with the RCD-clamp flyback circuit, noticeable size and cost reductions can be achieved.

The RCD-clamp flyback circuit is well suited to operation at switching frequencies around 100 kHz. With a carefully designed transformer (the leakage inductance less than 1% of the magnetizing inductance) and because of the reverse recovery of the clamp diode that partially emulates the active-clamp effect, as shown in Fig. 5, the power loss due to the leakage inductance of the transformer will be small (below 1% of the output power).

For a flyback converter operating in the wide ac input-voltage range (from 90 to 275  $V_{rms}$ ), the drain-to-source breakdown voltage of the main-switch MOSFET should be  $V_{DSS} \geq 500$  V. With today’s power semiconductor technology, a 600-V MOSFET provides the best compromise regarding low drain-to-source on-resistance (which determines the switch conduction loss) and low inter-electrode capacitances (which determine the switch turn-on and turn-off losses) [3]. A 600-V MOSFET has enough margin for an additional voltage stress during turn-off caused by the RCD-clamp circuit. Therefore, if the temperature of the MOSFET mounted on a small heatsink can be kept below approximately 70°C within the whole range of operation by an optimized PWM design, the employment of active clamp will not significantly benefit the circuit performance.

Finally, if the EMI requirements can also be satisfied with the RCD-clamp circuit by a careful design of the input filter and packaging (e.g. by using a shield or by additional small filter stage), the smaller size and lower cost of the RCD-clamp circuit will be fully taken advantage of.

The benefits of the active-clamp circuit become significant at higher switching frequencies (above 300-500 kHz). Moving to higher switching frequencies is the only way to reduce the size of the transformer which takes up a significant space in a flyback ac/dc adapter/charger. At lower switching frequencies (around 100 kHz), the size of the flyback transformer is typically 25x25x12.5 mm (e.g. EFD25 from Philips [4]). To employ the next lower-size transformer (20x20x10 mm, e.g. EFD20), the switching frequency should be increased several times. Increasing the switching

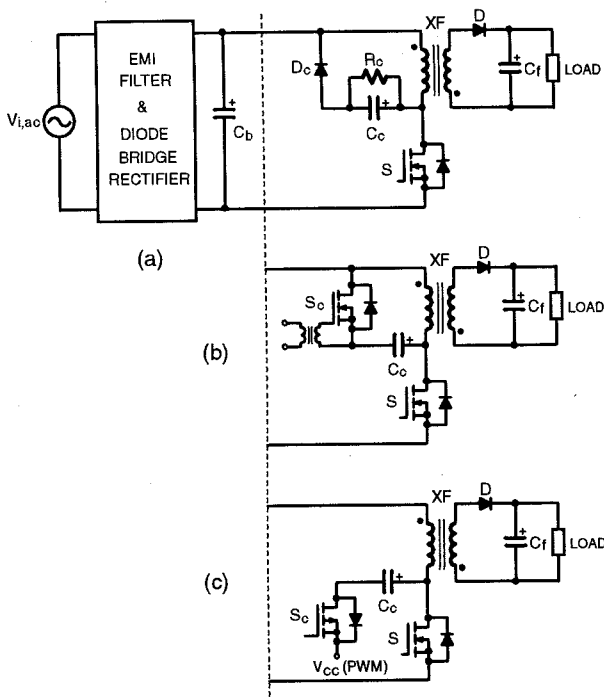


Fig. 1 Simplified circuit diagram of (a) RCD-clamp, (b) NMOS active-clamp, and (c) PMOS active-clamp flyback adapter/charger

frequency in an RCD-clamp converter results in unacceptable increase of switching losses of the power switch. Using the active-clamp which enables lower voltage stress during turn-off and ZVS during turn-on, the switching losses can be significantly decreased. Since with increased switching frequency the leakage inductance loss and the EMI noise proportionally increase, the advantages of the active-clamp circuit can be fully utilized in adapters/chargers operating at switching frequencies well above 100 kHz.

### III. DESIGN CONSIDERATIONS FOR RCD-CLAMP FLYBACK ADAPTER/CHARGER

The RCD-clamp flyback adapter/charger in this paper is designed according to the constant-voltage (CVM) / constant-power (CPM) / constant-current (CIM) charging profile given in Fig. 2. At output voltages below 7 V, the adapter/charger enters the hiccup mode (HM). The ac input voltage range of the adapter/charger is from 90 to 275 V<sub>rms</sub> with the line-frequency range from 47 to 63 Hz.

The circuit is designed around the following key components:

- a 600-V MOSFET,
- Economic Flat Design core EFD25 [4], and
- Schottky diode for secondary-side rectifier.

The switching frequency  $f_{sw} = 100$  kHz is chosen.

#### A. Front End

Besides the power transformer, the bulk capacitor is another large space-consuming component within the flyback adapter/charger. In order to reduce the size of the bulk capacitor, by decreasing its capacitance the minimum instantaneous voltage across the bulk capacitor will also be decreased. The waveforms of the bulk-capacitor voltage and currents, which neglect the

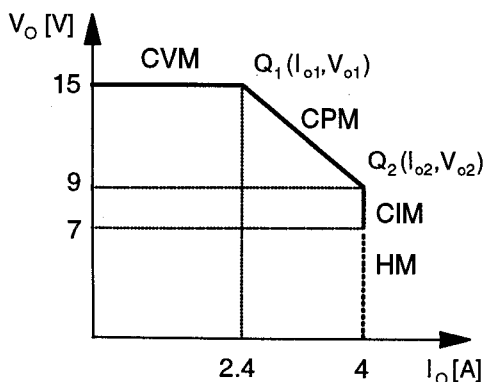


Fig. 2 Notebook ac/dc adapter/charger charging profile

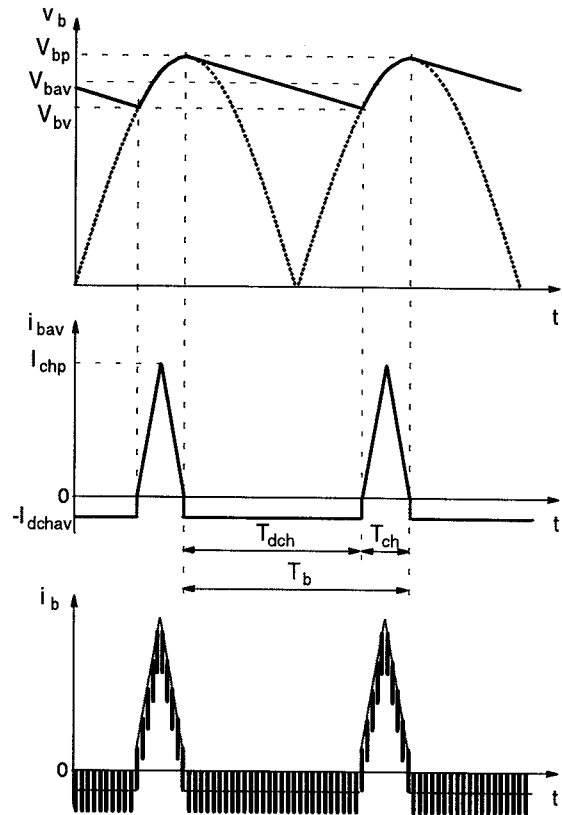


Fig. 3 Bulk-capacitor voltage and current waveforms

effect of the ac mains' inductance and resistance, are shown in Fig. 3. The current  $i_{bav}$  is the average current of the bulk capacitor within a switching cycle when the input current of the dc/dc converter is assumed to be constant. The current  $i_b$  is the instantaneous current of the bulk capacitor when the input current of the dc/dc converter is approximated with rectangular pulses. The relation between minimum bulk-capacitor voltage and bulk capacitance can be expressed as

$$C_b = \frac{P_{o1}}{\eta_{dc/dc} \cdot f_{Lmin} \cdot (V_{bp}^2 - V_{bv}^2)} \cdot \left[ 1 - \frac{1}{\pi} \cdot a \cos \left( \frac{V_{bv}}{V_{bp}} \right) \right], \quad (1)$$

where,  $\eta_{dc/dc}$  is the desired efficiency of the dc/dc converter ( $\eta_{dc/dc} = 0.9$ ), and  $f_{Lmin}$  is the minimum line frequency. The  $C_b$  vs.  $V_{bv}$  diagram at minimum ac input voltage  $V_{i,ac} = 90$  V<sub>rms</sub> is shown in Fig. 4. With decreased bulk capacitance, the dc/dc converter as constant-power load will draw larger average current. Due to the dominant effect of conduction-type losses at lower voltages and higher currents, the efficiency of the ac/dc adapter can significantly deteriorate.

The minimum size of the bulk capacitor is determined by the maximum rms current through

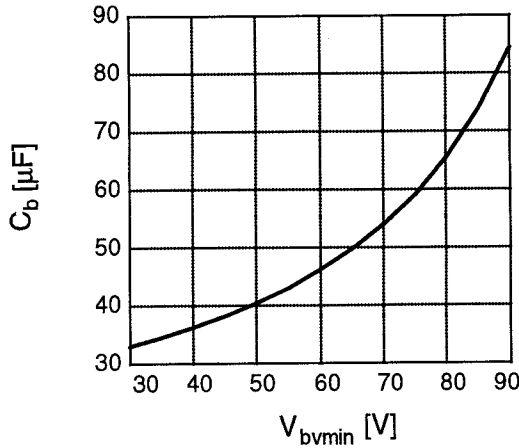


Fig. 4 Bulk capacitance vs minimum bulk-capacitor voltage

the capacitor. Assuming a constant input current of the dc/dc converter, as shown in Fig. 3(b), the rms current through the bulk capacitor can be expressed as

$$I_{bavrms} = \sqrt{\frac{I_{chp}^2}{3} \cdot \frac{T_{ch}}{T_b} + I_{dchav}^2 \cdot \frac{T_b - T_{ch}}{T_b}}, \quad (2)$$

where

$$T_b = \frac{1}{2 \cdot f_{Lmin}}, \quad (3)$$

$$T_{ch} = \frac{\arccos\left(\frac{V_{bv}}{V_{bp}}\right)}{\pi} \cdot T_b, \quad (4)$$

$$I_{chp} = 2 \cdot C_b \cdot \frac{V_{bp} - V_{bv}}{T_{ch}}, \quad (5)$$

and

$$I_{dchav} = \frac{T_{ch}}{T_b - T_{ch}} \cdot \frac{I_{chp}}{2} \quad (6)$$

are the charging-discharging period, charging time, peak charging current, and averaged discharging current, respectively. However, if more accurate approximation of the input current of the dc/dc converter with rectangular pulses is taken, as shown in Fig. 3(c), the rms current of the bulk capacitor is obtained as

$$I_{brms} = \sqrt{\left(\frac{I_{chp}^2}{3} + \frac{1-D_s}{D_s} \cdot I_{dchav}^2\right) \cdot \frac{T_{ch}}{T_b} + \frac{I_{dchav}^2}{D_s} \cdot \frac{T_b - T_{ch}}{T_b}}, \quad (7)$$

where  $D_s$  represents the duty cycle of the rectangular current pulses. For several possible standard capacitances, the values of the charging

TABLE I  
BULK CAPACITOR DESIGN CONSIDERATIONS  
( $V_{iac} = 90$  V<sub>rms</sub>,  $f_{Lmin} = 47$  Hz)

$C_b$ [μF]	$V_{bvmin}$ [V]	$T_{ch}$ [ms]	$I_{chp}$ [A]	$I_{dchav}$ [A]	$I_{bavrms}$ [A]	$I_{brms}$ [A]
33	30	4.45	1.41	0.52	0.66	0.84
47	60	3.59	1.67	0.43	0.66	0.79
56	72	3.08	1.85	0.40	0.69	0.79
68	80	2.90	2.00	0.38	0.70	0.80

time, peak charging current, averaged discharging current, and maximum rms currents are given in Table I. The current  $I_{brms}$  is calculated at  $D_s = 0.5$ . As can be seen, the maximum rms current of the bulk capacitor practically does not depend on the capacitance value in the considered range. The more accurate rms current,  $I_{brms}$ , is about 20% larger than the rms current  $I_{bavrms}$  obtained when the pulsating nature of the dc input current is entirely neglected.

With today's capacitor technology, the 400-V<sub>dc</sub> aluminum electrolytic capacitor is the only capacitor which can be employed as bulk capacitor in the wide input voltage range flyback adapters/chargers. Due to limited size-reduction potential of these capacitors (with reduced surface area, their ESR increases, and thus their current handling capability decreases even more [5]), the two-stage ac/dc adapter/charger topologies may have merits in high power-density adapter/charger applications. In a two-stage approach, the input voltage of the second stage is a constant, high dc-voltage, and the current drawn by the second stage is small. Hence the bulk capacitor, located between the two stages, can be significantly reduced. In addition, if the input stage is a boost-type converter, the input filter size of the adapter/charger may be reduced.

In this paper,  $C_b = 68$  μF is selected for the experimental flyback circuit. As EMI filter a standard Delta EMI filter is used.

## B. DC/DC Converter

The Mathcad-based design procedure includes design of the flyback transformer which has a dominant role, and design of the RCD clamp, secondary-side rectifier diode, and output filter. The design procedure is described below step by step.

**DCM/CCM Boundary:** The boundary between the discontinuous and continuous conduction modes (DCM/CCM) is defined at the boundary of the constant-voltage mode (CVM) and constant-power mode (CPM), denoted as operating point  $Q_1$ .

in Fig. 2. This boundary occurs at some dc input voltage  $V_{bb}$  whose value will be determined from the allowed maximum flux-density excursion and maximum drain-to-source voltage stress. The variables at the DCM/CCM boundary, at the operating point  $Q_1$ , are denoted with the subscript "B".

**Maximum Flux-Density Excursion at DCM/CCM Boundary and Air-Gap Length:** The maximum flux-density excursion,  $B_{1B}$ , and the air-gap length,  $l_g$ , are related to the maximum stored energy,  $W_{1B}$ , in the flyback transformer as

$$W_{1B} = \frac{P_{o1}}{\eta_{dcdc} \cdot f_{sw}} = \frac{1}{2} \cdot \frac{B_{1B}^2}{\mu_o} \cdot \left( l_g + \frac{l_c}{\mu_c} \right), \quad (8)$$

where  $l_c$  denotes the mean magnetic path length, and  $\mu_c$  is the relative permeability of the core material. Selecting  $B_{1B} = 200$  mT, the air gap length will be  $l_g = 0.41$  mm (16 mil), which is below 1% of the effective core length. Also, an additional flux-density region of up to about 50 mT will be available for operation in CCM [4].

**Turns Ratio:** The turns ratio of the transformer can be determined from the maximum allowed drain-to-source voltage stress

$$V_{DSS} = (1 + K_{DS}) \cdot (V_{bmax} + V_{cl}), \quad (9)$$

where  $K_{DS}$  is the drain-to-source voltage safety margin factor ( $K_{DS} = 0.85$  is used),  $V_{bmax}$  is the maximum bulk capacitor voltage ( $V_{bmax} = 385$  V), and  $V_{cl}$  is the clamp voltage, which is typically 20-50% higher than the reflected secondary-side voltage,

$$V_{cl} = K_{cl} \cdot N \cdot (V_{o1} + V_{F1}). \quad (10)$$

Using  $K_{cl} = 1.3$ , and substituting (10) into (9), the turns ratio is

$$N = \frac{\frac{V_{DSS}}{1 + K_{DS}} - V_{bmax}}{K_{cl} \cdot (V_{o1} + V_{F1})} = 6.16. \quad (11)$$

**Duty Cycle at DCM/CCM Boundary:** From Faraday's law:

$$\Delta B_{1B} = B_{1B} = \frac{(V_{o1} + V_{F1}) \cdot (1 - D_{1B})}{N_s \cdot f_{sw} \cdot A_c}, \quad (12)$$

where  $V_{F1}$  is the forward voltage drop on secondary-side rectifier diode ( $V_{F1} = 0.6$  V is assumed),  $D_{1B}$  is the duty cycle at the DCM/CCM boundary voltage,  $V_{bb}$ , in the operating point  $Q_1$ ,  $N_s$  is the number of secondary turns, and  $A_c$  is the core cross-sectional area. For each possible whole

number of secondary turns, the obtained value of the duty cycle  $D_{1B}$  is given in Table II.

**Input DC Voltage at DCM/CCM Boundary:** Using the flux balance relationship, the dc input voltage at the DCM/CCM boundary is obtained as

$$V_{bb} = \frac{N \cdot (V_{o1} + V_{F1}) \cdot (1 - D_{1B})}{D_{1B}}. \quad (13)$$

As can be seen from Table II, increasing the number of secondary turns shifts the DCM/CCM boundary towards higher dc input voltages.

**Number of Primary Turns:** The number of primary turns calculated as  $N_p = N \cdot N_s$  has to be slightly corrected after selection of the appropriate wire gauge in order to fit the whole available length of the bobbin.

**Primary-Side Inductance:** The primary-side inductance is determined as

$$L_p = \frac{\mu_o \cdot A_c}{l_g + \frac{l_c}{\mu_c}} \cdot N_p^2. \quad (14)$$

**Transformer Copper Design:** The transformer copper is designed at maximum output current, at the boundary of the constant power mode (CPM) and constant current mode (CIM), denoted as operating point  $Q_2$  in Fig. 2, at minimum ac input voltage,  $V_{i,ac} = 90$  V<sub>rms</sub>, which yields a minimum line-averaged bulk capacitor voltage (Fig. 3)

$$V_{bminav} = \frac{125 + V_{bvmin}}{2}, \quad (15)$$

where the minimum instantaneous bulk capacitor voltage,  $V_{bvmin}$ , depends on the selected bulk capacitance, as determined in (1). The dc/dc converter operates in CCM with maximum line-averaged duty cycle

$$D_{2maxav} = \frac{N \cdot (V_{o2} + V_{F2})}{V_{bminav} + N \cdot (V_{o2} + V_{F2})}. \quad (16)$$

With  $C_b = 68$   $\mu$ F, the minimum line-averaged bulk capacitor voltage is  $V_{bminav} = 103$  V. The estimated forward voltage drop on the secondary-side rectifier diode at  $I_{o2}$  is  $V_{F2} = 0.7$  V. Having the power and voltage levels, magnetizing inductance and duty-cycle, the primary and secondary current waveforms in CCM can be easily obtained. Limiting the suitable copper dimensions by the skin depth,  $\delta = 0.23$  mm at  $f_{sw} = 100$  kHz and  $T = 70$  °C, and limiting the dc current density below 10 A/mm<sup>2</sup>, the final copper design is performed as presented in Table II.

TABLE II  
SUMMARY OF FLYBACK TRANSFORMER DESIGN  
( $B_{1B} = 200$  mT,  $l_g = 16$  mil)

$N_s$	$D_{1B}$	$V_{bB}$ [V]	$N_p$	$L_p$ [ $\mu$ H]	$D_{2maxav}$	$I_{p2rms}$ [A]	$I_{s2rms}$ [A]	$Cu_p$		$Cu_s$ Foil [mil]	$B_{2max}$ [mT]
								AWG <sub>p</sub>	ST <sub>p</sub>		
6	0.55	77	38	229	0.37	0.71	5.7	31	2	3	208
7	0.48	104	42	312	0.37	0.68	5.5	32	2	3	215
8	0.41	141	50	407	0.37	0.66	5.4	33	2	3	224
9	0.33	193	56	516	0.37	0.66	5.3	28	1	3	245
10	0.26	277	64	637	0.37	0.65	5.3	32	1	3	255

**Maximal Flux Density:** The last column in Table II shows the maximal flux density which occurs at the minimum instantaneous bulk-capacitor voltage  $V_{bmin}$ , at the operating point  $Q_2$ .

**RCD Clamp:** In the first iteration, the RCD clamp is designed according to the power loss during commutation of the magnetizing current from the primary-side clamp-loop to the secondary-side circuit [6]. However, the actual clamp-loss is noticeably lower, due to the reverse recovery of the clamp diode which emulates the active-clamp effect, as shown in Fig. 5. During the clamp-diode reverse recovery, significant part of the charge put into the clamp capacitor during the clamp-diode forward conduction will be moved to the secondary side. The additional loss due to overlapping of the diode current and voltage during reverse recovery reduces the positive effects. The clamp resistance can be chosen from a wide range, *i.e.* from a few 10 k $\Omega$  to above 1 M $\Omega$ . The trade-off between the maximum voltage stress on the MOSFET and the power loss in the clamp circuit is nicely illustrated in

Fig. 5. The final value of the clamp resistance has to be found experimentally.

**Secondary-Side Rectifier Diode:** The maximum voltage stress on the secondary-side rectifier diode is

$$V_{Rmax} = (1 + K_D) \cdot \left( \frac{V_{bmax}}{N} + V_{o1} \right), \quad (17)$$

where  $K_D$  denotes the diode voltage safety-margin factor, necessary because of the additional ringing voltage at the diode turn-off. With a reasonable  $K_D = 0.5$ ,  $V_{Rmax} = 120$  V. The current rating of the diode should be higher than the maximum output current,  $I_{o2} = 4$  A. The IR Schottky rectifier 10CTQ150 ( $V_{RRM} = 150$  V,  $I_{F(AV)} = 10$  A) [7] satisfies both the voltage and current requirements.

**Output Filter:** The output filter is a simple capacitive filter. The asymptotic values of the filter capacitance and ESR are defined for the two extreme cases, when the total voltage ripple is generated only by the ideal capacitor (ESR=0) or by the capacitor's ESR:

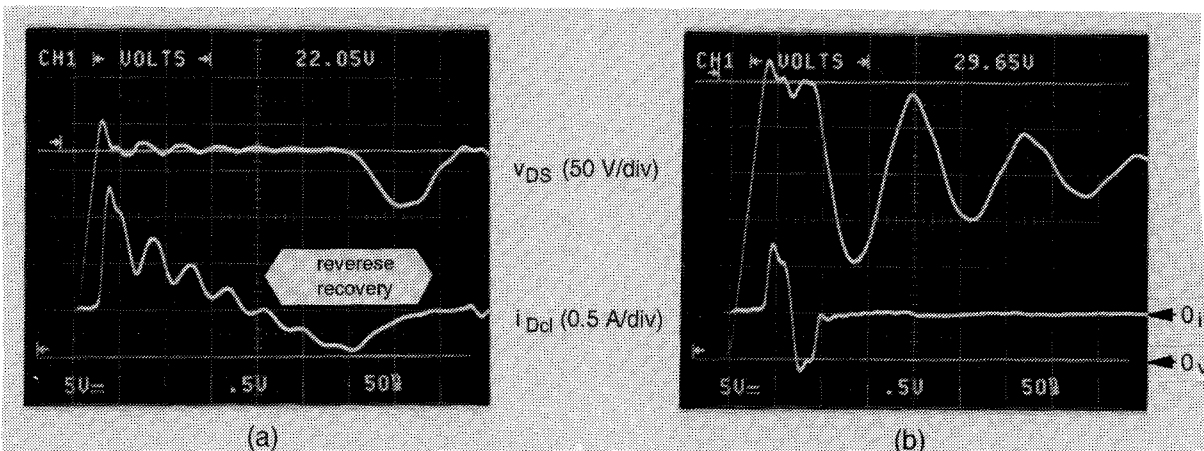


Fig. 5 Emulation of active-clamp effect by clamp-diode reverse recovery at two extreme values of the clamp resistance: (a)  $R_{cl} = 31$  k $\Omega$ , and (b)  $R_{cl} = 2$  M $\Omega$

$$C_{o,asympt} = \frac{I_{o2} \cdot D_{2max}}{\Delta V_{opp} \cdot f_{sw}}, \quad (18)$$

where  $D_{2max}$  is the maximum duty cycle at minimum bulk capacitor voltage,  $V_{bmin}$ , at the operating point  $Q_2$ ,  $\Delta V_{opp}$  is the maximum allowed output voltage ripple ( $\Delta V_{opp} = 200$  mV), and

$$ESR_{Co,asympt} = \frac{\Delta V_{opp}}{I_{s2pmax}}, \quad (19)$$

where  $I_{s2pmax}$  is the maximum peak value of the secondary current at minimum bulk-capacitor voltage, at the operating point  $Q_2$ . The actual values of the output filter capacitance and ESR should be selected as  $C_o > C_{o,asympt}$  and  $ESR_{Co} < ESR_{Co,asympt}$ . Usually the capacitor's ESR has the dominant role. The output filter capacitor is implemented by a 220  $\mu$ F aluminum electrolytic capacitor and a 100  $\mu$ F aluminum solid OSCON capacitor in parallel.

### C. Loss Analysis

In Table II, five different designs related to the selection of the DCM/CCM boundary are presented. The converter operates in CCM at dc input voltages ranging from  $V_{bmin}$  to  $V_{bB}$ , and in DCM at voltages from  $V_{bB}$  to  $V_{bmax}$ . As can be seen from Table II, by increasing the number of secondary turns, the DCM/CCM boundary is shifted towards higher dc input voltages, and the circuit will operate in CCM in wider input voltage range. To determine the optimum DCM/CCM boundary, a detailed loss analysis has to be performed at different DCM/CCM boundaries.

The Mathcad-based design optimization software calculates the following loss components:

- transformer core and copper losses,
- RCD-clamp loss,
- MOSFET conduction and switching losses,
- secondary-side rectifier loss,
- output filter loss,
- control circuit and start-up resistor losses, and
- primary and secondary-side current-sense resistor losses.

By increasing the DCM/CCM boundary voltage  $V_{bB}$ , most of the loss components (transformer core loss, clamp loss, MOSFET conduction and switching losses, output filter loss, primary and secondary-side current-sense resistor losses) will decrease; the secondary-side rectifier loss, and the control circuit and start-up resistor losses remain constant; only the transformer copper loss will increase. At higher input voltages the total power loss monotonically decreases. At lower input voltages the increasing copper loss may dominate the other decreasing losses at higher  $V_{bB}$  voltages. All in all, the optimum design should be close to the highest possible  $V_{bB}$  voltage, *i.e.* the largest possible number of secondary turns.

## IV. EXPERIMENTAL RESULTS

Measurement results obtained on two experimental setups are presented. The first setup was built according to the design procedure described in the previous chapter. The second setup, originally designed as active-clamp flyback adapter/charger at 90-kHz switching frequency, is used for experimental comparison of the flyback adapter/ charger circuit with active and RCD clamp.

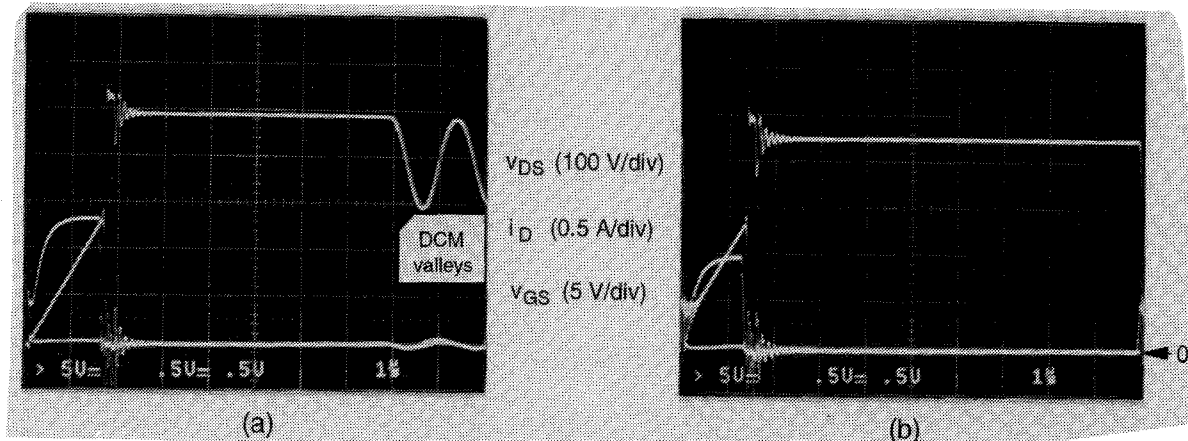


Fig. 6 Primary-side experimental waveforms at  $V_{i,dc} = 385$  V at the operating point (a)  $Q_1$  and (b)  $Q_2$ , measured in the circuit with the transformer designed for  $V_{bB} = 141$  V

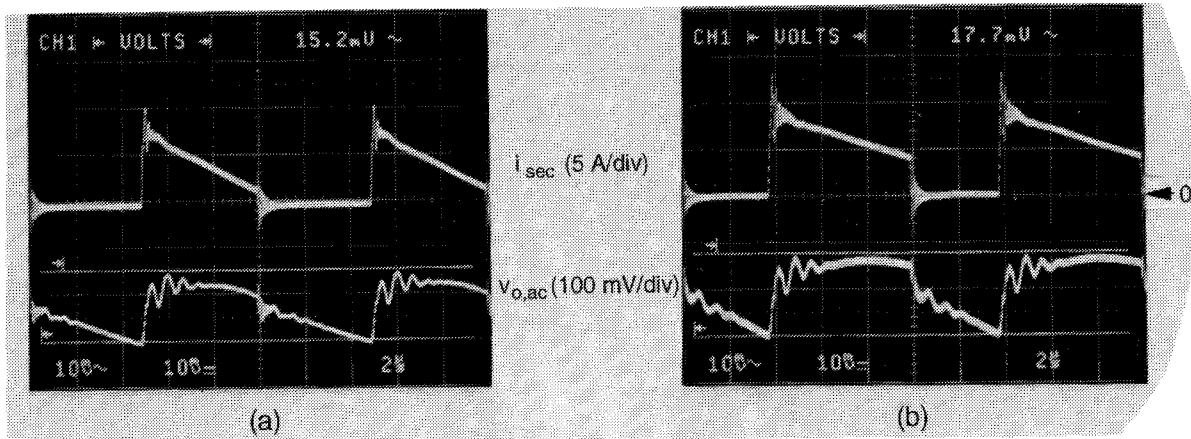


Fig. 7 Secondary-side experimental waveforms at  $V_{i,dc} = 103$  V at the operating point (a)  $Q_1$  and (b)  $Q_2$ , measured in the circuit with the transformer designed for  $V_{bB} = 141$  V

### A. Optimized RCD-Clamp Flyback Adapter/Charger

The optimized RCD-clamp flyback adapter/charger was built according to the charging profile given in Fig. 2. Besides the 600-V MOSFET and the EFD25 transformer, the basic characteristics of the circuit are:

- active start-up,
- CMOS PWM controller in current mode control,
- four secondary-side rectifier diodes in parallel (it was experimentally found that a single secondary winding with Cu-foil and four diodes in parallel is superior to four secondary windings with Cu-wire, each winding connected to a diode),
- output filter with low ESR aluminum solid OSCON capacitor,
- output current-sense resistor: 10 m $\Omega$ .

Experimental waveforms of the gate-to-source voltage, drain-to-source voltage, and drain current at both operating points,  $Q_1$  and  $Q_2$ , at maximum

dc input voltage ( $V_{bmax} = 385$  V) measured in the circuit with the transformer designed for  $V_{bB} = 141$  V are shown in Fig. 6. As can be seen, at  $Q_1$  the circuit operates in DCM, the maximum value of the drain-to-source voltage is about 550 V. At  $Q_2$ , the circuit operates entirely in CCM, the maximum voltage stress on the MOSFET is reduced due to the lower output voltage.

Experimental waveforms of the secondary-side diode current and output voltage ripple at  $Q_1$  and  $Q_2$ , at minimum line-averaged dc input voltage ( $V_{bminav} = 103$  V), are shown in Fig. 7. The maximum output voltage ripple is below 200 mV.

Three different transformers were built and employed in the same adapter/charger circuit for efficiency and temperature measurements. The three DCM/CCM boundary voltages selected for comparison are  $V_{bB} = 77$  V, 141 V, and 277 V. Efficiency measurement results are presented in Fig. 8, and temperature measurement results are given in Table III.

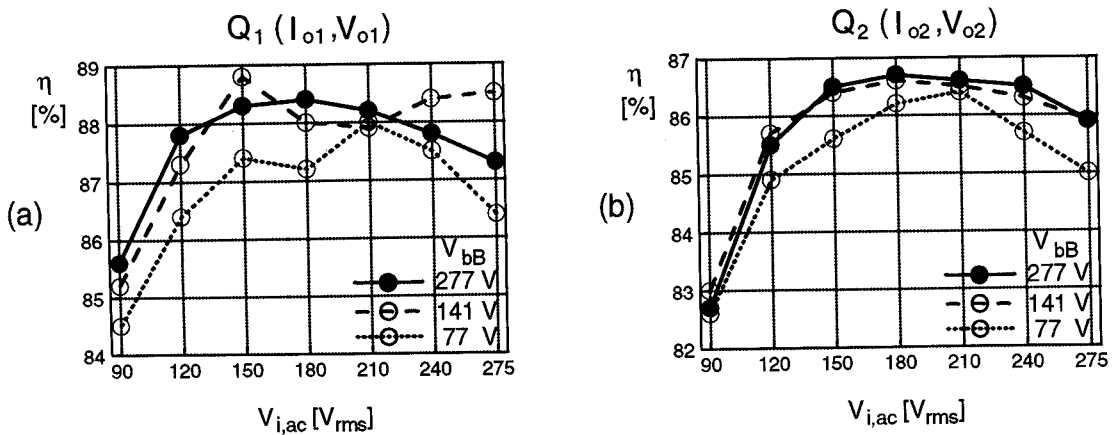


Fig. 8 Efficiency measurement results at the operating point (a)  $Q_1$  and (b)  $Q_2$  obtained on setup 1

TABLE III  
TEMPERATURE MEASUREMENT RESULTS (SETUP 1)

Operating Point	$V_{bB}$ [V] $V_{i,ac}$ [V <sub>rms</sub> ]	$T(S)$ [°C]			$T(D)$ [°C]			$T(XF_{Cu})$ [°C]			$T(XF_{Fe})$ [°C]		
		77	141	277	77	141	277	77	141	277	77	141	277
$Q_1$ (2.4 A, 15 V)	90	55	54	49	57	55	55	53	54	54	51	48	47
	120	55	55	49	57	56	55	54	56	54	52	51	47
	150	<b>52</b>	<b>45</b>	50	57	56	54	54	54	54	52	52	47
	180	58	57	53	58	56	54	55	56	54	53	52	47
	210	<b>51</b>	60	57	57	56	54	53	57	56	53	52	49
	240	<b>58</b>	<b>54</b>	60	58	56	54	55	55	56	53	53	50
	275	71	<b>53</b>	65	59	56	56	57	56	57	55	53	52
$Q_2$ (4 A, 9 V)	90	58	56	51	73	72	72	59	61	62	53	50	50
	120	55	53	48	72	70	71	58	59	59	53	51	51
	150	56	55	50	72	70	70	58	59	59	53	52	51
	180	<b>52</b>	56	50	72	70	69	58	58	58	54	52	51
	210	<b>51</b>	61	54	72	70	69	58	59	59	54	53	51
	240	61	65	58	72	69	69	59	59	59	55	53	52
	275	69	70	61	72	69	69	59	60	90	56	54	52

As can be seen from Fig. 8, the 277-V design has the highest overall efficiency. The 141-V design has only slightly lower efficiency. At the operating point  $Q_1$ , the 141-V design has even higher efficiency at two distinct ranges of the ac input voltage. This can be explained by the operation of the circuit in DCM when the MOSFET turns on at the valley of the ringing drain-to-source voltage, which noticeably reduces the MOSFET switching losses at these input voltages. This effect can be also seen from the temperature measurements in Table III, as well as from the drain-to-source voltage waveform in Fig. 8(a). The temperature of the MOSFET in the 141-V design does not rise monotonically with the increase of the ac input voltage, but it drops suddenly around 150 V<sub>rms</sub> and in the region between 240 and 275 V<sub>rms</sub> input voltage. The drain-to-source voltage waveform in DCM has two valleys. In the most critical operating point,  $Q_2$ , at minimum ac input voltage, the three designs differ in efficiency by less than 0.5%.

For the most part, the temperature measurement results well agree with the theoretical predictions. The temperature of the MOSFET monotonically rises with increasing input voltage, except at DCM valleys (marked in bold and italics in Table III), showing the dominance of the switching losses; only at  $Q_2$  at the low end of the ac input voltage the MOSFET temperature increases

in the opposite direction, due to the prevailing conduction loss. With increasing DCM/CCM boundary voltage  $V_{bB}$ , the MOSFET temperature sinks in both operating points (except at the DCM valleys). The 277-V design has the lowest maximum MOSFET temperature.

The copper temperature is much more balanced in both operating points. Hence, the copper temperature cannot have significant influence on the optimized design. The core temperature measurement results correspond well with the theoretical predictions. The core temperature slightly decreases with increasing DCM/CCM boundary voltage and lightly increases with rising input voltage. The temperature of the transformer is always below 60°C.

The temperature of the secondary-side rectifier diode is well balanced. By decreasing the DCM/CCM boundary voltage  $V_{bB}$ , the diode temperature increases only very slightly, due to the nonlinearity of its V-I characteristic at lower currents as in DCM.

The maximum temperature of the diode bridge rectifier and EMI filter is below 60°C.

To summarize, when each particular design is optimized for a given number of secondary turns, the final design should be selected according to the temperature distribution; the efficiency is not essential any more. In spite of the benefits of the DCM valleys at lower  $V_{bB}$  voltages, the circuit will

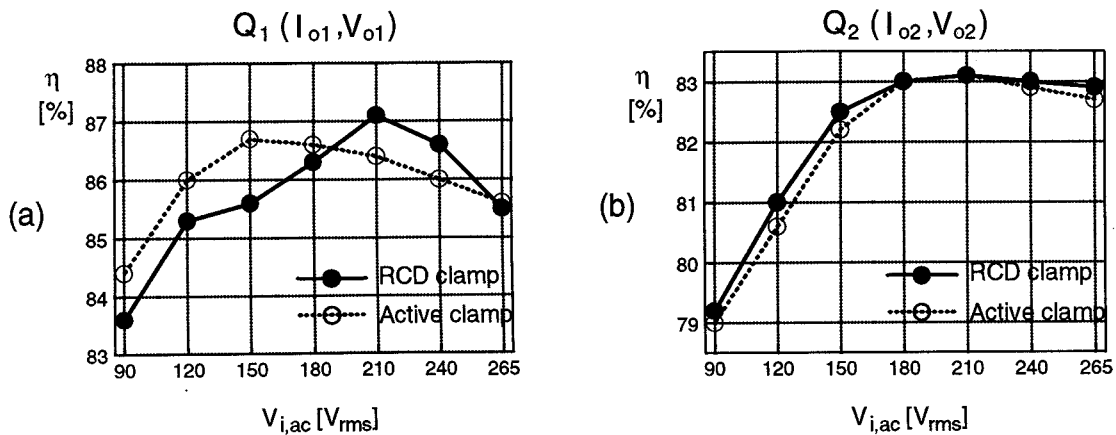


Fig. 9 Efficiency measurement results at the operating point (a)  $Q_1$  and (b)  $Q_2$  obtained on setup 2

exhibit the most balanced temperature distribution at the highest possible DCM/CCM boundary voltage, *i.e.* the largest possible number of secondary turns.

#### B. RCD-Clamp vs. Active-Clamp Flyback Adapter/Charger

For experimental comparison of the RCD-clamp and active-clamp flyback adapterschargers at lower switching frequencies, a 30-W adapter/charger was used, originally designed as PMOS active-clamp flyback circuit with ZVS for the following charging profile (see Fig. 2):  $(I_{o1}, V_{o1}) = (1.62 \text{ A}, 18.5 \text{ V})$  and  $(I_{o2}, V_{o2}) = (3 \text{ A}, 10 \text{ V})$ . The

main power components are the same as in the first experimental setup. A 500-V PMOSFET ( $R_{DSon} = 6 \Omega$ ) from Motorola [3] is employed as clamp switch. Both the main and the clamp switches are mounted on heatsinks of the same small size. The switching frequency is 90 kHz. The RCD-clamp mode (RCM) is obtained by simple replacement of the active-clamp circuit with the same RCD circuit as the one used in the first setup. In the active-clamp mode (ACM), the circuit is adjusted to operate with ZVS at the CVM/CPM boundary (operating point  $Q_1$ ), but to loose ZVS at the CPM/CIM boundary (operating point  $Q_2$ ). Efficiency measurement results are presented in Fig. 9, and temperature measurement results are

TABLE IV  
TEMPERATURE MEASUREMENT RESULTS (SETUP 2)

Flyback Circuit with		RCD-Clamp				Active-Clamp				
Operating Point	$V_{i,ac}$ [V <sub>rms</sub> ]	$T(S)$ [°C]	$T(D)$ [°C]	$T(XF_{Cu})$ [°C]	$T(XF_{Fe})$ [°C]	$T(S_1)$ [°C]	$T(S_2)$ [°C]	$T(D)$ [°C]	$T(XF_{Cu})$ [°C]	$T(XF_{Fe})$ [°C]
$Q_1$ (1.62 A, 18.5 V)	90	60	59	72	67	55	49	57	65	63
	120	56	56	70	66	49	49	56	66	65
	150	61	56	70	67	47	49	56	68	68
	180	59	56	70	67	48	51	57	71	71
	210	54	57	69	66	49	53	58	73	75
	240	58	56	70	67	48	55	59	76	77
265	67	56	71	69	50	57	60	78	80	
$Q_2$ (3 A, 10 V)	90	74	72	80	72	85	55	72	75	72
	120	74	74	82	75	86	55	71	77	74
	150	69	72	78	72	80	54	69	74	73
	180	68	71	78	72	78	53	68	74	73
	210	70	72	79	73	78	51	67	73	74
	240	70	71	79	72	79	52	67	73	73
265	73	73	81	76	81	52	67	74	74	

given in Table IV.

As can be seen, with ZVS the efficiency in ACM is only slightly higher than the efficiency in RCM. In addition, at higher ac input voltages, the efficiency in RCM prevails, due to the drain-to-source voltage valley in DCM operation. Without ZVS in  $Q_2$ , the efficiency in ACM is below the efficiency in RCM in the whole ac input voltage range. In  $Q_1$ , the temperature of the RCM MOSFET is noticeably higher than the temperature of the corresponding ACM MOSFET, but it never rises above 70°C, as shown in Table IV. However, in ACM, the clamp switch significantly contributes to the total losses (notice that the temperatures of the main switch and the clamp switch are about the same). This is due to the high  $R_{DSon}$  of the PMOSFET which is significantly higher than the  $R_{DSon}$  of the NMOSFET. Without ZVS in  $Q_2$ , the temperature of the NMOSFET in ACM becomes higher than in RCM. This can be explained by operation of the RCM circuit in DCM. The other loss components in RCM and ACM are more balanced.

The efficiency and temperature measurement results verify the evaluation of the RCD-clamp and active-clamp flyback topologies presented in chapter II and confirm that the employment of active clamp at switching frequencies around 100 kHz will not significantly benefit the adapter/charger performance.

## V. SUMMARY

High power-density requirements (above 6 W/in.<sup>3</sup>) for next generation of notebook ac/dc adapters/chargers demand operation with extremely high efficiencies because the heat dissipation from adapters is removed by natural convection only. Besides high efficiencies, power dissipation in adapters should be distributed throughout the adapter packages to avoid creating "hot spots." To maximize adapter efficiency in the entire (universal) line-voltage range and to accurately estimate component power losses, the adapter/charger design can only be accomplished by using analytical-based analysis and design optimization tools. Recognizing the need for such a design tool, we have developed a Mathcad-based design optimization software, structured so that it allows the designer to observe trends and more trade-offs in order to achieve the desired circuit performance.

At lower power levels (below 45 W) and higher output voltages (typically above 7.5 V), the flyback topology is the prevalent choice in the adapter/charger applications because of its low parts count (hence low cost) and good efficiency.

At lower switching frequencies (around 100 kHz), the RCD-clamp flyback converter is the best choice. Efficiency and temperature comparisons of a 30-W RCD-clamp and active-clamp flyback power stage with constant-voltage / constant-power / constant-current charging profile, operating at 90-kHz switching frequency, have shown that the RCD-clamp circuit has only slightly lower efficiency than the active-clamp circuit in the whole ac input voltage range, and that the power dissipation of the RCD-clamp circuit is also well balanced. At higher ac input voltages, the efficiency of the RCD-clamp circuit may even prevail, due to operation in DCM. Therefore, the smaller size and lower cost of the RCD-clamp flyback adapter/charger are fully advantageous at lower switching frequencies.

The benefits of the active-clamp flyback circuit can be entirely utilized in adapters/chargers operating at higher switching frequencies (above 300-500 kHz), at which a significant size reduction of the flyback transformer is possible.

Besides the power transformer, the bulk capacitor is another large space-consuming component. Trade-offs between the bulk-capacitor size and conversion efficiency are also discussed.

Finally, the paper provides design guidelines for the RCD-clamp flyback adapter/charger using the Mathcad-based design optimization software. For different whole numbers of secondary turns related to the DCM/CCM boundary, particular designs with highest efficiency are obtained. The final design is selected according to the temperature, *i.e.* power loss distribution. It is expectable that the highest possible DCM/CCM boundary voltage, *i.e.* the largest possible number of secondary turns will yield the most balanced power loss distribution. The design procedure is experimentally verified.

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