

# Analysis, Design, and Performance Evaluation of Clamped-Current Boost Input-Current Shaper for Universal Input-Voltage-Range Applications

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**Abstract** - In cost-sensitive, off-line applications, compliance with existing line-current harmonic standards can be achieved by employing clamped-current boost (CCB) input-current shapers (ICSs). In this paper, a thorough analysis of the CCB ICS is presented, and a complete design-oriented mathematical model is derived. The model is verified experimentally on a 100-W, universal input-voltage-range ICS.

## I. INTRODUCTION

As it has been demonstrated in [1]-[4], various power-quality standards, such as IEC 1000-3-2 [5], can be met by line-current shapers that are substantially different from sinusoidal. A trapezoidal waveshaper is particularly attractive due to its potential to achieve high power factor (PF) with low peak-to-rms ratio (crest factor) and relatively low total harmonic distortions (THDs) [1]. In [1]-[4], trapezoidal-waveshape approaches are exploited in implementing various simple, low-cost, boost input-current shapers (ICSs). These ICSs, also known as clamped-current boost (CCB) ICSs [2]-[4], do not require dedicated ICS controllers. Instead, any conventional current-mode PWM controller chip can be used to control CCB ICSs.

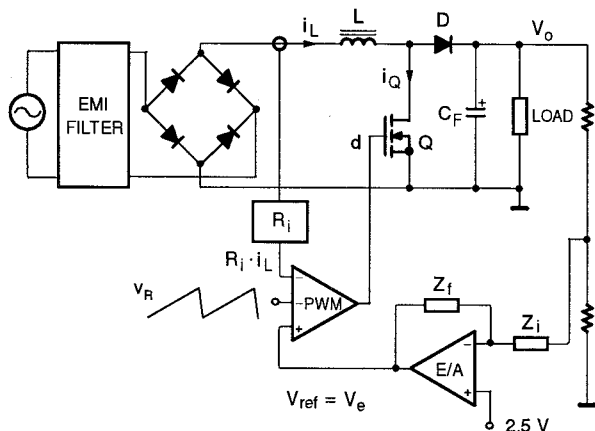


Fig. 1 Conceptual circuit diagram of CCB ICS

The conceptual circuit diagram of the CCB ICS is shown in Fig. 1. In this circuit, the PWM modulator compares the difference between reference voltage  $V_{ref}$  and slope-compensation ramp  $v_R$  (used to stabilize the current loop for duty cycles  $> 50\%$ ) with the voltage on sensing resistor  $R_i$  which is proportional to inductor current  $i_L$ . It should be noted that in the CCB ICS, reference voltage  $V_{ref}$  is not derived from the rectified line voltage, but it is equal to the output voltage of the error amplifier,  $V_e$ . Since for ICSs the cross-over frequency of the voltage-regulation loop is much lower (typically 4 to 8 times) than twice the line frequency [6], the output voltage of the error amplifier is practically constant during a half line cycle. As a result, the peak inductor current is limited (clamped) by constant reference  $V_{ref}$ , which makes the input current roughly trapezoidal. Note that in practical circuits, sensing of inductor current  $i_L$  is implemented by sensing the switch current,  $i_Q$ , since during on time,  $i_L = i_Q$ .

So far, a number of papers have been published dealing with the analysis and design of the CCB ICSs. In [2], detailed analysis of the CCB ICS is performed for the circuit operating with maximum duty cycle  $\leq 0.5$  and without external ramp. A simplified analysis and design guidelines for the CCB ICS operating with maximum duty cycle close to 100% and external ramp is discussed in [3]. Finally, in [4] the average-current control scheme for the CCB ICSs is proposed.

The objective of this paper is to present a complete, design-oriented analysis of the clamped-current control for CCB ICSs by extending the analysis given in [3] to include the effects of the boost inductance, switching frequency, and maximum duty cycle of the controller. The design equations that include all these effects are derived in closed forms so that they can easily be computed by any standard mathematical software, thus making it possible for design engineers to apply the given design equations to their own set of design specifications. The presented mathematical

model of and design procedure for the CCB ICS are experimentally verified on a universal input-voltage-range, 100-W prototype converter.

## II. ANALYSIS

In this section, the analysis of the CCB ICS shown in Fig. 1 is performed assuming that:

- input voltage is a full-wave rectified sine wave, i.e.,  $v_i = V_{im} |\sin(\omega_L t)|$ , where  $V_{im}$  is the amplitude and  $\omega_L$  is the angular frequency;
- dc output voltage  $V_o$  has negligible ac ripple;
- switching frequency  $f_s$  is constant and much higher than line frequency  $f_L$ , so that the input voltage can be considered constant during a switching cycle (quasi-static approach);

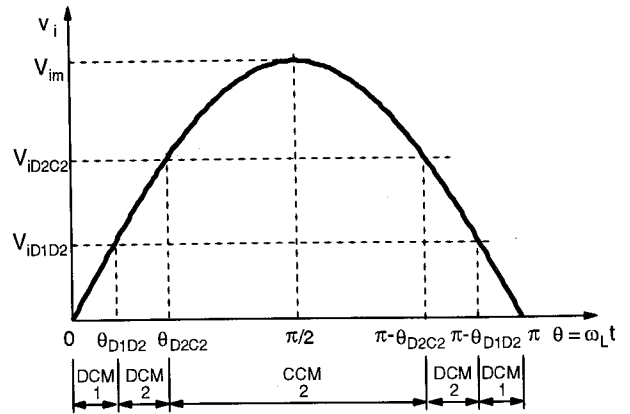


Fig. 3 CCB ICS operation modes

- reference voltage  $V_{ref}$  to the PWM modulator is constant during each half of a line cycle, because the bandwidth of the output-voltage loop is much smaller than the rectified line frequency ( $2f_L$ );
- phase-shift of the line current caused by the input filter can be neglected.

In the CCB ICS in Fig. 1, the conduction of switch Q is initiated by the internal oscillator of the controller (not shown in Fig. 1). The switch is turned off either when sensed voltage  $R_i i_L$  reaches the difference between reference voltage  $V_{ref} = V_e$  and slope-compensation-ramp voltage  $v_R$ , i.e.,

$$R_i \cdot i_L = V_{ref} - v_R, \quad (1)$$

as shown in Fig. 2(a), or when the duty cycle of the switch reaches its preset maximum  $D_{max}$ , as illustrated in Fig. 2(b).

Within a half line cycle the boost inductor can operate in both discontinuous-conduction mode (DCM) and continuous-conduction mode (CCM). At lower instantaneous line voltages, the boost-inductor current,  $i_L$ , is discontinuous, while at higher line voltages  $i_L$  is continuous. Depending on which event terminates the conduction of Q in a switching cycle, two discontinuous and two continuous conduction modes of operation are possible. In this paper, the DCM and CCM where Q turns off when the switch duty ratio reaches its maximum value (Fig. 2(b)) are denoted as DCM1 and CCM1, respectively. Similarly, the DCM and CCM in which sensed voltage  $R_i i_L$  reaches the difference of the reference voltage and slope-compensation-ramp voltage (Fig. 2(a)) are denoted as DCM2 and CCM2, respectively. From the two CCMs only CCM2 needs to be considered since CCM1 usually encompasses only a few switching cycles with fast rising or falling edges of the inductor current which can be approximated with

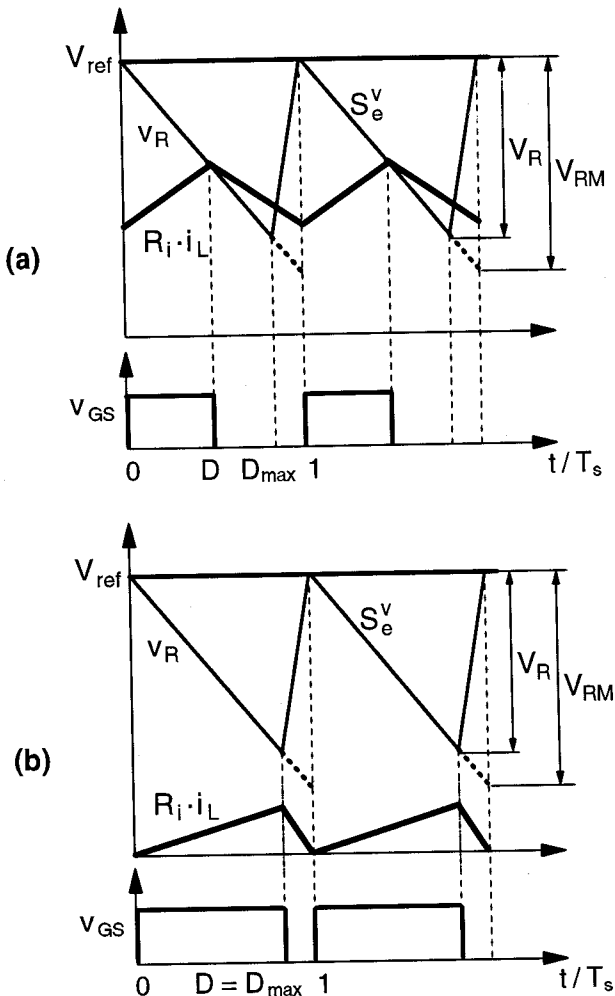


Fig. 2 Reference voltage,  $V_{ref}$ , slope-compensation-ramp,  $v_R$ , sensed voltage,  $R_i i_L$ , and duty cycle of CCB ICS:  
(a) switch turns off when  $R_i i_L$  reaches  $V_{ref} - v_R$ ;  
(b) switch turns off when duty cycle  $D$  reaches  $D_{max}$ .

TABLE I  
CCB ICS MODE SEQUENCES

MODE SEQUENCE	OPERATION MODE			MS CONDITION	BOUNDARY ANGLE	
	DCM1	DCM2	CCM2		$\theta_{DD}$	$\theta_{DC}$
MS1	+		+	$V_{ref} - V_R > R_L \cdot \dot{i}_{L,pk,DCM1,max}$ (See Eq. (14))	$\theta_{D1C2}$	$\theta_{D1C2}$
MS2	+	+	+	$0 < V_{ref} - V_R < R_L \cdot \dot{i}_{L,pk,DCM1,max}$	$\theta_{D1D2}$	$\theta_{D2C2}$
MS3		+	+	$V_{ref} - V_R < 0$	0	$\theta_{D2C2}$

vertical segments, as illustrated in Fig. 6(a). The three operation modes within a half of a line cycle are shown in Fig. 3. Depending on the line and load conditions, three Mode Sequences (MSs) can be distinguished, as summarized in Table I.

In MS1, there is a direct transition from DCM1 to CCM2. In DCM1 ( $D = D_{max}$ ), the peak sensed voltage  $R_L \cdot \dot{i}_L$  is always less than the difference of reference voltage  $V_{ref}$  and peak slope-compensation-ramp voltage  $V_R$  (see Fig. 2(b)). MS3 is without DCM1, i.e. the peak sensed voltage always reaches the difference of the reference voltage and the slope-compensation-ramp voltage,  $V_{ref} - V_R$ . By inspection of Fig. 2(b), it can be easily found that the condition for MS3 is:  $V_{ref} - V_R \leq 0$ . Finally, MS2 is the Mode Sequence between MS1 and MS3.

Expressions of the inductor current waveforms in the three operation modes as well as expressions for the boundary angles between the operation modes are derived next. Since it is more convenient to perform these derivations by using current signals instead of voltage signals, reference current  $I_{ref}$  and slope-compensation-ramp current  $i_R$  are defined from (1) as

$$\dot{i}_L = \frac{V_{ref}}{R_i} - \frac{V_R}{R_i} = I_{ref} - i_R \quad (2)$$

To obtain the expressions for inductor current waveforms and boundary angles, the slope of the compensation ramp must be determined first.

### A. Slope-Compensation Ramp

To ensure the stability of the current loop, the slope of the compensation (external) ramp,  $S_e^i$ , should be at least 50% of the maximum down slope of the inductor current in CCM2,  $S_{f,max}^i$ , i.e.,

$$S_e^i = k_S \cdot S_{f,max}^i, \quad k_S \geq 0.5 \quad (3)$$

From Fig. 2(a) and (2), the slope of the compensation ramp is

$$S_e^i = \frac{I_R}{D_{max} T_s} = \frac{I_{RM}}{T_s} \quad (4)$$

Since the inductor current in CCM2 has maximum down slope at the DCM1-CCM2 boundary,

$$S_{f,max}^i = \frac{V_o - V_{ID1C2}}{L} \quad (5)$$

where the input voltage at the DCM1-CCM2 boundary is

$$V_{ID1C2} = (1 - D_{max}) \cdot V_o \quad (6)$$

substituting (6) into (5) and using (3), the slope of the compensation ramp is determined as

$$S_e^i = k_S \cdot \frac{D_{max} \cdot V_o}{L} \quad (7)$$

Finally, from (4) and (7), the amplitude of the compensation ramp,  $I_{RM} = V_{RM}/R_i$ , is obtained as

$$I_{RM} = k_S \cdot \frac{D_{max} \cdot V_o}{L \cdot f_s} \quad (8)$$

where  $f_s = 1/T_s$ .

### B. Discontinuous Conduction Mode

In DCM, the average inductor current, which is also the line current, is defined as

$$i_{L,ave,DCM} = \frac{T_{on} + T'_{off}}{2 \cdot T_s} \cdot i_{L,pk,DCM} \quad (9)$$

where  $T'_{off}$  is the time which takes the inductor current to decrease from  $i_{L,pk,DCM}$  to zero, and  $i_{L,pk,DCM}$  is the peak inductor current,

$$i_{L,pk,DCM} = \frac{V_{im} \cdot |\sin(\omega_L t)|}{L \cdot f_s} \cdot D_{DCM} \quad (10)$$

where  $D_{DCM} = T_{on}/T_s$ .  $T'_{off}$  is determined from the inductor flux balance as

$$T'_{off} = \frac{V_{im} \cdot |\sin(\omega_L t)|}{V_o - V_{im} \cdot |\sin(\omega_L t)|} \cdot T_{on} \quad (11)$$

Substituting (10) and (11) into (9), the average inductor current in DCM is obtained as

$$i_{L,ave,DCM} = \frac{1}{2Lf_s} \cdot \frac{V_{im} \cdot |\sin(\omega_L t)|}{1 - \frac{V_{im} \cdot |\sin(\omega_L t)|}{V_o}} \cdot D_{DCM}^2 \quad (12)$$

In DCM1,  $D_{DCM} = D_{max}$  and (12) becomes

$$i_{L,ave,DCM1} = \frac{1}{2Lf_s} \cdot \frac{V_{im} \cdot |\sin(\omega_L t)|}{1 - \frac{V_{im} \cdot |\sin(\omega_L t)|}{V_o}} \cdot D_{max}^2 \quad (13)$$

It should be noted that at low line voltages,  $V_{im} \cdot |\sin(\omega_L t)| \ll V_o$ , the average inductor current in DCM1 is proportional to the line voltage.

The maximum value of the peak inductor current in DCM1, which determines the condition for MS1 is obtained by setting  $D_{DCM} = D_{max}$  and by substituting (6) for the instantaneous rectified line voltage,  $V_{im} \cdot |\sin(\omega_L t)|$ , in (10),

$$i_{L,pk,DCM1,max} = \frac{D_{max}(1 - D_{max}) \cdot V_o}{L \cdot f_s} \quad (14)$$

In DCM2, the inductor current reaches the difference of the reference current and ramp current, i.e.,

$$i_{L,pk,DCM2} = I_{ref} - I_{RM} \cdot D_{DCM2} \quad (15)$$

From (10) and (15),

$$D_{DCM2} = \frac{I_{ref}}{I_{RM} + \frac{V_{im} \cdot |\sin(\omega_L t)|}{L \cdot f_s}} \quad (16)$$

and substituting (16) into (12), the average inductor current in DCM2 is obtained as

$$i_{L,ave,DCM2} = \frac{1}{2Lf_s} \cdot \left( \frac{I_{ref}}{I_{RM}} \right)^2 \cdot \frac{V_{im} \cdot |\sin(\omega_L t)|}{\left( 1 - \frac{V_{im} \cdot |\sin(\omega_L t)|}{V_o} \right) \cdot \left( 1 + \frac{V_{im} \cdot |\sin(\omega_L t)|}{I_{RM} L f_s} \right)^2} \quad (17)$$

Again, at low line voltages,  $V_{im} \cdot |\sin(\omega_L t)| \ll V_o$  and  $V_{im} \cdot |\sin(\omega_L t)| \ll I_{RM} L f_s = k_S D_{max} V_o$  (according

to (8)), the average inductor current in DCM2 is proportional to the line voltage.

### C. Continuous Conduction Mode

In CCM2, the average inductor current is defined as

$$i_{L,ave,CCM2} = I_{L,pk,CCM2} - \frac{\Delta i_{L,CCM2}}{2} \quad (18)$$

where

$$I_{L,pk,CCM2} = I_{ref} - I_{RM} \cdot D_{CCM2} \quad (19)$$

is the peak inductor current, and  $\Delta i_{L,CCM2}$  is the peak-to-peak inductor-current ripple,

$$\Delta i_{L,CCM2} = \frac{V_{im} \cdot |\sin(\omega_L t)|}{L \cdot f_s} \cdot D_{CCM2} \quad (20)$$

From the inductor flux balance, the switch duty ratio is determined as

$$D_{CCM2} = 1 - \frac{V_{im} \cdot |\sin(\omega_L t)|}{V_o} \quad (21)$$

Substituting (19)-(21) into (18), the average inductor current in CCM is obtained as

$$\begin{aligned} i_{L,ave,CCM2} &= I_{ref} - I_{RM} \\ &+ \left( \frac{I_{RM}}{V_o} - \frac{1}{2Lf_s} \right) \cdot V_{im} \cdot |\sin(\omega_L t)| \\ &+ \frac{V_{im}^2}{2Lf_s V_o} \cdot \sin^2(\omega_L t) \end{aligned} \quad (22)$$

As it can be seen from (22), the average inductor current in CCM2 consists of three components: a constant-current component, a component

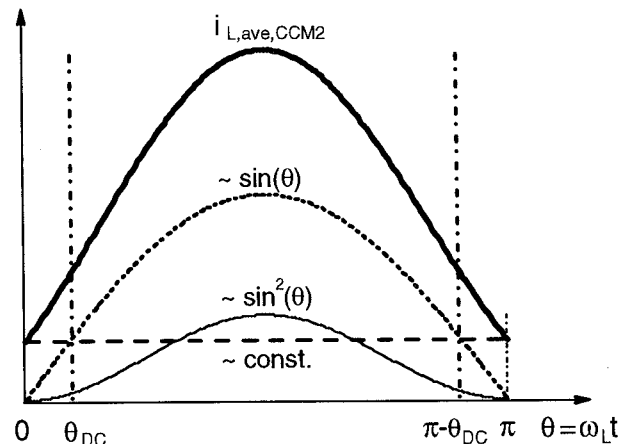


Fig. 4 Current components in CCM2

proportional to the line voltage (desired component), and a component proportional to the square of the line voltage. The three CCM2 current components are shown in Fig. 4.

To make the desired component which is proportional to line voltage positive, from (8) and (22) it follows that it is necessary to satisfy the condition

$$k_S > \frac{1}{2D_{max}} \quad (23)$$

Similarly, from (8) and (22), the ratio of the amplitudes of the desired component and the component proportional to the square of the line voltage is equal to

$$\frac{V_o}{V_{im}} \cdot (2k_S D_{max} - 1) \quad (24)$$

From (24), it can be seen that a larger external ramp increases the amplitude of the desired component. Also, according to (24), with increasing  $V_{im}$ , the contribution of the component proportional to the square of the line voltage to the total average inductor current increases. It should be noted that the sign of the constant-current component can be positive or negative depending on the input voltage and output power.

#### D. Boundary Angle Between Operation Modes

The DCM1-DCM2 boundary angle is obtained from (10) and (15) at  $D_{DCM} = D_{max}$ ,

$$\theta_{D1D2} = a \sin\left(\frac{Lf_s}{V_{im}} \cdot \left(\frac{I_{ref}}{D_{max}} - I_{RM}\right)\right), \quad (25)$$

while the DCM1-CCM2 boundary angle is directly determined from (6),

$$\theta_{D1C2} = a \sin\left(\frac{V_o}{V_{im}} \cdot (1 - D_{max})\right). \quad (26)$$

Finally, the DCM2-CCM2 boundary angle is obtained by equating the peak inductor current from (19) with the peak-to-peak inductor-current ripple from (20), and using (21),

$$I_{ref} = I_{RM} \left(1 + \frac{V_{im} \sin(\theta_{D2C2})}{I_{RM} Lf_s}\right) \cdot \left(1 - \frac{V_{im} \sin(\theta_{D2C2})}{V_o}\right) \quad (27)$$

#### E. Reference Current

The reference current in (17), (22), (25), and (27) can be determined from the input-output power balance,

$$P_i = \frac{2}{\pi} \cdot V_{im} \cdot \left( \int_0^{\theta_{DP}} i_{L,ave,DCM1}(\theta) \cdot \sin(\theta) \cdot d(\theta) + \int_{\theta_{DD}}^{\theta_{DC}} i_{L,ave,DCM2}(\theta) \cdot \sin(\theta) \cdot d(\theta) + \int_{\theta_{DC}}^{\pi/2} i_{L,ave,CCM2}(\theta) \cdot \sin(\theta) \cdot d(\theta) \right) = \frac{P_o}{\eta}, \quad (28)$$

where  $\theta = \omega_L t$ , and  $\eta$  is the efficiency of the ICS power stage. Equation (28) encompasses all three MSs from Table I. Definition of boundary angles  $\theta_{DD}$  and  $\theta_{DC}$  is given in Table I.

The input power during CCM2 can be expressed in a closed form. By substituting (22) into (28), after integration, the following is obtained:

$$P_{i,CCM2} = \frac{2}{\pi} \cdot V_{im} \cdot (I_{ref} - I_{RM}) \cdot \cos(\theta_{DC}) + \frac{1}{\pi} \cdot V_{im}^2 \cdot \left(\frac{I_{RM}}{V_o} - \frac{1}{2Lf_s}\right) \cdot \left(\frac{\pi}{2} - \theta_{BC} + \frac{\sin(2\theta_{DC})}{2}\right) + \frac{1}{3\pi} \cdot \frac{V_{im}^3}{Lf_s V_o} \cdot \cos(\theta_{DC}) \cdot (2 + \sin^2(\theta_{DC})). \quad (29)$$

The input power during DCM1 and DCM2 can be obtained by numerical integration of the following expressions:

$$P_{i,DCM1} = \frac{1}{\pi} \cdot \frac{V_{im}^2}{Lf_s} \cdot D_{max}^2 \cdot \int_0^{\theta_{DP}} \frac{\sin^2(\theta)}{1 - \frac{V_{im} \sin(\theta)}{V_o}} \cdot d\theta, \quad (30)$$

and

$$P_{i,DCM2} = \frac{1}{\pi} \cdot \frac{V_{im}^2}{Lf_s} \cdot \left(\frac{I_{ref}}{I_{RM}}\right)^2 \cdot \int_{\theta_{DD}}^{\theta_{DC}} \frac{\sin^2(\theta)}{\left(1 - \frac{V_{im} \sin(\theta)}{V_o}\right) \cdot \left(1 + \frac{V_{im} \sin(\theta)}{I_{RM} Lf_s}\right)^2} \cdot d\theta. \quad (31)$$

In MS1, the boundary angles are equal,  $\theta_{DD} = \theta_{DC} = \theta_{D1C2}$ , and as seen from (26), independent of the reference current. Hence, by replacing  $\theta_{D1C2}$  from (26) into (29) and (30),  $I_{ref}$  can

be directly determined from the power balance, (28).

In MS3, the boundary angles are  $\theta_{DD} = 0$  and  $\theta_{DC} = \theta_{D2C2}$ , defined by (27). After substituting  $I_{ref}$  from (27) into (29) and (31), from the power balance, (28), the boundary angle  $\theta_{D2C2}$  can be found first. Then,  $I_{ref}$  can be calculated from (27).

Finally, in MS2, the boundary angles are  $\theta_{DD} = \theta_{D1D2}$ , (25), and  $\theta_{DC} = \theta_{D2C2}$ , (27). Again, after replacing  $I_{ref}$  from (27) into (25) and (29)-(31), from the power balance, (28), the boundary angle  $\theta_{D2C2}$  can be found first, and then  $I_{ref}$  can be calculated from (27).

The whole procedure described above can be easily implemented by using any standard mathematical software (e.g. Mathcad). In a particular design,  $I_{ref}$  is calculated for all three MSs. The actual value of  $I_{ref}$ , i.e. the actual MS, is the one which satisfies a MS condition from Table I.

### F. Input Current Harmonics

The input current contains only odd harmonics whose rms values can be determined by using Fourier analysis:

$$I_{i,k} = \frac{2\sqrt{2}}{\pi} \cdot \left( \int_0^{\theta_{DD}} i_{L,ave,DCM1}(\theta) \cdot \sin(k\theta) \cdot d(\theta) + \int_{\theta_{DD}}^{\theta_{DC}} i_{L,ave,DCM2}(\theta) \cdot \sin(k\theta) \cdot d(\theta) + \int_{\theta_{DC}}^{\pi/2} i_{L,ave,CCM2}(\theta) \cdot \sin(k\theta) \cdot d(\theta) \right) \quad (32)$$

The total harmonic distortions are obtained by summing the squares of the first  $N$  (e.g.  $N = 19$ ) odd harmonics,

$$THD_i = \frac{\sqrt{\sum_k I_{i,k}^2}}{I_{i,1}}, k = 3, 5, \dots, N \quad (33)$$

### III. DESIGN

In this section the derived mathematical model is used in the design of an experimental 100-W / 385-Vdc CCB ICS for the universal input voltage range ( $V_{i,rms} = 90\text{-}265$  V).

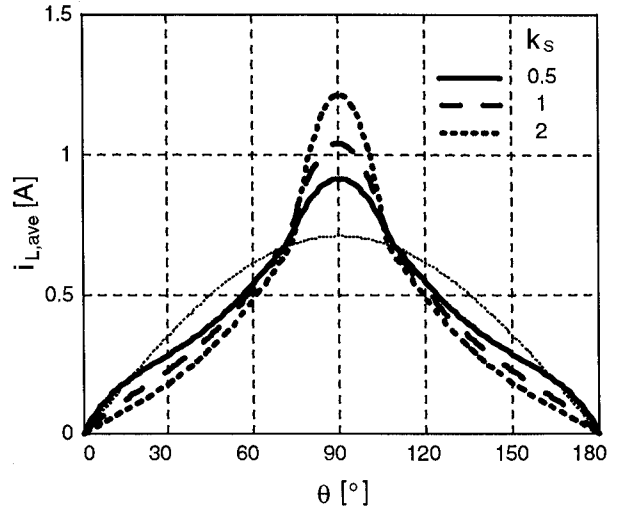


Fig. 5 Line current waveform vs.  $k_s$  at  $V_{i,rms} = 220$  V

According to the line current components, (13), (17), and (22), the design variables are the product of boost inductance and switching frequency  $L \cdot f_s$ , maximum duty cycle  $D_{max}$ , and the height of the ramp current,  $I_{RM}$ . The design of  $L \cdot f_s$  and  $D_{max}$  is determined by the specifications of the power stage and it is performed as for a conventional boost ICS circuit [6]. Therefore, the design of the CCB ICS in this paper is focused on the control circuit, particularly on the ramp current height,  $I_{RM}$ , determined by (8). The key design parameter is the normalized slope of the ramp current,  $k_s$ .

For higher line voltages, i.e.,  $V_{i,rms} > 180$  V, the operation corresponds to MS3. In MS3, the quality of the line current is inversely proportional to  $k_s$ , i.e., with increasing  $k_s$ ,  $THD_i$  increases and  $PF_i$  decreases. As an example, line current waveforms, obtained in Mathcad, for three different values of  $k_s$  at  $V_{i,rms} = 220$  V ( $L = 0.5$  mH,  $f_s = 100$  kHz,  $D_{max} = 0.9$ , and  $\eta = 0.9$ ) are shown in Fig. 5; the corresponding values of  $THD_i$  (calculated for the first 19 odd harmonics) and  $PF_i$  are given in Table II.

TABLE II  
 $THD_i$  and  $PF_i$  vs.  $k_s$  at  $V_{i,rms} = 220$  V

$k_s$	$THD_i$ [%]	$PF_i$
0.5	18.1	0.984
1	28.2	0.962
2	40.2	0.928

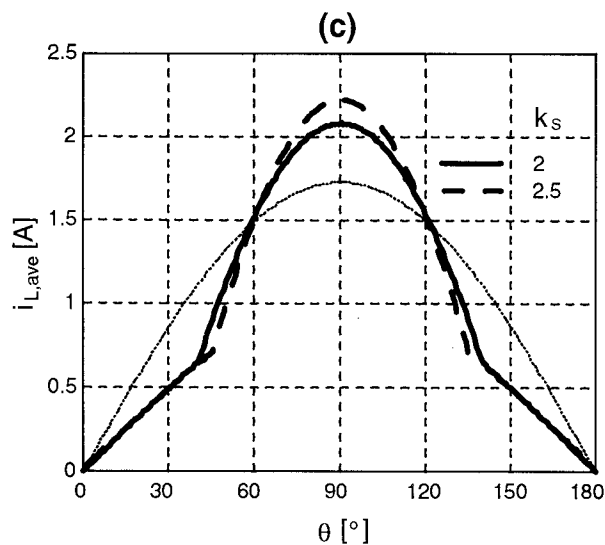
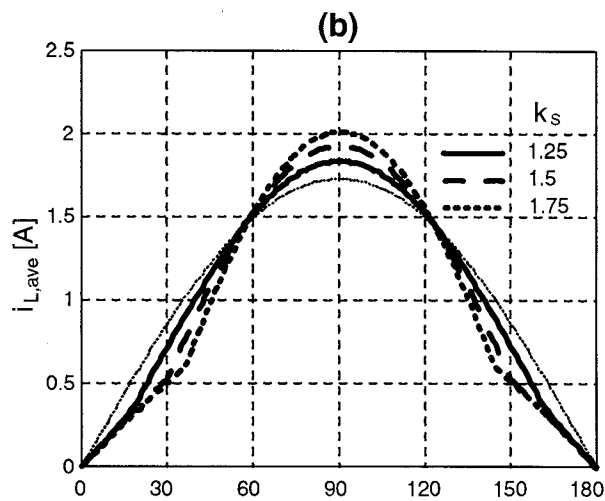
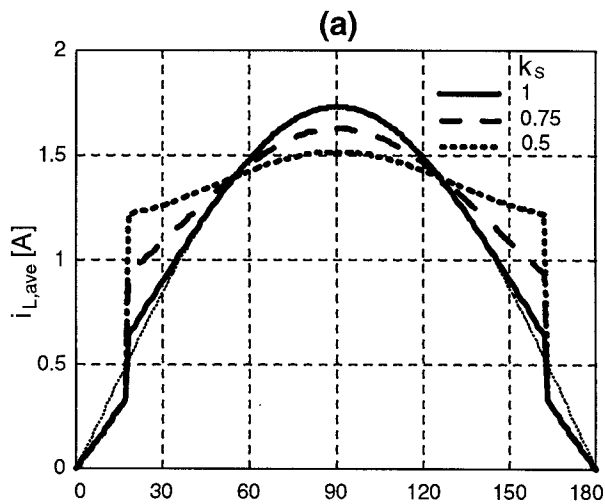


Fig. 6 Line current waveform vs.  $k_S$  at  $V_{i,rms} = 90$  V in (a) MS1, (b) MS2, and (c) MS3

TABLE III  
MS,  $THD_i$  and  $PF_i$  vs.  $k_S$  at  $V_{i,rms} = 90$  V

$k_S$	MS	$THD_i$ [%]	$PF_i$
0.5	1	20.4	0.98
0.75	1	11.6	0.993
1	1	4.3	0.999
1.25	2	8.2	0.997
1.5	2	14.4	0.99
1.75	2	18.6	0.983
2	3	21.9	0.977
2.5	3	27.0	0.965

At lower line voltages, all three MSs are possible. For example, at minimum line voltage,  $V_{i,rms} = 90$  V, with increasing  $k_S$ , the operation changes from MS1  $\rightarrow$  MS2  $\rightarrow$  MS3, as presented in Table III and Fig. 6. In MS2, similarly as in MS3, the quality of the line current is inversely proportional to  $k_S$ , i.e., with increasing  $k_S$ ,  $THD_i$  increases and  $PF_i$  decreases. However, in MS1, the quality of the line current varies proportionally to  $k_S$ , i.e., with increasing  $k_S$ ,  $THD_i$  decreases and  $PF_i$  increases (see Table III). It was found as good design compromise to select  $k_S$  so that at minimum line voltage, operation in MS1 close to the boundary with MS2 is achieved. It follows from Table III that  $k_S = 1$ .

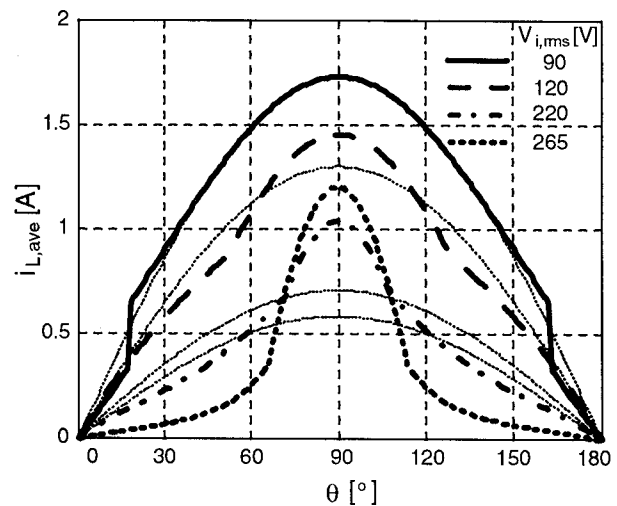


Fig. 7 CCB ICS line-current waveform vs.  $V_{i,rms}$  with  $k_S = 1$  at full load. Ideal sinusoidal line-current waveforms are also shown (.....).

TABLE IV  
CCB-ICS BASIC CHARACTERISTICS at  $k_S = 1$   
( $I_R = 6.24$  A,  $I_{RM} = 6.93$  A,  $\Delta I_{L,pk,DCM1,max} = 0.693$  A)

$V_{i,rms}$ [V]	MS	$I_{ref}$ [A]	$\theta_{DD}$ [°]	$\theta_{DC}$ [°]	$THD_i$ [%]	$PF_i$
90	1	7.22	8	18	4.3	0.999
120	2	6.27	1	52	9.8	0.995
220	3	2.96	0	72	28.2	0.96
265	3	1.49	0	66	68.2	0.825

Line current waveforms obtained in Mathcad, with  $L = 0.5$  mH,  $f_s = 100$  kHz,  $D_{max} = 0.9$ ,  $\eta = 0.9$ , and  $k_S = 1$ , for four rms line voltages, are shown in Fig. 7. The circuit operates in MS1 at  $V_{i,rms} = 90$  V, in MS2 at  $V_{i,rms} = 120$  V, and in MS3 at  $V_{i,rms} = 220$  V and  $V_{i,rms} = 265$  V. Corresponding values of  $THD_i$  and  $PF_i$  are given in Table IV. The

values of  $I_{ref}$  and boundary angles  $\theta_{DD}$  and  $\theta_{DC}$  are also included in Table IV. In Figs. 5-7 ideal, sinusoidal line-current waveforms are also shown.

It should be noted that the line current waveform and the input power factor at higher line voltages can be improved by employing nonlinear feed-forward control [4].

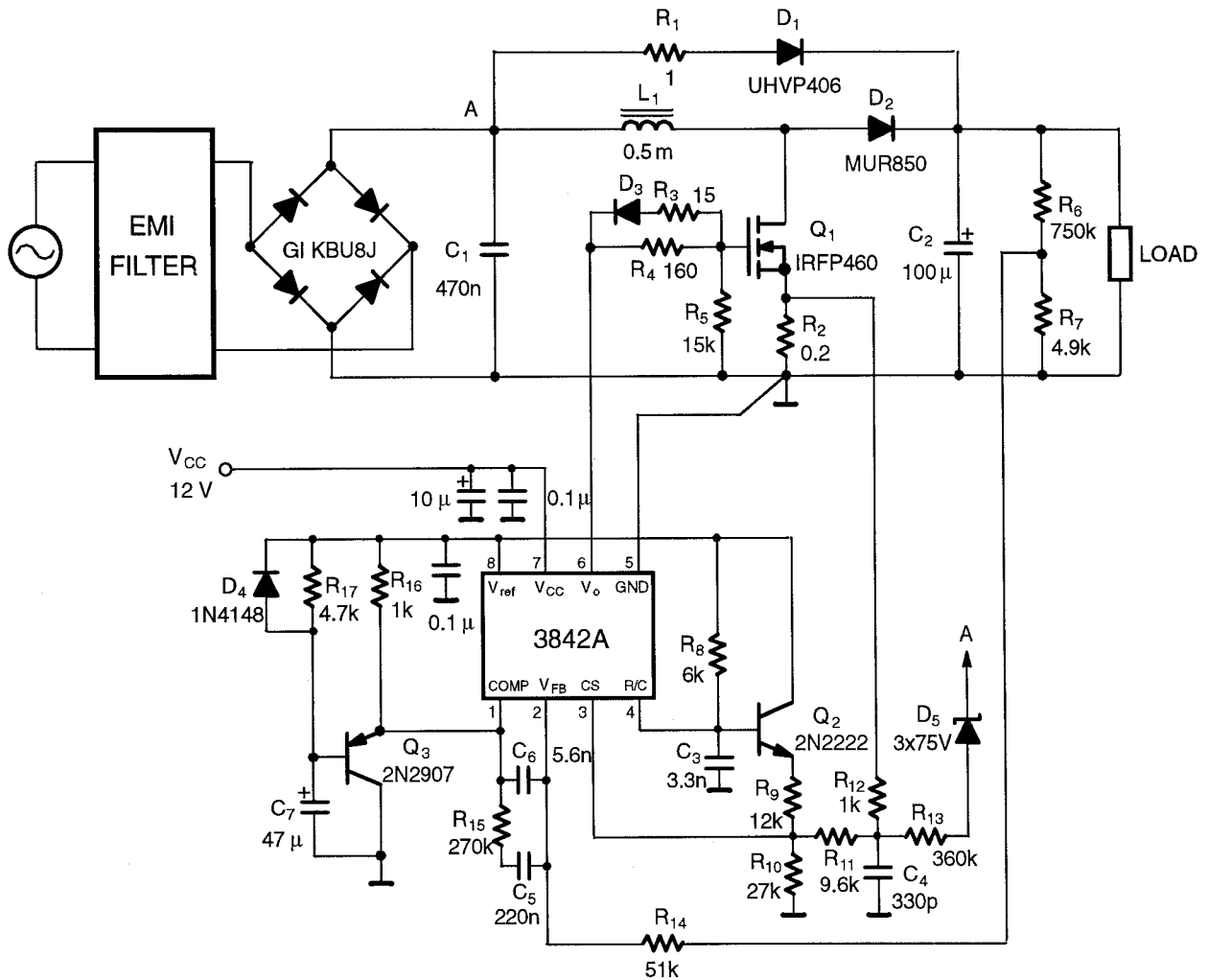


Fig. 8 Experimental CCB ICS circuit diagram

The experimental circuit diagram is shown in Fig. 8. The control circuit is based on the conventional current-mode PWM controller 3842 [7]. Design of resistors  $R_2$ ,  $R_9$ ,  $R_{10}$ , and  $R_{11}$ , related to the external ramp, is described next.

As the input signals of the PWM (see also Fig. 1) are voltages, expression (3) is rewritten with voltage signals,

$$S_e^v = k_S \cdot R_i \cdot S_{f,max}^i \quad (34)$$

The slope-compensation-ramp voltage is generated from the oscillator voltage of the PWM controller. The slope of the ramp voltage at the input of the PWM (pin 3) is obtained as

$$S_e^v = \frac{R_{10} // R_{11}}{R_{10} // R_{11} + R_9} \cdot \frac{\Delta V_{osc}}{D_{max}} \cdot f_s, \quad (35)$$

where  $R_{10} // R_{11}$  denotes the parallel connection of  $R_{10}$  and  $R_{11}$ ;  $\Delta V_{osc}$  is the peak-to-peak oscillator voltage at pin 4 of the controller chip ( $\Delta V_{osc} = 1.7$  V [7]). It is assumed that  $R_{11} \gg R_{12}$ . The current-sense resistor, seen by the input of the PWM, is

$$R_i = \frac{R_9 // R_{10}}{R_9 // R_{10} + R_{11}} \cdot R_2, \quad (36)$$

where the attenuation caused by the low-pass filter,  $R_{12} - C_4$ , is neglected. The maximum down slope of the inductor current is, from (5) and (6),

$$S_{f,max}^i = \frac{D_{max} \cdot V_o}{L} \quad (37)$$

Substituting (35)-(37) into (34), it follows that

$$\frac{R_{11}}{R_9} = k_S \cdot \frac{D_{max}^2 \cdot V_o}{\Delta V_{osc} \cdot L f_s} \cdot R_2 \quad (38)$$

The other relationship between resistors  $R_2$  and  $R_9 - R_{11}$  is obtained from the maximum voltage condition on pin 3 of the 3842 controller:  $V_3 \leq 1$  [7],

$$\begin{aligned} \frac{R_9}{R_{10}} &\geq V_{osc,min} + \Delta V_{osc} - V_{BE} - 1 \\ &+ \frac{R_9}{R_{10}} \cdot (R_2 \cdot i_{L,pk,max} - 1), \end{aligned} \quad (39)$$

where  $V_{osc,min}$  is the minimum oscillator voltage at pin 4 ( $V_{osc,min} \approx 1$  V) and  $i_{L,pk,max}$  is the maximum

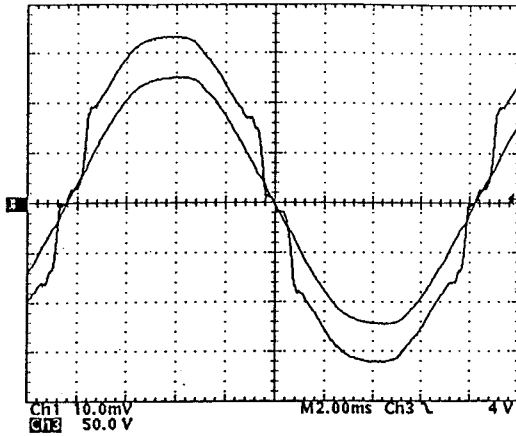
peak inductor current, obtained at minimum line voltage,  $V_{i,rms} = 90$  V. From (8), (19), (21), and Table IV,  $i_{L,pk,max} = 2.58$  A. The resistances given in Fig. 8 satisfy expressions (38) and (39).

#### IV. EXPERIMENTAL RESULTS

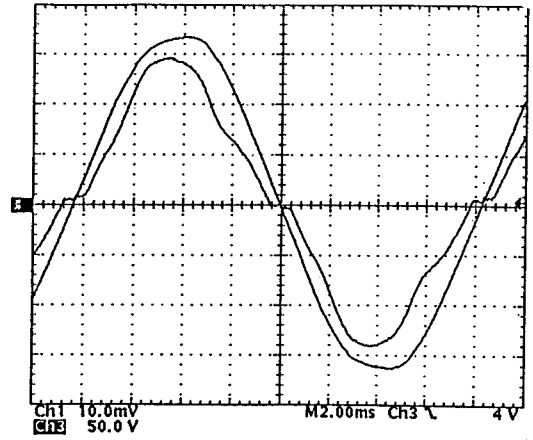
Experimental line-current waveforms at full resistive load ( $I_{LOAD} = 0.26$  A) for four rms line voltages are presented in Fig. 9. The experimental waveforms are in good agreement with the theoretical waveforms, except for the additional phase shift in the experimental line-current waveforms, which is due to the effect of the input filter.

In order to improve the quality of the line current waveform, i.e., decrease  $THD_i$  and increase  $PF_i$ , feed-forward control [4] is employed at  $v_i(t) > 225$  V. The nonlinear feed-forward control is implemented with three 75-V Zener diodes in series, as shown in Fig. 8. Instead of high-voltage Zener diodes, low-voltage Zener diodes can be used with an additional resistive voltage divider. As can be seen from Figs. 9(d) and 9(f), the feed-forward limits the peak current and makes the current waveform wider, resulting in higher input power factor.

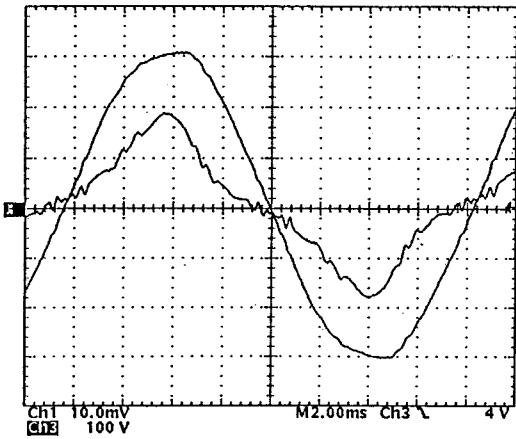
At higher rms line voltages, the line current contains some irregularities which can be explained with the circuit behavior in DCM. Namely, after the boost diode turns off, the MOSFET drain-source capacitance and the boost diode capacitance oscillate with the boost inductance, as shown in the inductor-current waveforms in Fig. 10. The amount of charge transferred back into the filter capacitance  $C_1$  varies depending on the duration of DCM. For example, in Fig. 10(c), the DCM oscillation consists of three half sinusoids, which means that more charge is transferred into  $C_1$  than out of  $C_1$ , i.e., extra charge is available from  $C_1$  to supply the load and less charge is necessary to be drawn from the line. Hence, the line current slightly decreases around interval  $T_2$ . In DCM around interval  $T_3$ , there are two full-sinusoidal oscillations and no extra charge is accumulated in  $C_1$ , resulting in no distortion of the line current. Around interval  $T_1$ , the circuit operates in CCM. The irregularities in the line current waveform at higher line voltages can be made smaller by increasing the filter capacitance,  $C_1$ .



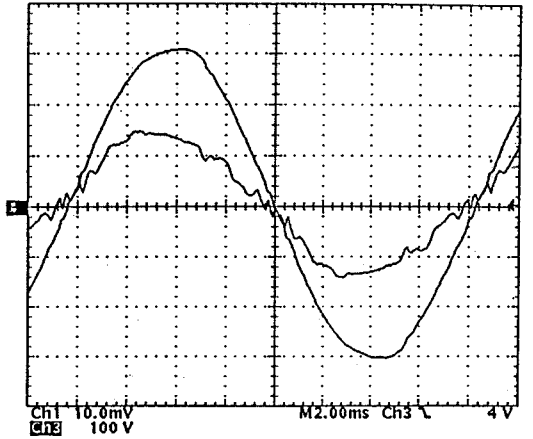
(a)  $V_{i,rms} = 90 \text{ V}$ ,  $PF_i = 0.995$



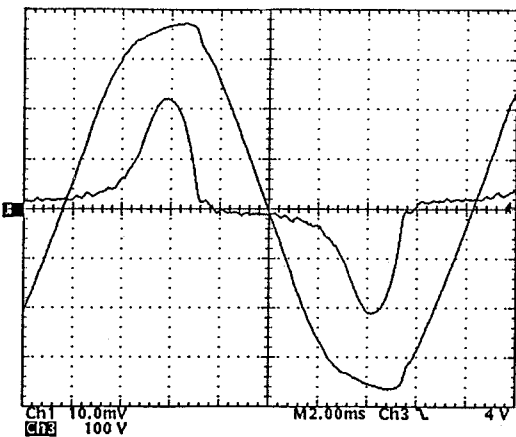
(b)  $V_{i,rms} = 120 \text{ V}$ ,  $PF_i = 0.984$



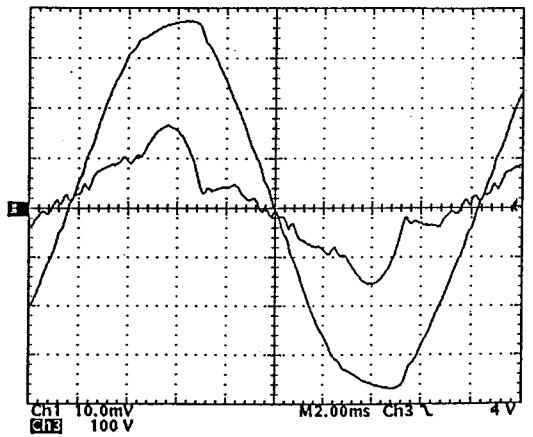
(c)  $V_{i,rms} = 220 \text{ V}$ ,  $PF_i = 0.95$   
w/o feed-forward control



(d)  $V_{i,rms} = 220 \text{ V}$ ,  $PF_i = 0.98$   
w/ feed-forward control



(e)  $V_{i,rms} = 265 \text{ V}$ ,  $PF_i = 0.8$   
w/o feed-forward control



(f)  $V_{i,rms} = 265 \text{ V}$ ,  $PF_i = 0.923$   
w/ feed-forward control

Fig. 9 Experimental line voltage and line current (0.5 A/div) waveforms at full resistive load

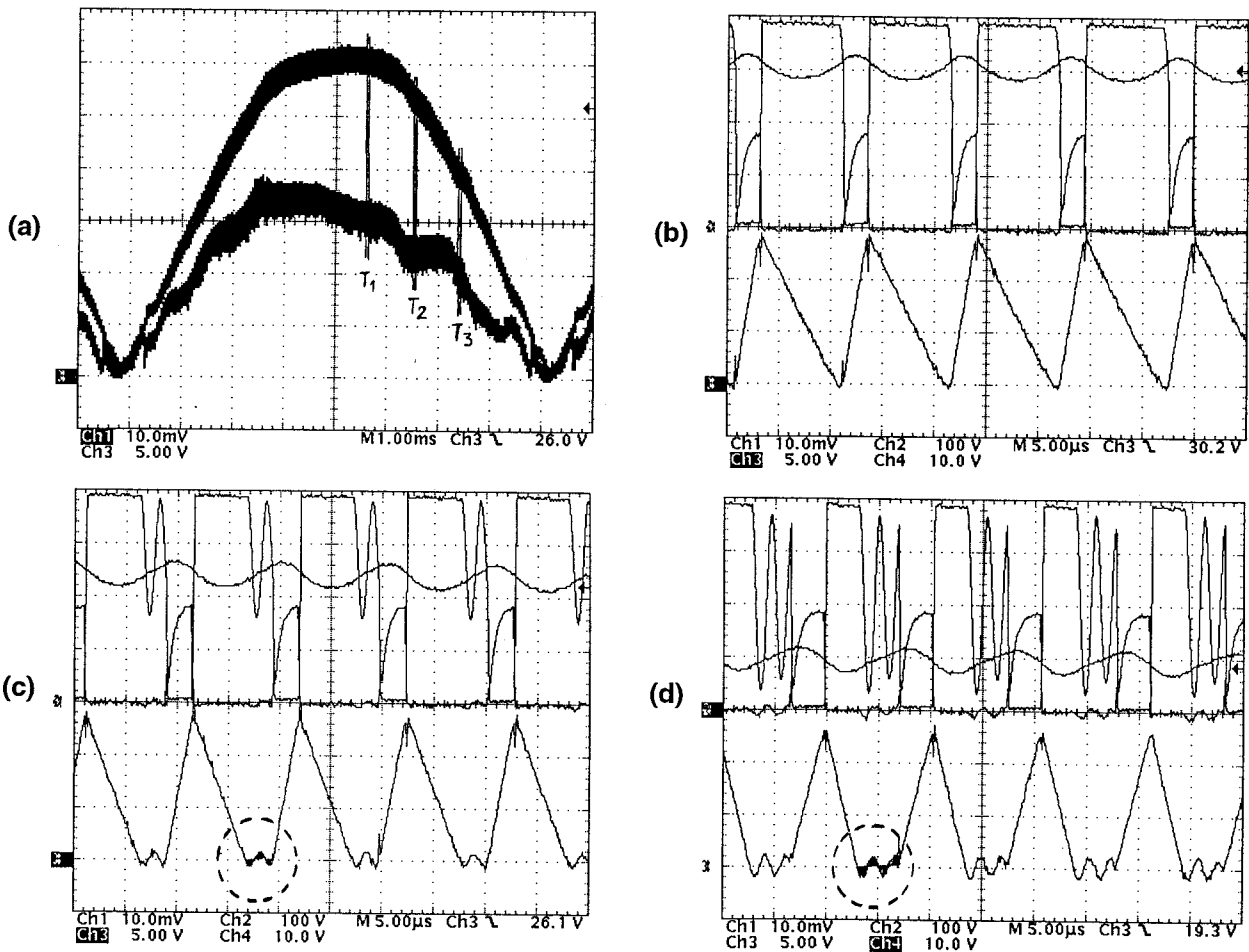


Fig. 10 Line-current waveform irregularities at  $V_{i,rms} = 220$  V, w/ feed-forward control: (a) experimental voltage and current waveforms after rectifier bridge; expanded waveforms around intervals (b)  $T_1$ , (c)  $T_2$ , and (d)  $T_3$ , from top to bottom:  $v_{DS}$  (100 V/div),  $v_A$  (50 V/div),  $v_{GS}$  (10 V/div), and  $i_L$  (0.2 A/div).

## V. CONCLUSION

A design-oriented analysis of the clamped-current boost input-current shaper that includes the effects of the boost inductance, switching frequency, and maximum duty cycle of the controller is presented. The derived design equations are given in closed forms so that they can easily be computed by any standard mathematical software. The presented mathematical model of and proposed design procedure for the clamped-current boost input-current shaper are experimentally verified on a universal input-voltage-range, 100-W converter.

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