Review of Milan M. Jovanović’s work and impact on the power electronics industry

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Abstract—Milan M. Jovanović (1952-2018) is the most cited industry-affiliated power electronics researcher. This paper is a review of Milan’s work based on his top 100 cited papers in the field of power electronics (according to Google Scholar), as well as his most recently published papers. His primary area of interest was the development and performance optimization of power electronics technologies for modern server, telecom, and portable data-processing equipment, as well as for on-board electric vehicle applications. Power conversion techniques developed by research teams led by Milan have been employed in hundreds of millions of power supplies made by Delta Electronics and other manufacturers, enabling further miniaturization of electronics equipment and resulting in enormous cumulative energy savings and electronic-material waste reduction.

I. INTRODUCTION

Milan M. Jovanović (1952-2018) is the most cited industry-affiliated power electronics researcher. He published almost 100 papers in major technical journals and magazines and close to 200 technical papers in conference proceedings. He holds more than 50 U.S. patents.

For over 35 years, Milan and his research teams innovated more efficient ways of supplying electrical energy to information technology devices with reduced size and weight. His primary area of interest was the development and performance optimization of power electronics technologies for modern server, telecom, and portable data-processing equipment, as well as for on-board electric vehicle applications. His main area of expertise was efficiency improvements of centralized and distributed ac/dc power systems through the development, refinements, and optimization of power converter architectures, topologies, control, and power management techniques aimed at creating conditions for optimal use of semiconductor components and magnetic devices. His experience included analysis, modeling, control, simulation, and design of high-frequency, high-power-density power converters; modeling, testing, evaluation, and application of high-power semiconductor devices; and design optimization of magnetic devices for power conversion applications. His latest research was focused on the development of next-generation on-board power converters for automotive applications and power conversion and management issues related to maximizing the efficiency and power density of distributed power systems in large data centers. Power supply techniques developed by research teams led by Milan have been employed in hundreds of millions of power supplies made by Delta Electronics and other manufacturers, enabling further miniaturization of electronics equipment and resulting in enormous cumulative energy savings and electronic-material waste reduction. Making our world greener was a philosophy of Milan that heavily influenced his work and achievements.

Milan’s achievements were widely recognized by the power electronics community, which distinguished him by numerous professional awards. In 2001, he was elected to the grade of IEEE Fellow “for contributions to high-frequency power conversion techniques.” In 2015, he was inducted to the U.S. National Academy of Engineering “for efficiency improvements of ac/dc power supplies in information technology systems.”

This paper is a review of Milan M. Jovanović’s work based on his top 100 cited papers in the field of power electronics (according to Google Scholar), as well as his most recently published papers. All of Milan’s papers referenced in this paper are categorized based on the power supplies’ architectures, topologies, and modes of operation as shown in Table I. A special category in Table I includes review-type papers.

II. AC/DC CONVERTERS

A. Single-Phase Front Stage

A.1 Single-Phase CCM Boost PFC

In development and performance optimization of power electronics technologies for modern server and telecom equipment, efficiency improvement of off-line power supplies has been one of the most important challenges. Generally, at higher power levels, the continuous-conduction-mode (CCM) boost converter is the preferred topology for implementing the front stage of the off-line power supplies with power factor correction (PFC). The output voltage of the boost PFC circuit is relatively high since it must be higher than the peak input voltage. Due to the high output voltage, the boost converter requires the use of a fast-recovery rectifier. At high switching frequencies, fast-recovery rectifiers produce significant reverse-recovery-related losses when switched under hard switching conditions [4]. These losses can be significantly reduced and good efficiency can be maintained even at high switching frequencies by employing soft-switching techniques.

A number of soft-switched boost converters and their variations [29], [44], [45], [49], [51], [54], [63], [66], [68], [70], [92], [97] and [109] were proposed, which employ an auxiliary active switch with a few passive components (inductors and capacitors) to form an active snubber that is used to control the di/dt rate of the rectifier current and to create conditions for zero-voltage switching (ZVS) of the main switch and the rectifier. Although many soft-switching circuits were introduced, there are two distinguished topologies that have been utilized for power supplies in computer servers [66] and telecom equipment [44]. From the late 1990s until the mid-2010s, the majority of off-line power supplies for data centers employed one of these two topologies.

Since the late 2010s, newly introduced SiC diodes that do not cause reverse-recovery-related losses have replaced the fast recovery rectifiers. As a result, the above mentioned soft-switching technologies are seldom used in new designs of off-line power supplies.

Recently, to maximize the efficiency of ac/dc power supplies, bridgeless PFC circuit topologies that reduce the conduction loss by reducing the number of semiconductor components in the line-
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current path have been employed [1]. Because of low electromagnetic interference (EMI), a bridgeless PFC rectifier, also referred to as dual boost converter, has drawn the most attention. However, it has a major drawback: low utilization of switches and magnetic components. In [9] and [103], an implementation was proposed that employs a unique multi-winding, multi-core inductor to increase utilization of the magnetic material.

Another approach to improve the efficiency of ac/dc power supplies by reducing the conduction loss of the front stage is to replace the line-voltage full-bridge rectifier diodes with synchronous rectifiers (SRs) [81].

In high-power (several kW) and/or high-voltage (>650 V) applications, multi-level CCM boost PFC converters have advantages compared to the conventional two-level CCM boost PFC converters. In [6], a three-level CCM boost PFC converter was introduced, which uses a smaller inductor and lower voltage devices than the conventional boost PFC counterpart, yielding high-power density, high efficiency, and low cost.

Single-phase CCM boost PFC converters are also employed in high-availability power systems for data processing and communication equipment used in mission-critical applications, where these converters must be implemented with enhanced reliability. Usually, increased power-system reliability is achieved by employing power system components with high intrinsic reliability and by implementing highly redundant power-system architectures that include the redundancy of the primary power source. In [111], a number of dual ac-input ac/dc power supply architectures were proposed. Fault tolerant power systems that use a dual ac-input architecture can be implemented with isolated boost converters [91]. In fact, implementation with isolated-boost converters offers a reduced number of components compared to implementation with non-isolated boost converters, which further increases reliability.

A.2 Single-Phase DCM/CCM Boost PFC

In off-line power supplies with PFC, a discontinuous-conduction-mode (DCM)/CCM boundary boost converter is widely employed at low-power levels (up to 300W) because it is more efficient and more cost effective than its CCM counterpart. These benefits are brought about by elimination of the reverse-recovery-related losses of the boost diode and by turning on the boost switch with ZVS or near ZVS (also called valley switching). However, the switching frequency, which changes with the instantaneous line voltage and load current, varies over a wide range. In order to prevent excessive switching losses, a maximum switching frequency is often limited. Line-current distortions due to valley switching and switching-frequency limitation were analyzed in [28].

The peak inductor current of the DCM/CCM boundary boost PFC is twice its average current, which often necessitates a larger differential-mode (DM) EMI filter. The input current ripple and, consequently, the input DM-EMI filter can be significantly reduced by interleaving two or more DCM/CCM boundary boost PFC converters. In addition, the output current ripple can also be significantly reduced, resulting in a reduced equivalent-series-resistance (ESR) loss of the output capacitor, and possibly a reduction in capacitor volume. Another benefit of interleaving is that the efficiency at lighter loads can be increased by employing phase shedding, i.e., by progressively turning off converters as the load decreases.

By interleaving two or more DCM/CCM boundary boost PFC converters, the benefits of DCM/CCM boundary boost PFC converters can be extended to higher power levels. However, since the switching frequency is variable, the synchronization of interleaved DCM/CCM boundary boost PFC converters presents a challenging task.

In [22], a systematic classification and detailed analysis of open-loop interleaving methods for DCM/CCM boundary boost PFC converters with master-slave relationship was provided. It was shown that the only open-loop control method that results in stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control.

In [43] and [59], a systematic review of phase-locked-loop (PLL)-based closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters was presented. It was concluded that the PLL-based closed-loop methods always provide stable operation.

The results presented in [22], [43], [59], and [61] had a significant impact on the development of dedicated controller integrated circuits (ICs) for the DCM/CCM boundary boost PFC converters by different IC manufacturers.

In [50], the interleaved DCM/CCM boundary boost PFC converter with current-mode control is compared with two CCM boost PFC converters with soft switching at universal line voltage (90-270 Vrms) and 1.2-kW maximum output power. It was concluded that the efficiency of the interleaved DCM/CCM boundary boost PFC converter at higher power levels (>1 kW) is similar to the efficiency of the two CCM boost PFC converters with soft switching.

A.3 Single-Phase DCM Boost PFC

In [42], a digital signal processor (DSP) based digital control of the single-phase DCM boost PFC converter for the universal line voltage was presented. The implementation of digital control for switch-mode power supplies became feasible with the emergence of high-speed and relatively low cost DSPs at the late 1990s and early 2000s. The DSP-based control offers many features that are not available in analog control such as, for example, programmability, flexibility, insensitivity to aging and environmental variations (e.g., temperature and humidity), intelligence (e.g., self-diagnosis, parameter estimations, etc.), and real-time communications. In addition, the implementation of soft-start control and management of fault protection is far more flexible and often simpler in digital-based control than in its analog counterpart.

The DCM boost PFC converter is quite suitable for digital control implementation because it requires only a low-bandwidth voltage loop. In [42], a step-by-step design procedure based on digital redesign technique was provided. It was shown that the proposed DSP control with variable duty cycle can achieve a power factor (PF) greater than 0.99 in the entire line range.

A.4 Single-Phase Buck PFC

Typically, a boost PFC front stage exhibits 1%–3% lower efficiency at 100-Vrms line than at 230-Vrms line. Another drawback of the universal-line boost PFC front stage is related to its relatively high output voltage, typically 380-400 V. This high voltage not only has a detrimental effect on the switching losses of the boost converter, but also the switching losses of the primary-side switches of the downstream isolated dc/dc output stage and the size and efficiency of its isolation transformer.

At lower power levels (below 350 W), the drawbacks of the universal-line boost PFC front stage can be overcome by implementing the PFC front stage with the buck topology. Since the buck PFC converter does not shape the line current around the zero crossings of the line voltage, i.e., during the time intervals when the line voltage is lower than the output voltage, it exhibits increased
total harmonic distortion (THD) and lower PF compared to its boost counterpart. As a result, in applications where the IEC61000-3-2 and corresponding Japanese specifications need to be met, the buck converter PFC employment is limited to power levels typically below 100 W.

In [24], a detailed design-oriented analysis of the clamped-current buck PFC converter was provided. The proposed design was employed in an 80-V output, universal-input clamped-current buck PFC converter, which is used as the front stage in a 90-W notebook adapter. It was shown that the buck PFC maintains a high efficiency of around 96% across the entire input voltage range and across a load range from 100% to 25%.

In [21], a bridgeless buck PFC rectifier was introduced. By eliminating the input bridge diodes, the proposed rectifier’s efficiency is further improved. Moreover, the rectifier doubles its output voltage, which extends the useable energy of the bulk capacitor after a drop-out of the line voltage.

A.5 Single-Phase Passive PFC

In [40], it was shown theoretically and verified experimentally that the full-bridge (FB) rectifier with an LC filter can meet the European (IEC 1000-3-2, Class D) and the corresponding Japanese specifications for line-current harmonic limits. The major advantages of the passive PFC compared to the active PFC are lower cost and higher efficiency. However, the major drawback of the passive PFC is the relatively heavy weight of the inductor. Inductor design considerations and performance evaluation results for applications with power levels between 75 W and 600 W were presented.

A.6 Power Storage

A well-recognized disadvantage of a single-phase PFC converter is that the power delivered from the line to the PFC stage output is much lower than required when the ac line voltage is close to zero and much higher than required when the ac line voltage is close to its peak value. As a result, the output voltage of the PFC stage has high double-line-frequency ripple. This ripple can be reduced by adding a large number of Aluminum (Al) capacitors at the output. However, these capacitors significantly increase the size of the PFC stage and severely limit the lifetime of the PFC stage.

To overcome these drawbacks, a power pulsation buffer (PPB) can be used in parallel to the PFC output. The PPB is essentially a bidirectional converter that charges an energy-storage capacitor (ESC) at the other end when the PFC stage input power exceeds the output power and discharges the ESC when the input power is below the output power. The voltage variation across the ESC during a line cycle can be much larger than that across the Al capacitors. Therefore, the value of the ESC can be much lower than the value of the Al capacitors. The ESC is typically implemented with high-power-density ceramic capacitors. For PPB, the buck topology is commonly used due to its low component count and high efficiency. However, the design of the buck PPB control is very challenging. In earlier publications, up to five feedback loops were used that require a very powerful and expensive DSP. In [82], a simple control method was proposed with only one feedback loop and with input power feedforward. It was shown that the proposed design can meet a typical 3% requirement for the double-line frequency ripple at the output of the PFC stage.

B. Three-Phase Front Stage

B.1 Three-Phase CCM Boost PFC

Active three-phase PFC rectifiers need to meet very challenging performance requirements. Today, in the majority of applications, their input current is required to have a THD less than 5% and a PF greater than 0.99. One of the most cost-effective topologies that can meet these requirements is the three-phase six-switch boost PFC rectifier, which is usually implemented without neutral-point connection. Control methods that can achieve a high quality of the input currents in the three-phase six-switch boost PFC rectifier are usually implemented with digital technology. One control method, well suited for digital implementation is the average-current control.

In the average-current control, the output voltage controller is usually implemented with proportional plus integral (PI) compensation, whereas the current controller can be implemented with PI or P compensation. The average-current control in most implementations also includes voltage feedforward (VFF), zero-sequence-signal (ZSS) injection, and duty-cycle feedforward (DDF). In [74], it was shown that with mismatched input-voltage and input-current sensing gains, as well as offset errors in the input-voltage and input-current sensing, the current controller with P compensation exhibits lower THD of input currents and higher PF compared to that with PI compensation.

In [79], implementation and performance comparisons of five control methods for the average-current-controlled three-phase six-switch boost PFC rectifier were presented: three control methods in the stationary (a,b,c) reference frame and two control methods in the rotating (d,q) frame. The stationary (a,b,c) reference frame methods include implementations with three independent controllers, with six-step pulse-width modulation (PWM), and with three-step PWM (introduced in [80]), whereas the rotating (d,q) frame methods include implementations with ZSS-injection based PWM and with space vector modulation (SVM). It was found that the average-current control with three independent controllers exhibits the lowest THD of the input currents, whereas the average-current control in the rotating (d,q) reference frame with ZSS-injection based PWM and with SVM exhibits the highest PF. Regardless of the control method used, start-up of the PFC rectifier should be controlled so that the input currents and output voltage do not experience abrupt changes, such as current spikes and voltage overshoots. To limit the inrush currents after the boost switching is enabled, a duty cycle soft-start procedure was proposed in [76].

A three-phase ac/dc converter can also be implemented with three single-phase ac/dc converters. In [78], an isolated three-phase ac/dc converter without neutral-point connection was implemented with three single-phase isolated ac/dc converter modules. The major advantages of the modular implementation are that a mature design of the single-phase power supplies can be utilized, as well as the ease of power expandability. To be able to employ single-phase modules designed for the 180/265-Vrms phase-to-neutral voltage in three-phase power systems with the nominal phase-to-phase voltage of 380/480 Vrms, the three single-phase modules must be connected in star (Y) configuration. Without neutral-point connection, any imbalance in the three-phase source phase voltages and/or in the three single-phase modules will create a potential difference between the Y point of the single-phase modules and the source neutral point, resulting in oscillations and significant variations of the input voltages of the single-phase modules. For stable and reliable steady-state operation, where the input voltages always stay within a specified range, a balancing control of the three single-phase modules is necessary. The stable and reliable operation also has to be guaranteed at start-up, as well as in case of phase failure (open or short of one of the phases) and load transients. In [78], the balancing control between three single-phase modules is achieved by equalizing the input admittances of the PFC front stages, which operate with average current control.
B.2 Three-Phase DCM Boost PFC

It is well established that three-phase PFC rectifiers with three or more active switches exhibit superior PF and input-current THD compared to those implemented with fewer switches. However, due to the simplicity and low cost of single- and two-switch rectifiers, they are increasingly employed in cost-sensitive applications such as three-phase battery chargers.

Major concerns in three-phase single- and two-switch rectifiers are their relatively low efficiency due to hard switching and a relatively high input-current THD because of their inability to actively shape each phase current independently.

To minimize the efficiency issue, implementations of three-phase single- and two-switch rectifiers with reduced switching losses were proposed in [32], [101], and [102]. In the proposed circuits, a resonant technique is employed to achieve zero-current switching (ZCS) of the switches. However, this technique requires additional components that increase complexity and cost. In addition, the implementation employing a resonant technique suffers from high voltage and/or current stresses.

To improve the input-current THD of the three-phase single-switch rectifiers, harmonic-injection techniques were introduced in [55], [58], [64], [87], and [88]. These harmonic-injection techniques do not require additional components since the harmonic injection is solely performed at the control level. While all these techniques are proven to reduce the THD without penalizing efficiency, they are not capable of reducing the THD below 5%.

Recently, a new three-phase, two-switch ZVS DCM PFC boost rectifier, also called Taipei rectifier, was introduced in [93], [95], and [105]. The proposed rectifier achieves less than 5% input-current THD over the entire input range and above 20% load and features ZVS of all switches without any additional soft-switching circuitry.

C. Second Stage DC/DC

C.1 Second-Stage PWM DC/DC

The FB ZVS-PWM dc/dc converter is the most widely used soft-switched circuit in high-power applications. This constant-frequency converter employs phase-shift control and features ZVS of primary switches with a relatively small circulating energy. However, full ZVS operation can only be achieved in a limited load and input-voltage range, unless a relatively large inductance is provided in series with the primary winding of the transformer which can be implemented by increasing the leakage inductance of the transformer and/or by adding an external inductor. This increased inductance has a detrimental effect on the performance of the converter since it causes an increased loss of the duty cycle on the secondary side as well as a severe voltage ringing across the secondary-side output rectifiers, which is due to the resonance between the inductance and the junction capacitance of the rectifier.

Several techniques have been proposed to extend the ZVS range of the FB ZVS converters without loss of duty cycle and secondary-side ringing [10], [25], [35], [62], and [89]. In these proposed FB ZVS-PWM converters, the energy available for ZVS increases as the input voltage increases, which is the desirable direction of change since more energy is required to achieve ZVS at higher input voltages.

In recent years, multilevel power converters have received a lot of attention due to their suitability for applications with high input voltages. Specifically, multilevel converters can be implemented with semiconductor switches rated at a fraction of the input voltage, which are typically less expensive and more efficient than their high-voltage-rated counterparts. A new three-level ZVS converter is introduced in [18] and [47]. The proposed three-level ZVS converter employs a coupled inductor on the primary side to achieve ZVS in the entire line and load ranges. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause loss of duty cycle or severe voltage ringing across the output diode.

The majority of today’s computers and computer peripherals require power supplies that are capable of operating in the 90-270-Vrms line range and can provide a hold-up time of at least 10 ms. Generally, the hold-up time is the time during which a power supply needs to maintain its output voltage(s) within a specified range after a dropout of the line voltage. This time is used to orderly terminate the operation of the data-processing equipment or to switch over to an uninterruptible power supply (UPS) operation after a line failure. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor. However, the stored energy in the storage capacitor cannot be fully utilized without a dramatic loss of the converter efficiency due to a significant increase of the dc/dc stage input voltage range. A method that substantially improves the utilization of the stored energy without deterioration of conversion efficiency was proposed in [56] and [90]. This hold-up time extension circuit improves the efficiency and cost by reducing the number of Al capacitors.

For a long time, efficiency increases of power conversion circuits were primarily driven by increased power density requirements since power density increases are only possible if appropriate incremental improvements in full-load efficiency are achieved so that the thermal performance is not adversely affected. As a result, maximization of the full-load efficiency was the design focus. Beginning in the early 2000s, the focus of the power supply industry shifted to efficiency improvements across the entire load range prompted by economic reasons and environmental concerns caused by the continuous aggressive growth of Internet infrastructure and a relatively low energy efficiency of power delivery systems of large Internet-equipment hosting facilities.

A method of maintaining high power-conversion efficiency across the entire load range was introduced in [36] and [104]. Specifically, the proposed method substantially increased the conversion efficiency at light load by minimizing switching and driving losses of semiconductor switches, as well as core losses of magnetic components. These losses were minimized by periodically turning off and on the power converter with a duty cycle set so that when the converter is on, it operates at the power level that exhibits the maximum efficiency. The required output power during the periods when the converter is turned off is supplied from an energy-storage device.

At output power levels below 100 W (e.g., in adapters/chargers for laptops), for the second-stage isolated dc/dc converter, the flyback topology is commonly employed due to its minimal number of semiconductor and magnetic components. The flyback converter is typically designed to operate at the DCM/CCM boundary, since in this mode of operation the primary switch turns on with valley switching and the secondary rectifier turns off with ZCS. This way, the switching and reverse-recovery losses of semiconductor components are significantly reduced. However, at the DCM/CCM boundary, the switching frequency varies, depending on the input voltage and load. Switching frequency increases with decreasing load negatively affecting the light-load efficiency and complicating the controller IC design. To address these issues, [33] proposed an adaptive off-time control that decreases the switching frequency at very light loads. The variable-frequency flyback power stage model, which is necessary for the control loop design, was proposed in [85].

In [65], practical implementation and performance of 70-W constant-frequency and variable-frequency flyback converters were
compared with asymmetrical half-bridge and resonant half-bridge converters. It was found that the variable-frequency flyback converter has slightly lower efficiency than the half-bridge topologies, but significantly lower cost.

In the 1990s, the development of semiconductor technology made the voltage drop across power MOSFETs considerably lower than the forward voltage drop of Schottky diodes with the same voltage rating. This created a strong motivation to replace Schottky diodes with MOSFETs, called synchronous rectifiers (SRs), on the low-voltage secondary side of dc/dc converters. However, due to the large die size of SR MOSFETs, their gate-charge and, therefore, driving loss were high. Also, due to slow MOSFET body diodes, SR reverse-recovery loss in the case of inaccurate timing of their gate-drive voltages was considerable. Therefore, success of replacing Schottky diodes with SRs depended on the development of circuits that can drive SRs with low loss and accurate timing. Efficiency-improvement limits due to replacement of Schottky diodes with both self-driven and control-driven SRs in forward converters with RCD clamp and with active clamp were considered in [34] and [72].

In adapter/charger applications, one of the design issues is the audible noise because these adapters are usually placed close to the user. The source of the audible noise is the mechanical vibration of the magnetic components. At light load, in order to increase efficiency, switch mode power supplies in adapters usually operate in burst mode or in frequency-foldback mode. In [75], it was theoretically shown and experimentally verified that operation of switch-mode power supplies in burst mode results in lower audible noise than operation in frequency foldback mode. C.2 Second-Stage Resonant DC/DC

Resonant converters use a resonant-tank circuit to shape a switch voltage and/or current waveform to minimize switching losses and allow high-frequency operation while maintaining high conversion efficiencies. As a result, resonant converters are extensively used in state-of-the-art power supplies that offer the highest power densities and efficiencies. Generally, resonant converters operate with variable switching-frequency control. When operating above the resonant frequency, resonant converters operate with ZVS of the primary switches. However, variable switching-frequency control is seen as a drawback of resonant converters especially in applications with a wide input-voltage and/or output-voltage range. Specifically, as the input or output voltage range increases, the control frequency range also increases so that driving and magnetic component losses also increase, thereby reducing conversion efficiency. Furthermore, in many applications, converters are restricted to operate within a relatively limited frequency range to avoid interfering with other parts of the system. While resonant converters can operate with a constant frequency (clamp-mode operation), such an operation is not desirable because the increased circulating energy in the resonant tank circuit significantly degrades conversion efficiency. As a result, there have been several attempts to improve performance of resonant converters operating in a wide input-voltage and/or a wide output-voltage range by reducing the switching frequency range with additional range windings and/or switches to effectively change the turns ratio of the transformer. While these approaches have been proven to improve performance, their major drawbacks are additional cost and complexity.

A new control method that improves the performance of resonant converters that operate with wide input/output-voltage ranges by substantially reducing their switching-frequency range was introduced in [107] and [108]. Reduction of the switching frequency range was achieved by controlling the output voltage with a combination of variable-frequency feedback control and open-loop delay-time control. Variable-frequency control is used to control the primary switches of an isolated resonant converter, while delay-time control is used to control secondary-side rectifier switches that replaced the diode rectifiers. The introduced control method is applied to a dc/dc series-resonant converter as the output stage of an on-board charger module (OBCM) for electric vehicles (EVs) operating with a wide output-voltage range. Moreover, the same control method is employed to a bi-directional OBCM.

In [73], a control method for efficiency improvement of the LLC resonant converter operating with a wide input-voltage and/or output-voltage range by means of topology morphing was presented. In this approach, the LLC topology is gradually changed between full-bridge and half-bridge so that a tight output control and uninterrupted power flow were maintained during the transitions.

In [69], two half-bridge high-frequency off-line resonant-type converters with ZVS were presented: ZVS quasi-resonant and ZVS multi-resonant converters. Merits and limitations of these two converters were discussed and comparisons were made with respect to efficiency, load range, and operating frequency range.

D. Single-Stage AC/DC

D.1 Single-Phase Single-Stage AC/DC

In a single-stage off-line power supply, the front stage PFC rectifier and the second stage dc/dc converter are integrated in one stage, typically saving one switch and one controller. However, unlike in a two-stage off-line power supply, in a single-stage off-line power supply, the voltage of the energy-storage capacitor, also called bulk voltage $V_B$, is not regulated and it varies with the line voltage and load current. In universal line applications, voltage $V_B$ varies in a wide range, which requires a large high-voltage rated (> 400 Vdc) capacitor to meet hold-up time requirements. There is a strong trade-off between the cost and size savings brought about by using a single switch and controller, and the increased cost and size of the energy-storage capacitor. The single-stage approach is attractive for lower-power (< 100W), cost-sensitive applications, whereas, for higher power applications, the two-stage approach is the best choice.

The research in the area of the single-stage off-line power supplies was focused on reducing voltage $V_B$. In [15], voltage $V_B$ was substantially reduced with variable switching-frequency control. However, even with a wide range of switching frequency, voltage $V_B$ cannot be kept below 450 Vdc, which is typically used in universal-line single-stage off-line power supplies.

In [23], a single-stage single-switch PFC (SPFC) technique was introduced that was the first single-stage off-line power supply with reduced voltage $V_B$ below 450V suitable for the universal-line applications. Voltage $V_B$ was kept within the desirable range in the entire line and load ranges by the addition of two auxiliary primary windings of the transformer. A complete design-oriented analysis for both DCM and CCM operations of the PFC inductor was provided in [52].

In [57], it was shown that the same performance of the SPFC converter can be achieved when the two additional windings were implemented as portions of the primary winding of the transformer by employing tapping, which made the construction of the transformer simpler. The construction of the transformer was further simplified by merging the two tapering points into one tapering point. In order to improve the efficiency of the SPFC converter in [57], the flyback transformer continuously operates at the DCM/CCM boundary with valley switching. Due to the
DCM/CCM boundary operation, the maximum voltage \( V_o \) at universal-line applications was well below 400V.

A further efficiency improvement of the S\(^2\)PFC technique [57] was disclosed in [39], where the conduction losses in the primary side of the converter were substantially reduced. This was achieved by an effective current interleaving technique between the PFC inductor and a bypass diode. In addition, by rearranging the rectifiers in the PFC part of the converter in such a way that the energy-storage capacitor and the PFC inductor are connected to the ac line voltage through only two rectifiers, one diode forward-voltage drop was eliminated. In 15 years this invention has been implemented in more than 15 million notebook adapters for the universal-line voltage with a nameplate output power greater than or equal to 75W manufactured by Delta. This adapter technology was the only single-stage adapter technology in the external power supply industry that met the EN61000-3-2 standard specifications on the line-current harmonics with an efficiency around 90%.

The S\(^2\)PFC technique [39] was also implemented for high-brightness LED drives at universal line voltage [27]. To meet the line-current harmonic specifications for lighting equipment at low line (JIS C 61000-3-2 class C) and to keep voltage \( V_o \) below 450V at high line, a variable PFC inductance was proposed. According to the proposed method, the PFC inductance has a constant high value at high line, while at low line it is reduced proportionally to the load current. The proposed LED driver was suitable for directly driving LED strings and no post-regulators were necessary, which was a significant advantage over the conventional PFC flyback circuits without energy-storage capacitor on the primary side.

In [37], it was shown that most of the published single-stage PFC (S\(^2\)PFC) circuits belong to two generalized topologies: S\(^2\)PFC with two-terminal PFC cell and S\(^2\)PFC with three-terminal PFC cell. It was also shown that the two generalized S\(^2\)PFC topologies are functionally equivalent. Finally, based on the generalized approach, a few new S\(^2\)PFC circuits were developed.

### D.2 Three-Phase Single-Stage PFC

A new, three-phase, single-stage, isolated ac/dc converter that was derived by combining the Taipei rectifier [93] with the conventional LLC resonant half-bridge converter was introduced in [94] and [106]. The new converter employs only two switches and achieves less than 5% THD of the three-phase input currents and provides a tightly regulated, isolated, output voltage. It features ZVS of both switches over the entire input voltage and load ranges without any additional soft-switching circuitry.

### III. DC/DC CONVERTERS

The second-stage dc/dc converters presented in Section II.C operate from higher input voltages (typically, 400 V) delivered by the front stage PFC rectifiers. The dc/dc converters described in this section supply power for microprocessor systems and operate at lower input voltages (typically below 75 V). This section also includes dc/dc converters with a high voltage conversion ratio used in dual-input-voltage (ac and dc) power supplies, dc/dc converters for wireless charging, as well as dc/dc converters for automotive applications and light emitting diode (LED) drivers.

Every new generation of microprocessor systems requires lower operating voltages at higher load currents with higher slew rates. High-current loads with high slew rates and tight output voltage regulation require dedicated dc/dc converters with fast transient responses, placed in a close proximity to the load in order to minimize the effects of the interconnection parasitics. These point-of-load (POL) converters, also known as voltage regulator modules (VRMs), today have an output voltage in the 0.8 — 1.3-V range and need to provide high currents, often exceeding 100 A, to highly dynamic loads with slew rates as high as 400-500 A/μs.

High-output-current converters in many cases are built by paralleling several lower-current modules. Paralleling has multiple benefits such as modularity, expandability, improved thermal performance and fast load-transient response. Proper paralleling must ensure even current sharing among the paralleled modules. The two most popular current-sharing approaches are the droop current sharing [16] and the active current sharing based on the current-balancing control loops [30], [31], and [60]. In [16], benefits and limitations of the droop current-sharing approach were presented, as well as a design procedure that provides a desired trade-off between the accuracy of the output voltage regulation and accuracy of balancing the paralleled modules’ output currents. In [31], based on an improved model of the active current-sharing control, stability and dynamic performance of paralleled VRMs were analyzed and current-sharing control design guidelines were provided. In [30], a low-cost implementation of the active current sharing control was proposed, where the error amplifier of the current sharing loop is replaced with a comparator. The advantage of this nonlinear current-sharing control is its inherent stability.

The issue of current balancing also exists in LED lighting power supplies where paralleled LED strings are supplied from the same voltage source. In [48], current balancing is achieved by using current-balancing transformers. To make the operation of the balancing transformers possible and provide equal driving currents for the paralleled LED strings, a series-connected switch is turned on and off by a high-frequency signal. The proposed circuit achieves current-balancing error below 4% at low cost.

To achieve fast transient responses, the power conversion must be performed at higher switching frequencies. However, high-frequency operation increases losses of semiconductor and magnetic components which have detrimental effects on converter efficiency. One approach to gain the performance benefits of increased switching frequency without compromising the efficiency is the interleaving technique, which enhances the performance of the paralleled converters. With interleaving, the switching frequency of the individual modules does not increase. However, by phase shifting the switching instances of the paralleled modules, the ripple frequency at the input and output of the paralleled modules increases as many times as the number of the interleaved modules. As a result, the input-current and output-voltage ripple are significantly reduced.

In [12], two interleaving approaches for the forward converters were compared. The first approach was paralleling of two forward converters at their outputs (two-choke approach), whereas the second one was paralleling of two forward power stages at the input of the secondary LC filter (one-choke approach) to reduce the number of output inductors. It was demonstrated that the operation of the one-choke and two-choke converters is quite different and that the two-choke approach leads to significantly higher efficiency than its one-choke counterpart.

Another important issue for power converters is stability and dynamic performance which are characterized in the frequency domain by the loop gain, input and output impedances, and audio susceptibility. These characteristics can be obtained through converter small-signal modeling or through simulations. However, computed transfer functions often differ significantly from the measured ones. Therefore, the control design should always be verified by measurements.

General concepts of converter transfer function measurements have been known since the 1970s. The measurements are usually straightforward as long as the feedback signal is confined to a
single path. However, when the feedback signal propagates through several feedback loops, the identification of the transfer functions which should be measured and applied to the error amplifier (EA) design becomes challenging [46] and [86].

In [46], transfer functions of isolated converters with optocoupler feedback were considered. It was shown that depending on the point where the control loop is broken, two different plant transfer functions can be identified. However, one plant transfer function and the corresponding EA design provide a more meaningful relationship between the resulting loop gain and the converter response to line and load disturbances.

In [86], measurement of plant and control transfer functions was discussed for converters with remote output voltage feedback, for multi-output converters with the magnetic amplifier control, and for multi-output converters with the weighted-mode control. Methods of stabilizing an oscillating power supply in order to find the oscillation origin were also discussed.

Measurement of converter input and output impedances becomes very important in distributed power systems. When the output impedance of the upstream converter is close to or exceeds the input impedance of the downstream converter, oscillatory transients and even instability can occur. Practical issues of input/output impedance measurements of power converters were discussed in [67].

In [60], the loop gain measurement for the average-current-sharing control was presented. Since a proper point for breaking the loop exists only in the small-signal model, but not in the hardware, measurement of the current-sharing loop gain is hindered. It was shown that the measurement issue can be solved by exciting the current-sharing loop with two perturbation sources of the same magnitude and opposite phase. These perturbation sources can easily be implemented for two paralleled modules by using a three-winding transformer to split the excitation signal from a frequency response analyzer.

A. Isolated DC/DC

Generally, power conversion with a large step-down ratio, such as from 48 V to 1-2 V, can be efficiently performed only in topologies with a step-down transformer. For these isolated, low-output-voltage and high-output current converters, secondary-side power losses are dominant and, consequently, they have a major effect on the conversion efficiency.

A.1 Isolated PWM DC/DC

In [41] and [14], it was shown that the current-doubler rectifier (CDR) is a suitable secondary-side topology. In [41], the forward-flyback converter with CDR was evaluated and compared to the conventional forward converter. In [14], implementation of SRs in the symmetrical half-bridge converter with CDR was considered. SR gates were charged in the resonant fashion by the energy stored in the transformer leakage inductance and discharged through switches driven by control signals. The measured full-load efficiency of 82% was a remarkable achievement in the late 1990s.

Isolated PWM dc/dc converters at higher power levels (multi kW) are implemented with double-ended topologies, such as half-brIDGE, full-brIDGE, and push-pull, which have better utilization of the isolation transformer core than the single-ended topologies, such as forward and flyback, due to symmetrical operation of the transformer in the first and third quadrants of the core BH characteristics. However, in double-ended topologies, a small asymmetry in the switch driving signals and variations in the switch voltage drops during their on-times cause non-zero volt-seconds applied to the transformer windings, which can eventually lead to core saturation. This issue is typically solved by adding blocking capacitors in series with the transformer primary winding or by means of flux-balancing control. In the multi-kW converters, the blocking capacitors contribute substantially to the converter size and cost. This is even more pronounced in the bidirectional converters, where the blocking capacitors have to be placed on both sides of the transformer. In [83] and [84], flux-balancing control methods for the isolated bidirectional full-bridge converter with active clamp and for the isolated bidirectional dual active bridge converter were described. For both converters, discrete-time small-signal models of the flux-balancing loop were developed and used to determine stability and steady-state error of the proposed control.

A.2 Isolated Resonant DC/DC

In the early 2000s, a high-frequency (1.8 MHz) resonant-converter technology with phase-shifted control was introduced as a promising cost-effective solution for the next generation of microprocessor power supply systems. A detailed analysis of operation and a design procedure for the high-frequency resonant converter technology was presented in [77].

Isolated resonant dc/dc converters are also employed in contactless battery chargers. In many applications, contactless electrical energy transmission (CEET) has distinct advantages over conventional energy transmission that uses wires and connectors. The most popular CEET is the transmission of electric power through an inductive coupling. However, CEET through an inductive coupling has several problems achieving high efficiency and supplying a well-regulated output voltage. Because of the separated primary and secondary windings, the leakage inductance associated with the inductive coupling is much higher than that in a conventional transformer with well interleaved windings. Therefore, the energy stored in the leakage inductance causes high parasitic ringing and loss of energy. In [2], [7], [26], and [99], a soft-switched contactless resonant battery charger with local controller that is suitable for an efficient operation is described. The proposed control scheme consists of a primary-current feedback control circuit in the inverter side and an output-voltage feedback control circuit in the rectifier side. The proposed contactless battery charger significantly reduces circulating energy and related conduction losses and achieves ZVS not only of the inverter-side switches but also of the rectifier-side switches.

B. Non-Isolated DC/DC

Non-isolated VRMs are almost universally implemented with multi-phase, interleaved, synchronous-resonant buck converters and, in the majority of applications, they are powered from the 12-V output of an ac/dc power supply.

Due to the very low output voltage, the duty cycle of the 12-V input VRMs is very narrow, i.e., it is only around 10%. Moreover, with anticipated future reductions of the microprocessor supply voltage, the duty cycle will be reduced even further. Generally, a small duty cycle has a detrimental effect on the VRM efficiency and the load transient response. In addition, a very small duty cycle limits the maximum attainable switching frequency because the conduction time of the buck switch cannot be lower than the sum of the rise and fall times of its driving voltage. A family of multi-phase PWM converters that provide extended duty cycle was introduced in [53]. Due to the high input-to-output gain characteristics, the proposed multi-phase step-down converters operate with larger duty cycles and lower voltage stress on the switches than their conventional buck converter counterparts.

One of the early publications about VRMs was [11], where the effects of the slew rate, interconnect inductance, and on-board capacitance on the VRM load transient response were analyzed.
Ref. [11] was also one of the first papers to propose a design procedure for the VRM output LC filter.

In [5], both efficiency and transient response of a VRM were considered. It was shown that reduction of the VRM output filter inductance, which is beneficial for the load transient response, causes a significant increase of the buck switch turn-off loss and degradation of efficiency. It was also shown that the driving loss of the VRM switches and SRs, considering the MOSFET devices available at that time, were substantial contributors to the overall VRM loss. To reduce the driving loss, which occur mostly in the SRs, a new resonant SR gate-driving circuit was proposed and evaluated in [5]. It was also demonstrated that PWM with a variable-slope ramp can considerably improve the VRM output voltage regulation during load transients.

In [3], an LED driver with adaptive drive voltage was proposed. The driver circuit consists of multiple linear current regulators and a voltage preregulator whose output voltage is automatically adjusted to a minimum voltage required to maintain the desired current through the linear regulators. Specifically, in the proposed driver, the voltage across the linear regulator in the LED string that exhibits the highest voltage drop is always self-adjusted to the lowest voltage possible. As a result, the proposed LED driver exhibits significantly higher efficiency than its counterpart without the adjustment of the drive voltage.

A special group of the non-isolated dc/dc converters is employed in dual input-voltage power supplies. In fact, telecommunication and computer networking industries use 48-V dc-bus distributed power systems, which are backed up by 48-V dc battery plants for their reliability, availability, and reserve time in case of ac power outages. As a result, powering converters from a 48-V dc bus and from a universal ac-line is a common requirement for telecommunication and computer networking industries. Present specifications of power supplies for networking computer applications already call for designs with a universal ac-line input and a 48-V nominal dc input. The requirement for the dual input-voltage power supplies puts a significant burden on the power supply manufacturers because of the additional efforts and resources necessary to design, manufacture, and handle two versions of power supplies. Furthermore, since the quantity of the dc-input version is still a small fraction of the quantity of the ac-input version, the additional engineering effort required for the design of the dc-input version may not be profitable. To minimize the effort and resources required for the design of power supplies that operate using dual input sources, a modular design approach is a suitable choice. In this approach, the ac- and dc-input versions of power supplies use different front ends and the same output stage. Specifically, the ac-input version employs a PFC boost-converter front end, whereas the dc-input version uses a dc-dc converter with a high input-to-output voltage gain. The modular design does not require any redesign of the output stage since both front ends provide the same input voltage to the output stage (typically 380 V).

In [19], a dc-input front-end for a server power supply for networking applications was implemented by using two cascaded boost converters. A two-inductor boost converter that is more suitable for a dc-input front-end converter of the modular design approach was introduced in [8], [17], [98], and [100].

IV. REVIEW PAPERS

Milan summarized his vast experience, expertise, and vision in power electronics technologies in several review-type papers. In [112]-[114], the past, present, and future of power conversion technologies for computer, networking, and telecom power systems were discussed. Meeting the continuously increasing power density and efficiency requirements required significant technology advancements in system architectures, devices and materials, topology optimization, and packaging/thermal design. Major technology challenges and future trends in each of these key technology areas were identified and briefly discussed.

In [13] and [110], various distributed power systems were discussed, including dc and ac bus architectures. Distributed power systems have been replacing centralized power systems in many applications where higher distribution efficiency, better load regulation, increased flexibility, maintainability, redundancy, and better power and heat management were the primary considerations. Benefits and challenges of distributed power systems in various applications were summarized. While the dc-bus distribution power systems have been proven to meet the performance requirements of desktop and server power systems, in the early 2000s many claims were made that a high-frequency ac-bus distribution power system was a more cost-effective solution to power future data-processing equipment. In [38], a constant-frequency inverter with phase-shift control was proposed for the ac-bus distribution power system. This inverter employed a coupled inductor to achieve ZVS in a wide range of load currents and input voltages with reduced circulating energy.

In [4], high-performance, active PFC techniques for high-power, single-phase applications were reviewed. Merits and limitations of several PFC techniques that were used in the 1990s until the mid-2010s in network, server, and telecom power supplies to maximize their conversion efficiency were discussed. These techniques include various ZVS and ZCS active-snubber approaches employed to reduce reverse-recovery-related switching losses, as well as techniques for the minimization of the conduction losses. The effect of recent advancements in semiconductor technology, primarily silicon-carbide technology, on the performance and design considerations of PFC converters were also discussed.

Finally, in [71], general properties of the resonant, quasi-resonant, multi-resonant, and PWM soft-switching techniques were summarized. Merits and limitations of each technique were discussed, and their most suitable application areas were defined.

V. CONCLUSIONS

The review of Milan M. Jovanović’s work is essentially the history of power electronics technologies for modern server, telecom, and portable data-processing equipment, as well as for on-board electric vehicle applications in the last 35 years. While in the past the major performance improvements were brought about primarily by refinements in power converter topologies and advancements in semiconductor and magnetic material, future efficiency and power density improvements are expected to come mostly from system architecture and power management optimization as well as from advancements in packaging and thermal management techniques. The impact of Milan’s work on the power electronics industry is enormous. Power conversion technologies developed by research teams led by Milan have been employed in hundreds of millions of power supplies made by Delta Electronics and other manufacturers, enabling further miniaturization of electronics equipment and resulting in enormous cumulative energy savings and electronic-material waste reduction. Milan’s legacy will live through the R&D work of thousands of power electronics engineers worldwide, who will find inspiration in his great achievements and vision. To honor Milan’s work, Delta’s Advanced R&D Power Electronics Laboratory in Research Triangle Park, NC, USA has been named the Milan M. Jovanović Power Electronics Laboratory.


