Single-Stage Flyback Power-Factor-Correction Front-End for HB LED Application

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Abstract — **This paper presents a single-stage flyback power-factor-correction (PFC) front-end for high-brightness light-emitting-diode (HB LED) applications. The proposed PFC front-end circuit combines the PFC stage and the dc/dc stage into a single stage. Experimental results obtained on a 78-W (24-V/ 3.25-A) prototype circuit show that at V_{IN} = 110 Vac, the proposed PFC front-end for HB LED applications can achieve an efficiency of 87.5%, a power factor of 0.98, and a total harmonic distortion (THD) of 14% with line-current sharmonics that meet the IEC 61000-3-2 Class C standard.**

Index terms — Driver, high-brightness light emitting diodes (HB LEDs), power factor correction (PFC), single-stage, flyback

I. INTRODUCTION

The technology and performance of high-brightness light-emitting diodes (HB LEDs) has undergone significant improvements driven by new applications in liquid-crystal-display (LCD) backlighting, automobiles, traffic lights, and general-purpose lighting [1]-[3]. As a solid state light source which does not contain mercury, HB LEDs have been widely accepted because of their superior longevity, low-maintenance requirements, and continuously-improving luminance, and they have great potential to replace existing lighting sources such as incandescent lamps and fluorescent lamps in the future.

For LED drivers with an output power over 25 W in general lighting applications, the input line current harmonics need to satisfy the limits set by IEC 61000-3-2 Class C regulations [4]. With passive power-factor-correction (PFC), which uses only inductors and capacitors, it is difficult to meet such requirements, and the size of the passive PFC components is bulky.

An LED driver with active PFC, which is implemented with two stages, is shown in Fig. 1. The first stage can achieve a near unity power factor and a low THD at universal input voltage range, while the second stage is used for the dc/dc conversion. However, the circuit in Fig. 1 has two independent feedback controls and a high component count, leading to an increased cost and size. In low-power lighting applications, where cost is the dominant issue, such an approach loses appeal.

Another active PFC implementation employs a single-stage ac/dc converter [5]-[13], where the PFC stage is integrated with the dc/dc stage, resulting in a reduced complexity and cost. There are two embodiments of the single-stage PFC ac/dc converters: without and with a bulk capacitor at the primary side, as illustrated in Figs. 2 and 3, respectively. Although the flyback single-stage PFC circuit in Fig. 2 [5] has the advantage of a low component count, its output voltage has a high ripple at twice the line frequency unless very large output capacitors are used. For an LED load, a small change in the driving voltage results in an increase of the LED current by orders of magnitude. Therefore, with this approach, a post-regulator is often required, which adds cost and lowers the efficiency.

The flyback single-stage PFC topology shown in Fig. 3 [11] presents one of the most cost-effective single-stage solutions. In this converter, the PFC stage operates in discontinuous conduction mode (DCM), while the dc/dc stage operates at the DCM/CCM boundary. A low input-current harmonic distortion can be achieved due to the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle is held relatively constant during a half line cycle. However, voltage V_B across bulk capacitor C_B is unregulated and at high lines it can increase to non-practical levels. To reduce the bulk capacitor voltage, one terminal of the boost inductor winding is connected to a tapping point of the primary winding of the flyback transformer, which provides a negative magnetic feedback. This solution has been successfully applied in adapter/charger applications for the universal line voltage, where the line current harmonics need to meet IEC 61000-3-2 Class D limits. However, the tapping of the flyback primary winding also results in a zero-crossing distortion due to the dead angle, as shown in Fig. 4. In fact, as long as the instantaneous line voltage is lower than the feedback voltage at the tapping point, no current is drawn from the input, which deteriorates the power factor and the line-current harmonics.

Therefore, applying the flyback single-stage PFC topology in Fig. 3 for lighting applications, where the line-current harmonics have to meet the more stringent limits set by IEC 61000-3-2 Class C standard, presents a challenging task, especially when the input voltage is universal.

In this paper it is shown that by optimizing the location of the tapping point of the primary-winding, the boost inductor, and the flyback transformer, high power factor and low THD can be achieved such that the line current harmonics meet the limits set by the IEC 61000-3-2 Class C standard, with a

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relatively high efficiency, if the line voltage range is limited to either the universal low-voltage (90 -140 V AC) or high-voltage range (180 - 276 V AC).

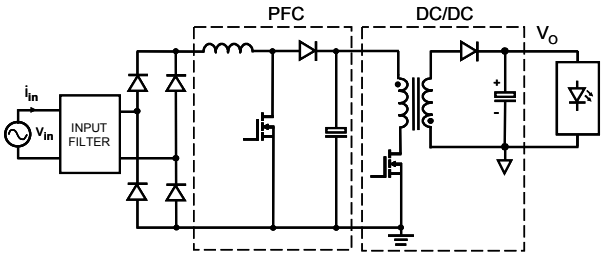


Fig. 1. Conventional two-stage LED driver

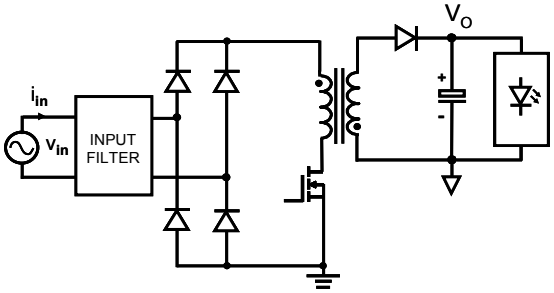


Fig. 2. Single-stage flyback LED driver without intermediate bus capacitor

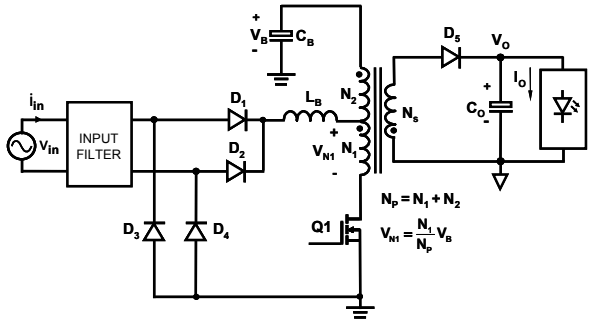


Fig. 3. Proposed PFC front-end for HB LED application

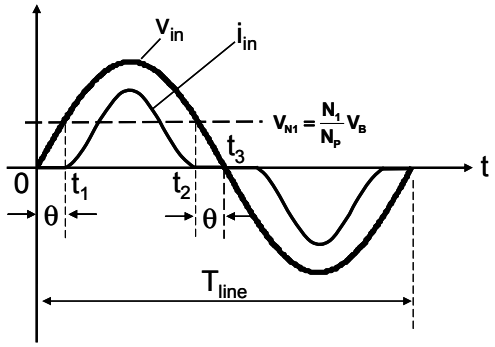


Fig. 4. Input voltage and current waveforms of the proposed PFC front-end

II. Operation of Proposed Single-Stage PFC Front-End for HB LED Application

To facilitate the understanding of operation, Fig. 5 shows the topological stages while Fig. 6 shows the key waveforms of the proposed PFC front-end for HB LEDs. There are five basic operation modes. Detailed description of each mode is given below assuming that input voltage is positive.

1) *Mode (a)*: Switch Q_1 is turned on at $t = T_0$, no current flows through the secondary winding N_S because diode D_5 is reverse biased. The sum of inductor current i_{LB} and discharging current i_{CB} of bulk capacitor C_B flows through the switch. Magnetizing current i_M of the transformer increases linearly with a slope of V_B/L_M, where L_M is the magnetizing inductance of the transformer, and V_B is the voltage across bulk capacitor C_B, respectively. When input voltage is higher than $(N_1/N_P)V_B$, inductor current i_{LB} can flow because diodes D_1 and D_4 are forward biased, otherwise, no current i_{LB} can flow. Inductor current i_{LB} increases linearly with a slope of $(v_{in}-(N_1/N_P)V_B)/L_B$. Magnetizing current i_M of the flyback transformer is a function of i_{LB} and i_{CB}, and can be expressed as

$$i_M = i_{CB} + \frac{N_1}{N_P} i_{LB} \tag{1}$$

It can be seen that during the on-time of switch Q_1, energy from two sources is stored in the flyback transformer. Namely, part of the magnetizing energy is supplied from the bulk capacitor, whereas part of the energy is supplied directly from the line. Generally, direct energy storage from the line improves the conversion efficiency.

2) *Mode (b)*: Switch Q_1 is turned off at $t = T_1$. Magnetizing current i_M continues to increase, and output capacitor C_{OSS} of switch Q_1 is charged by the sum of currents i_{LB} and i_{CB} until the voltage across capacitor C_{OSS} reaches $(V_B + nV_O)$, where $n = N_P/N_S$.

3) *Mode (c)*: Switch Q_1 is turned off but diode D_5 conducts at $t = T_2$. Energy stored in the transformer is released to the secondary side, inductor current i_{LB} decreases and continues to flow through primary winding N_2 to charge the bulk capacitor, i.e., $i_{CB} = i_{LB}$. The downslope of the inductor current i_{LB} is given by

$$\frac{di_{LB}}{dt} = -\frac{V_B + V_O(N_2/N_S) - v_{in}}{L_B} \tag{2}$$

Magnetizing current i_M can be expressed as

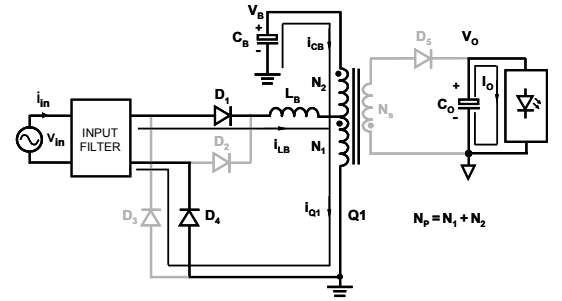
$$i_M = \frac{N_S i_S - N_2 i_{CB}}{N_P} = \frac{N_S i_S - N_2 i_{LB}}{N_P} \tag{3}$$

Rearranging (3) gives secondary current i_S as expressed by (4)

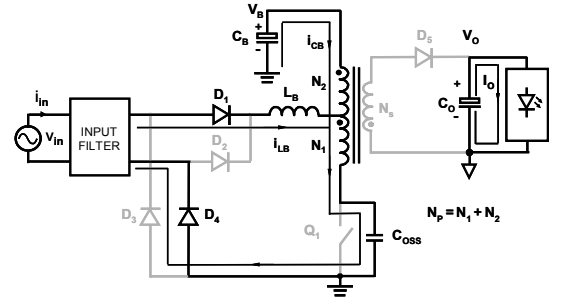
$$i_S = \frac{N_P}{N_S} i_M + \frac{N_2}{N_S} i_{LB} = n i_M + \frac{N_2}{N_S} i_{LB}. \tag{4}$$

It can be seen from (4) that during the off time, secondary current i_S is composed of two components, namely, the reflected magnetizing current and the reflected primary current which draws energy directly from the input line. Generally, direct energy transfer from the line to the output improves the conversion efficiency.

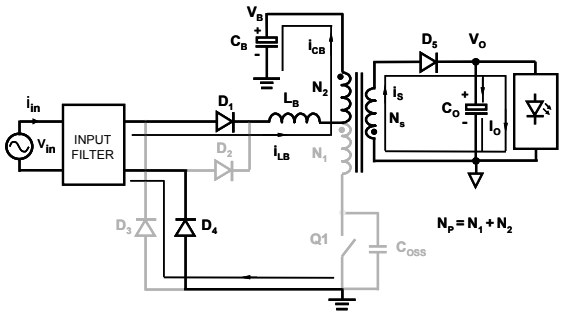
4) *Mode (d)*: Switch Q_1 is turned off and inductor current i_{LB} reaches zero at $t = T_3$. Energy stored in the transformer continues to be released to the secondary side.



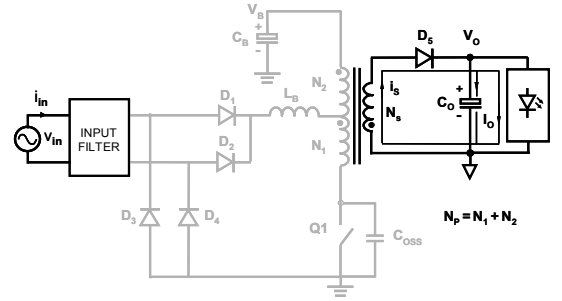
(a) T_0 - T_1



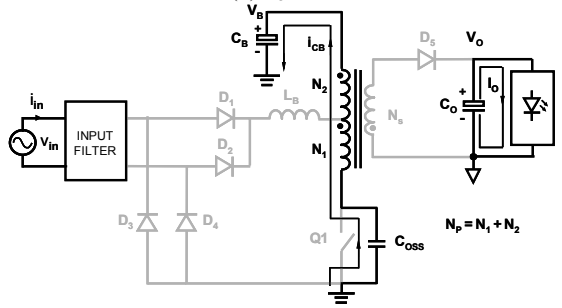
(b) $T_1 – T_2$



(c) $T_2 – T_3$



(d) $T_3 – T_4$



(e) $T_4 – T_5$

Fig. 5. Topological stages of the proposed PFC front-end at different operation modes

5) *Mode (e)*: Switch Q_1 remains turned off and secondary current i_S falls to zero at $t = T_4$. Capacitor C_{OSS} and magnetizing inductance L_M forms a series resonant circuit. During the resonance switch voltage decreases and reaches a minimum of $(V_B\text{-}nV_O)$, and the switch is turned on again at this moment ($t = T_5$), achieving partial zero-voltage switching.

When the input line voltage is negative, the five operation modes are the same except the input current flows through diodes D_2 and D_3 instead of diodes D_1 and D_4.

II. Analysis of the Bulk Capacitor Voltage

Since the intermediate bus voltage of the proposed PFC front-end is unregulated, the effect of input current shaping inductor L_B and the flyback transformer must be thoroughly understood to avoid over voltage of capacitor C_B. To simplify the analysis, the following assumptions were made.

1) The line voltage is a pure ac sine wave, given by

$$v_{in}(t) = \sqrt{2}V_{IN}\sin(2\pi f_{line}t) \tag{5}$$

where V_{IN} and f_{line} are the root-mean-square value and frequency of the input voltage, respectively.

2) The input voltage is constant in a switching cycle since the switching frequency is much higher than the line frequency.

3) The bulk capacitor voltage is ripple-free because the bulk capacitor is sufficiently large.

4) All semiconductors are ideal. The leakage inductance of the flyback transformer is neglected.

When switch Q_1 is turned on the voltage across winding N_1, V_{N1}, is $V_B(N_1/N_P)$. The input current i_{in} is zero when input voltage v_{in} is lower than V_{N1} during period $[0, t_1]$ and $[t_2, t_3]$ in a half line cycle, as shown in Fig. 4. t_1 to t_3 are defined as

$$t_1 = \frac{\arcsin(V_{N1}/(\sqrt{2}V_{IN}))}{2\pi}T_{line}, \tag{6}$$

$$t_2 = \frac{T_{line}}{2} - t_1, \tag{7}$$

and

$$t_3 = \frac{T_{line}}{2}. \tag{8}$$

where T_{line} is the time period of one line cycle of the input voltage.

Referring to Fig. 6, the increase of inductor current i_{LB} during turn-on time of switch Q_1 is given by

$$\Delta i_{LB} = (v_{in}(t) - \frac{N_1}{N_P}V_B)D_1T_S / L_B, \tag{9}$$

From the voltage-second balance of the boost inductor

$$[v_{in}(t) - V_{N1}]D_1T_S = [V_B + (N_2/N_P)V_O - v_{in}(t)]D_2T_S \tag{10}$$

D_2, which is the reset time of the inductor core to switching period T_S, can be given as

$$D_2 = \frac{(V_{in}(t) - V_{N1})D_1}{V_B + \frac{N_2}{N_P}V_O - V_{in}(t)} = \frac{(V_{in}(t) - V_{N1})D_1}{V_B + n(1-n_1)V_O - V_{in}(t)}, \tag{11}$$

where $n_1 = N_1/N_P$.

Duty cycle D_1 of switch Q_1 can be obtained based on the voltage-second balance of the flyback transformer, as expressed by (12).

$$D_1 = \frac{nV_O}{V_B + nV_O} \tag{12}$$

The changes of secondary current i_S during time period $[D_1T_S, (D_1+D_2)T_S]$ and $[(D_1+D_2)T_S, T_S]$ can be obtained from (4) as

$$\Delta i_{S\_1} = (n\Delta i_M + \frac{N_2}{N_S}\Delta i_{LB})\Big|_{D_1T_s}^{(D_1+D_2)T_s} = \frac{n^2V_O}{L_M}D_2T_S + n(1-n_1)\Delta i_{LB} \tag{13}$$

and,

$$\Delta i_{S\_2} = (n\Delta i_M)\Big|_{(D_1+D_2)T_s}^{T_s} = \frac{n^2V_O}{L_M}(1-D_1-D_2)T_S \tag{14}$$

Output current I_O is the average of secondary current i_S, i.e.,

$$I_O = \frac{1}{2}\Delta i_{S\_1}D_2 + \frac{1}{2}\Delta i_{S\_2}(D_2 + (1-D_1)) \tag{15}$$

Combining (9) to (15) gives switching cycle T_S as

$$T_S = \frac{2I_O}{\left(\frac{n^2V_O}{L_M}D_2 + \frac{n(1-n_1)(v_{in}(t)-n_1V_B)D_1}{L_B}\right)D_2 + \frac{n^2V_O}{L_M}((1-D_1)^2 - D_2^2)} \tag{16}$$

The average current of the boost inductor in a switching cycle is

$$\overline{i_{LB}} = \frac{1}{2}\Delta i_{LB}(D_1+D_2) = \frac{1}{2L_B}(v_{in}(t)-V_{N1})D_1(D_1+D_2)T_S$$
$$= \frac{I_O(v_{in}(t)-V_{N1})D_1(D_1+D_2)}{(\alpha n^2V_OD_2 + n(1-n_1)(v_{in}(t)-n_1V_B)D_1)D_2 + \alpha n^2V_O((1-D_1)^2-D_2^2)} \tag{17}$$

where $\alpha = L_B/L_M$.

The energy absorbed by the circuit from the source during a half line cycle is the integral of the product of instant voltage and average current at the same time, which is given by

$$E_{in} = \int_{t_1}^{t_2}\left(v_{in}(t)\overline{i_{LB}}\right)dt \,. \tag{18}$$

In a half line cycle, the input energy is equal to the output energy at steady state

$$E_{in} = E_{out} \,. \tag{19}$$

The output energy during a half line cycle is given by

$$E_{out} = P_OT_{line}/2 \tag{20}$$

V_B can then be found by combining (11), (12) and (16) to (20).

Bus voltage V_B is a function of input voltage V_{IN}, ratios α and n_1 for a given ratio n and output voltage V_O. Figure 7 shows the plot of bus voltage V_B vs. input voltage V_{IN}. Voltage V_B changes with input voltage V_{IN} almost linearly for a fixed ratio α, n, and n_1. Therefore, the voltage rating of bus capacitor C_B is strongly dependent on the maximum input voltage. A higher ratio n_1, i.e., a higher number of turns of the feedback winding N_1, results in a lower voltage V_B. The effect of ratio n_1 on voltage V_B is further illustrated in Fig. 8. For n = 6, α = 0.25, V_{IN} = 270 V and V_O = 24 V, bus voltage V_B can be reduced to 370 V from 600 V if ratio n_1 is increased to 0.5 from 0 (i.e., N_1 = 0 in the case without feedback winding N_1).

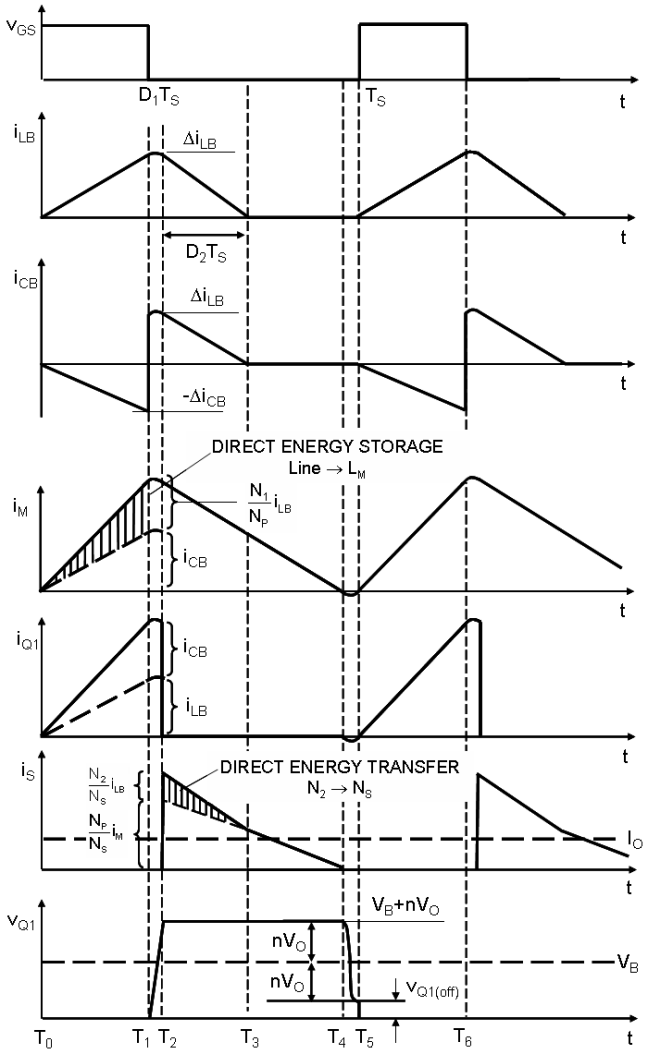


Fig. 6. Key waveforms of the proposed PFC front-end

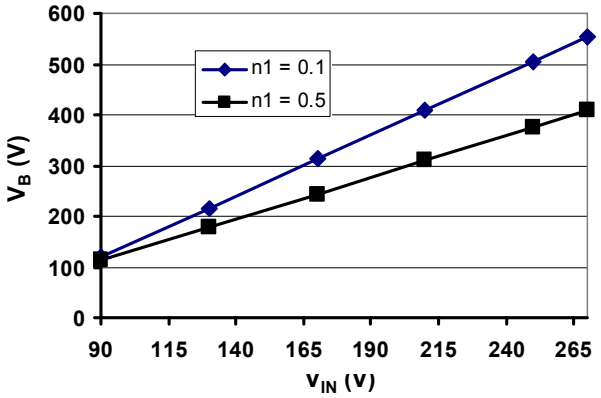


Fig. 7. Plot of bus voltage V_B vs. input voltage V_{IN} (α = 0.25)

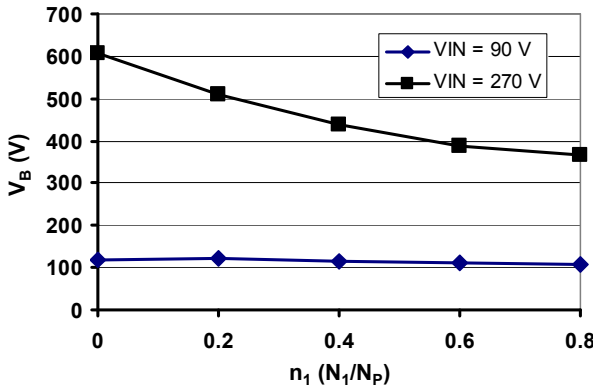


Fig. 8. Plot of bus voltage V_B vs. ratio n_1 of N_1 to N_P

The ratio α of L_B to L_M also has significant effect on the bus voltage. Fig. 9 shows the plot of bus voltage V_B vs. ratio α for two different input voltages (V_{IN} = 90 V and V_{IN} = 270 V). As can be seen from the plot, a higher ratio α, i.e., a higher inductance L_B or a lower magnetizing inductance L_M of the flyback transformer generates a lower bus voltage V_B. This can be understood that when inductance L_B increases, the change of inductor current Δi_{LB}, i.e., the stored magnetic energy of inductor L_B, also decreases, and charging current i_{CB} to capacitor C_B becomes lower, resulting in a lower bus voltage. A lower magnetizing inductance L_M of the flyback transformer results in higher discharging current i_{CB} from bulk capacitor C_B, and, therefore, a lower bus voltage. When V_{IN} = 270 V, the bus voltage can be reduced to 410 V from 585 V if ratio α is increased from 0.2 to 0.5. Bus voltage V_B can even be lower than the input voltage as ratio α continues to increase. As shown in Fig. 10, V_B drops to below input voltage V_{IN} (= 90 V) when ratio α is higher than 0.4.

When a sinusoidal input voltage is applied and the instantaneous input voltage is low, a lower V_B can still ensure the core of inductor L_B is fully reset before switch Q_1 is turned on and inductor L_B operates in DCM. The reason is that the voltage-second for inductor L_B in this case is low during turn-on time of switch Q_1 but the reset voltage (= $V_B + n_2V_O - v_{in}$) for the core is sufficient since input voltage v_{in} is low. However, at the peak of the input voltage, a lower bus voltage V_B not only increases the voltage-second for inductor L_B during turn-on time of switch Q_1, but also causes insufficient reset voltage for the core of inductor L_B since v_{in} is high, inductor L_B may enter CCM operation and lead to severe input line current distortion, as will be verified by the experiment in the next section. As can also be seen from Fig. 10, voltage V_B drops at a faster speed with ratio α when V_{IN} = 90 V compared to the case with V_{IN} = 270 V. As a result, when the input is universal, a certain ratio α may ensure DCM operation of inductor L_B and no severe input line current distortion occurs at high line, but may cause CCM operation of inductor L_B and undesired input line current distortion at low line. Therefore, the proposed PFC front-end is not suitable for universal input voltage unless a variable ratio α, i.e., a variable inductance of input current shaping inductor is realized. However, this inevitably increases the complexity of the circuit and the overall cost.

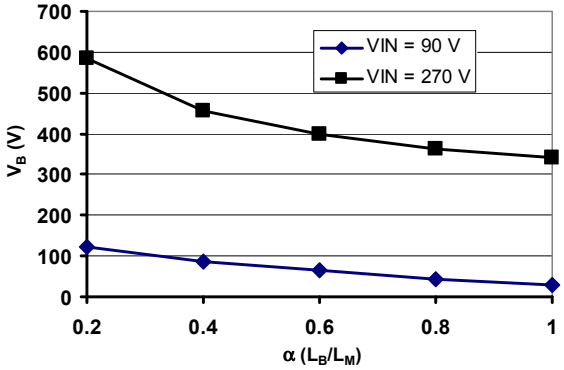


Fig. 9. Plot of bus voltage V_B vs. ratio α of L_B to L_M (n_1 = 0.133)

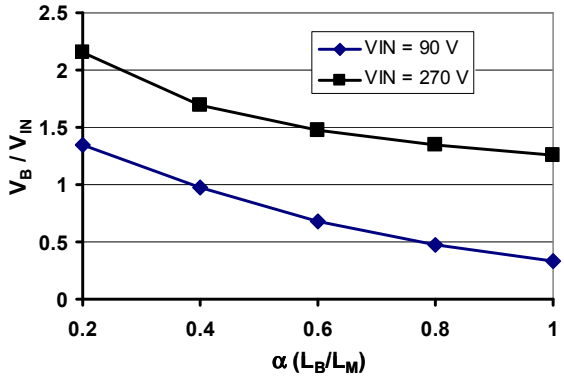


Fig. 10. Plot of normalized bus voltage with respect to input voltage vs. ratio α of L_B to L_M (n_1 = 0.133, and n = 6)

IV. Performance Evaluation

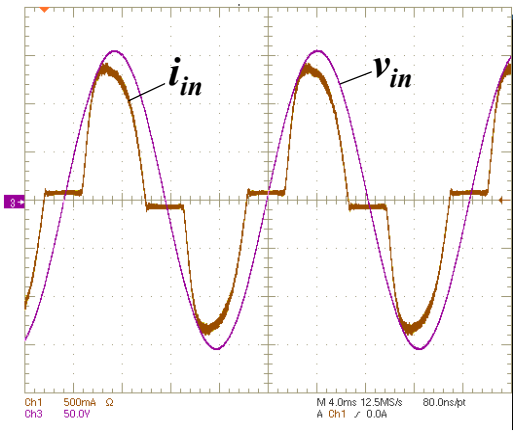
A PFC front-end employing the proposed scheme has been built and experiments have been carried out to verify the analysis in the previous section and demonstrate its performance. Table I lists the key components. Figure 11 shows the measured line current and voltage waveforms at V_{IN} = 110 V AC (60 Hz) on a prototype of proposed PFC front-end with an output voltage V_O = 24 V and output current I_O = 3.25 A. With a ratio α = 0.16 (L_B = 83 µH and L_M = 530 µH) and n_1 = 0.5 (N_1 = N_2 = 12 turns), measured THD, PF, V_B, and efficiency are 34.95%, 0.9284, 166.2 V, and 88.65%, respectively. When L_B is increased to 166 µH, i.e., ratio α = 0.31, measured THD, PF, V_B, and efficiency are 40.56%, 0.9014, 147.2 V, and 89.11%, respectively. It can be seen that a higher boost inductance L_B lowers bus voltage V_B, which agrees with the theoretical analysis. Better efficiency results when the boost inductance is increased since the peak inductor current decreases with lower switching loss and conduction loss. However, as inductance L_B increases, bus voltage V_B decreases, leading to a lower reset voltage for inductor L_B. As a result, inductor L_B might not be completely reset during turn-off time of switch Q_1, and enters CCM operation at the peak of input voltage, significantly deteriorating the power factor and THD. Measured

waveforms in Fig. 12 (b) show that inductor L_B enters CCM operation from DCM operation after L_B is increased, and serious distortion of the line current at the peak can be observed, as shown in Fig. 11 (b).

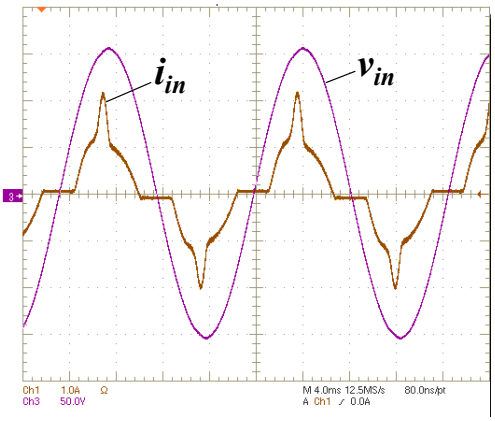
TABLE I
LIST OF KEY COMPONENTS

Flyback transformer	L_M = 645 µH core: PJ33/19 Primary: 30 turns, ∅0.55 Secondary: 5 turns, ∅0.5×3 TIW
Q_1	SPP15N65C3, 650 V, 15 A
D1-D4	STTH3L06U, 600 V, 3 A
D5	STPS20H100CT, 100 V, 20 A
C_O	2×1000 µF/25 V
C_B	120 µF/420 V
Inductor L_B	415 uH for high line, 166 µH for low line, core: RM10, 32 turns, ϕ0.1×60
Controller	NCP1207 ON Semiconductor

The tapping location also has significant effect on THD and PF as well as efficiency and bus voltage. Generally a higher ratio n_1 (= N_1/N_P) leads to a lower bus voltage, poorer PF and THD, but better efficiency because of a higher feedback winding voltage and stronger direct energy storage/transfer capability. With N_1 = N_2 = 12 turns, the sampled voltage across winding N_1 is half the bus voltage. In the case of L_B = 166 µH, the voltage at the tapping point of the primary winding of the flyback transformer is 73.6 V. Consequently, there is no input current flowing as long as the instantaneous input voltage is less than 73.6 V. As can be seen from Fig. 11, there is a long dead time during which no current flows through boost inductor L_B, leading to a high THD and low PF. However, when N_2 = 16 turns and N_1 = 8 turns, i.e., n_1 = 0.33, the measured PF is 0.97 and THD is reduced to 19.85% while the bus voltage is increased to 152 V from 147.2 V and the efficiency drops to 88.78%. Therefore, the tapping location as well as inductor L_B have to be optimized in order to have a good efficiency while meeting the THD and PF requirements.

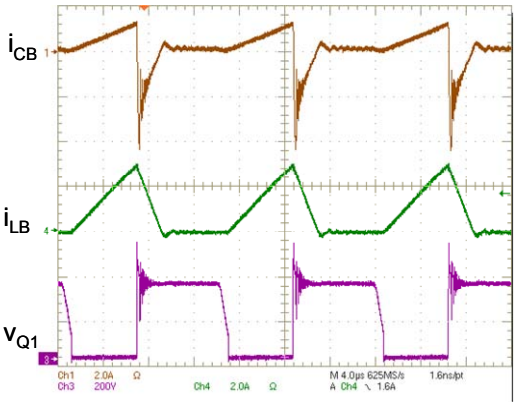


(a) L_B = 83 µH

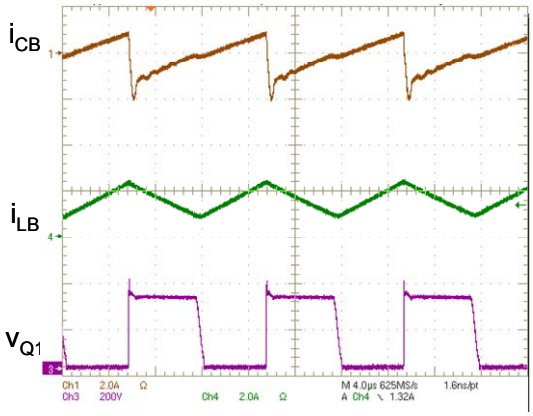


(b) L_B = 166 µH

Fig. 11. Measured line current and voltage waveforms at V_{IN} = 110 V AC with N_1 = N_2 = 12 turns, (a) L_B = 83 µH; (b) L_B = 166 µH



(a) L_B = 83 µH



(b) L_B = 166 µH

Fig. 12. Measured current and voltage waveforms, (a) L_B = 83 µH; (b) L_B = 166 µH. CH1: Current of primary winding N_2, CH4: Current of inductor L_B; CH3: Drain-to-source voltage of switch Q_1. Voltage scale: 200 V/div., current scale: 2 A/div., time scale: 4 µs/div.

Figure 13 shows the measured waveforms of line voltage and current at V_{IN} = 110 V AC and P_O = 78 W with an improved design for n_1 = 0.133 and α = 0.26 (N_1/ N_2 = 4/26, L_B = 166 µH and L_M = 645 µH). Measured PF and THD are

0.9855 and 14%, respectively, which are significantly improved compared to the case with $n_1 = 0.5$ ($N_1/N_2 = 12/12$). The percentage of 2nd to 11th harmonic current to the fundamental current is shown in Fig. 14, all below the Class C limit. The plot of measured efficiency vs. input voltage for different loads at low line is shown in Fig. 15. An efficiency of 87.5% is achieved at V_{IN} = 110 V AC and P_O = 78 W, with a measured V_B of 169.8 V, very close to the predicted 164.8 V.

Further experiments have been done to validate the proposed PFC front-end and the theoretical analysis at high line. Figure 15 shows the measured line current and voltage waveforms while Fig. 16 shows the plot of efficiency vs. input voltage at high line with $n_1 = 0.133$ and $\alpha = 0.64$ (N_1/N_2 = 4/26, L_B = 415 µH, and L_M = 645 µH). The measured PF, THD, bus voltage, and efficiency at V_{IN} = 220 V AC are 0.95, 12.72%, 308 V, and 90.39%, respectively. The percentage of 2nd to 11th harmonic current to the fundamental current at P_O = 89 W is shown in Fig. 17, all below the Class C limit. It is noted that at high line, an inductance L_B of 415 µH is used instead of 166 µH in order to improve the efficiency and limit the voltage of capacitor C_B at maximum input voltage. At V_{IN} = 274V, the predicted bus voltage is 396.6Vwith a 1.7% error compared to the measured 403.3V

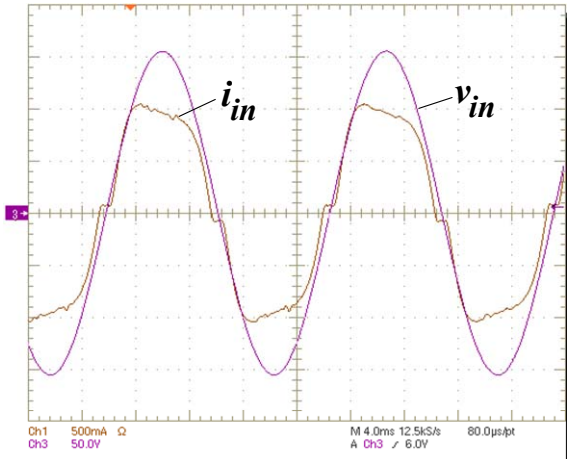


Fig. 13. Measured line voltage and current waveforms at V_{IN} = 110 V AC with N_1/N_2 = 4/26, L_B = 166 µH, and L_M = 645 µH

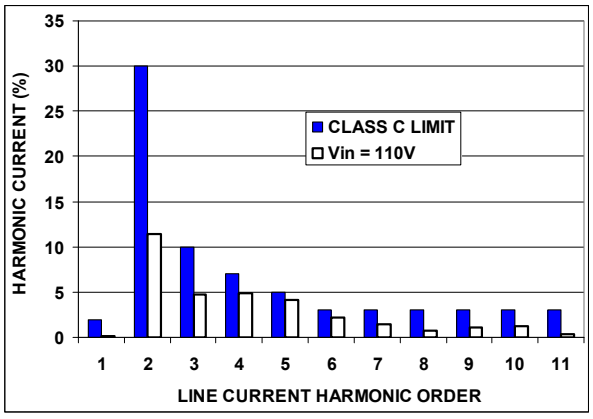


Fig. 14. Measured line current harmonics at low line

Measurements with actual LED load have also been made. Four LED strings with 7 series-connected white LEDs (Philips Lumileds, LXHL-LW3C) in each string were paralleled and directly driven by the proposed PFC front-end prototype with an output voltage of 24 V. The measured total LED current and output voltage ripple at twice the line frequency is shown in Fig. 19. The peak-to-peak ripple of output voltage is less than 20 mV at I_O = 3.8 A resulting in a very low LED current ripple. Therefore, the proposed PFC front-end is suitable for directly driving LED strings, and no post-regulators are necessary, which is a significant advantage over the conventional flyback PFC without intermediate bus voltage. Furthermore, the proposed PFC front-end also has significant size reduction, as can be seen from Fig. 20.

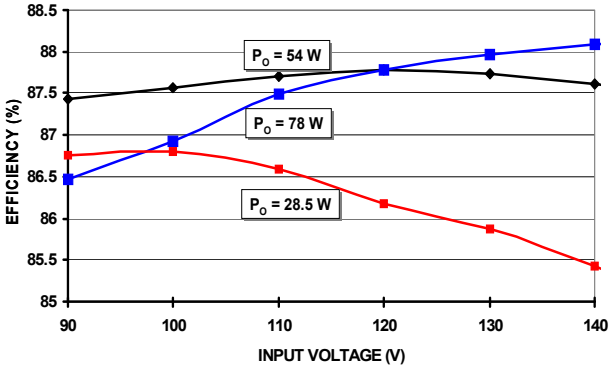


Fig. 15. Measured efficiency vs. input voltage at low line

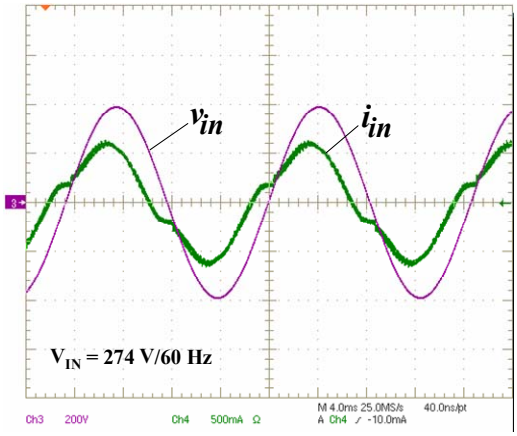


Fig. 16. Measured line voltage and current waveforms at V_{IN} = 274 V AC with N_1/N_2 = 4/26, L_B = 415 µH, and L_M = 645 µH

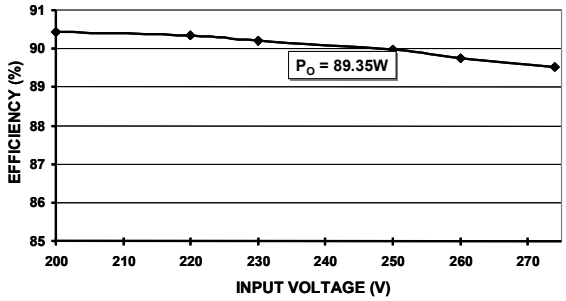


Fig. 17. Measured efficiency vs. input voltage at high line

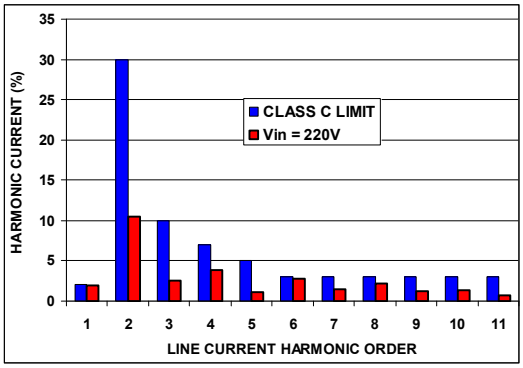


Fig. 18. Measured line current harmonics at high line

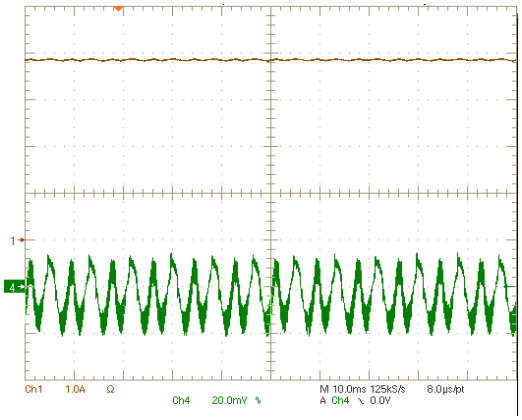


Fig. 19. Measured total LED current and output voltage ripple at V_{IN} = 220 V AC. CH1: LED current, scale: 1 A/div.; CH4: Output voltage ripple, scale: 20 mV/div; Time scale: 10 ms/div.

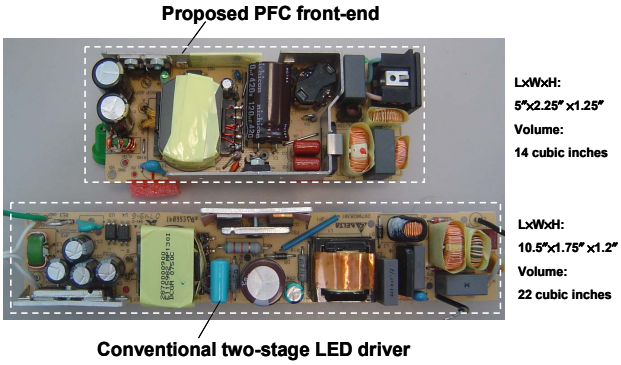


Fig. 20. Photo of the proposed PFC front-end and a conventional two-stage LED driver for size comparison

V. SUMMARY

A single-stage flyback power-factor-correction front-end for HB LED application is presented in this paper. With the integration of the PFC stage and dc/dc stage, significant reduction of component count, size, and cost can be achieved. Experimental results obtained on a prototype show that at V_{IN} = 110 V AC, V_O = 24 V, and I_O = 3.25 A, the proposed PFC front-end for LED driver has achieved an efficiency of around 87.50%, a power factor of 0.98 and a total harmonic distortion (THD) of 14% for the line current with harmonic contents meeting IEC 61000-3-2 Class C standard. Experimental results have also been obtained at high line when the inductance of the input current shaping inductor is increased. Measured output voltage ripple with an actual LED load at V_O = 24 V, I_O = 3.8 A is less than 20 mV. Therefore, LED strings can be directly driven without a post-regulator, improving the efficiency, lowering the cost, and reducing the size.

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