A New ZVS-PWM Full-Bridge Converter

Yungtaek Jang and Milan M. Jovanović

Delta Products Corporation
Power Electronics Laboratory
P.O. Box 12173, 5101 Davis Dr.
Research Triangle Park, NC 27709, U.S.A.

Yu-Ming Chang

DELTA Electronics Inc.
3, Tung Yuan Road,
Chungli Taiwan, R.O.C.

Abstract — A full-bridge converter which employs a coupled inductor to achieve zero-voltage switching of the primary switches in the entire line and load range is described. Because the coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifier. The operation and performance of the proposed converter is verified on a 670-W prototype.

1. Introduction

The full-bridge (FB) zero-voltage-switching (ZVS) PWM converter shown in Fig. 1 is the most widely used soft-switched circuit in high-power applications, [1]-[4]. This constant-frequency converter features ZVS of the primary switches with relatively small circulating energy. The control of the output voltage at constant frequency is achieved by the phase-shift technique. In this technique the switching transition of switches in the Q_1-Q_2 leg of the bridge is delayed, i.e., phase shifted, with respect to the switching transition of corresponding switches in the Q_3-Q_4 leg. With no phase-shift between the legs of the bridge, no voltage is applied across the primary of the transformer and, consequently, the output voltage is zero. On the other hand, if the phase shift is 180°, the maximum volt-second product is applied across the primary winding, which produces the maximum output voltage. In the circuit in Fig. 1, ZVS of the lagging-leg switches Q_1 and Q_2 is achieved primarily by the energy stored in output filter inductor L_F. Since the inductance of inductor L_F is relatively large, the energy stored in inductor L_F is sufficient to completely discharge output parasitic capacitance C_1 and C_2 of switches Q_1 and Q_2 and to achieve ZVS even at very light load currents. However, the discharge of parasitic capacitances C_3 and C_4 of leading-leg switches Q_3 and Q_4 is done by the energy stored in leakage inductance L_{LK} of the transformer because during the switching of Q_3 or Q_4 the transformer primary is shorted by the simultaneous conduction of rectifiers D_{R1} and D_{R2} which carry the output filter inductor current. Since leakage inductance L_{LK} is small, the energy stored in L_{LK} is also small so that ZVS of Q_3 and Q_4 cannot be achieved even at relatively high output currents. The ZVS range of the leading-leg switches can be extended to lower load currents by intentionally increasing the leakage inductance of the transformer and/or by adding a large external inductance in series with the primary of the transformer. If properly sized, the external inductance can store enough energy to achieve

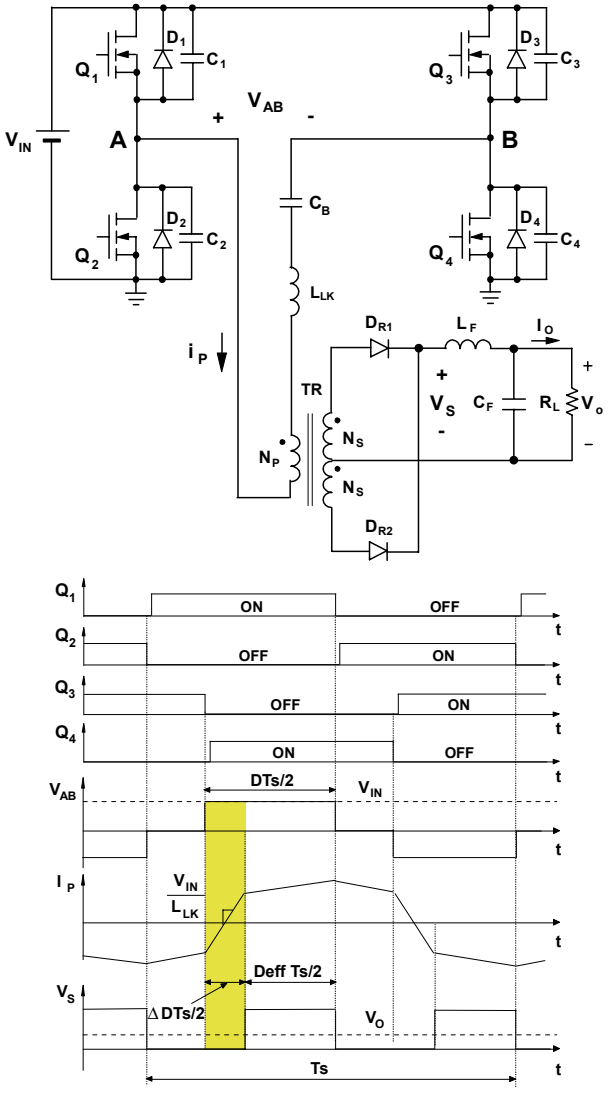

Fig. 1. Conventional full-bridge ZVS converter and its key waveforms.

ZVS of the leading-leg switches even at low currents. However at full load a large external inductance also stores excessive energy that produces large circulating currents, which adversely affects the stress of the semiconductor components as well as the conversion efficiency.

One of the major limitations of the circuit in Fig. 1 is a loss of duty cycle which is indicated by gray color. Generally, a large leakage and/or external inductance extends the time that is needed for the primary current to change direction from negative to positive, and vice verse, as shown in Fig. 1. This extended commutation time results in a loss of duty cycle on the secondary of the transformer, which decreases the conversion efficiency. Namely, to provide full power at the output, the secondary-side duty-cycle loss ΔD must be compensated by reducing the turns ratio of the transformer. With a smaller transformer's turns ratio, the reflected output current into the primary is increased, which increases the primary-side conduction losses. In addition, since a smaller turns ratio of the transformer also increases the voltage stress on the secondary-side rectifiers, the rectifiers with a higher voltage rating that typically have higher conduction losses may be required.

Another major limitation of the conventional FB ZVS converter in Fig. 1 is a severe parasitic ringing at the secondary side of the transformer caused by the resonance of the rectifier's junction capacitance with the leakage inductance of the transformer and/or the external inductance during the turn-off of a rectifier. To control the ringing, a lossy snubber circuit is required on the secondary side which may significantly lower the conversion efficiency of the circuit.

The ZVS range of the leading-leg switches in the FB ZVS-PWM converter in Fig. 1 can be extended to lower load currents without a significant increase of the circulating energy and loss of duty cycle by using a saturable external inductor instead of a linear inductor [5]. If the saturable inductor is designed so that it saturates at higher load currents, the inductor will not store excessive energy at high loads. At the same time, at low load currents, when the inductor is not saturated, it will have sufficiently high inductance to store enough energy to provide ZVS of the leading-leg switches even at very light loads. While it was demonstrated that a properly designed saturable inductor can improve the performance of the FB ZVS-PWM converter, the circuit requires a relatively large-size magnetic core to implement the inductor, which increases the cost of the circuit. Generally, a larger core is required to eliminate the thermal problem that is created by excessive core loss, since the saturable core is placed in the primary circuit and its flux swings between the positive and negative saturation levels.

In this paper, a new isolated, constant-frequency, FB ZVS converter which employs a coupled inductor on the primary side to achieve ZVS in a wide range of load current and input voltage with reduced circulating energy and conduction losses is described. Because in the proposed circuit the energy required to create ZVS conditions does not need to be stored in the leakage inductance, the leakage inductance of the transformer can be minimized. This virtually eliminates the duty cycle loss and also significantly reduces the energy of the secondary-side ringing caused by a resonance between the leakage inductance and junction capacitance of the rectifier. As a result, the proposed circuit exhibits an increased conversion efficiency.

2. New FB ZVS Converter with Coupled Inductor

Figure 2 shows a circuit diagram of the proposed isolated, dc/dc FB ZVS converter that employs a coupled inductor on the primary side to extend the ZVS range of the primary switches with a minimum circulating energy and conduction loss. The primary side of the converter consists of two bridge legs Q_1-Q_2 and Q_3-Q_4 connected through two capacitors C_{B1} and C_{B2} to the series connection of coupled inductor L_C and transformer TR. The two primary side capacitors are used to prevent the saturation of the coupled inductor and transformer cores by blocking the flow of any dc current through L_C and TR. Generally these capacitors are selected large enough so that their voltages are approximately constant during a switching cycle. To regulate the output voltage against load and/or input voltage changes at a constant switching frequency, the circuit requires a phase-shift control. It should be noted that in Fig. 2, the output side of the converter is implemented with a full-wave rectifier with a tapped secondary. However, any other implementation of the secondary side rectification stage is possible.

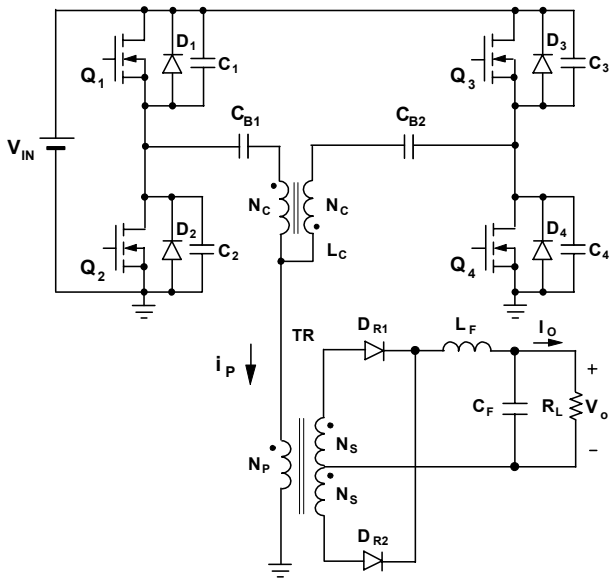

Fig. 2. Proposed full-bridge ZVS converter with coupled inductor.

To facilitate the explanation of operation of the circuit in Fig. 2, Fig. 3 shows its simplified circuit diagram. In the simplified circuit it is assumed that the inductance of output filter L_F is large enough so that during a switching cycle the output filter can be modeled as a constant current source with a magnitude equal to output current I_O. Also, it is assumed that the capacitance of blocking capacitors C_{B1} and C_{B2} is large enough so that the capacitors can be modeled as constant voltage sources. Because the average voltages of the coupled inductor windings and the transformer windings during a switching cycle are zero and the pair of switches in each bridge leg operate with 50% duty cycle, the magnitude of voltage sources V_{CB1} and V_{CB2} in Fig. 3 are equal to $V_{IN}/2$, i.e., $V_{CB1}=V_{CB2}=V_{IN}/2$.

To further simplify the analysis, it is also assumed that the resistance of conducting semiconductor switches is zero, whereas the resistance of the non-conducting switches is infinite. In addition, the leakage inductances of coupled inductor L_C and transformer TR, as well as the magnetizing inductance of transformer TR are neglected because their effect on the operation of the converter is negligible. Magnetizing inductance of coupled inductor L_C and output capacitances $C_1 – C_4$ of primary switches are not neglected in this analysis, since they play a major roll in the operation of the circuit. In Fig. 3, coupled inductor L_C is modeled as an ideal transformer with turns ratio $n_{LC}=1$ and with parallel magnetizing inductance L_M. The number of turns of each of the windings of L_C is N_C.

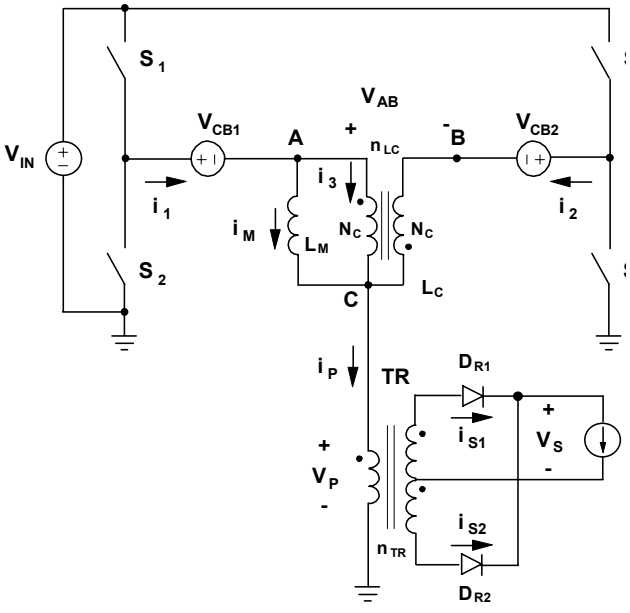

Fig. 3. Simplified circuit diagram of proposed converter showing reference directions of currents and voltages.

Finally, to further facilitate the analysis, Fig. 4 shows the topological stages of the converter during a switching cycle, whereas Fig. 5 shows the key waveforms. As shown in Fig. 5, at time $t=T_O$, switch S_1 in S_1-S_2 leg and switch S_3 in S_3-S_4 leg are closed and currents i_1 and i_2 flow through the corresponding switch, blocking capacitor, and winding of coupled inductor L_C into the primary of transformer TR, as can be seen from the equivalent circuit in Fig. 4(a). At the same time, output current I_O flows through the upper secondary of the transformer so that primary current $i_P=i_1+i_2=I_O/n_{TR}$, where $n_{TR}=N_P/N_S$ is the turns ratio of the transformer, N_P is the number of primary-winding turns, and N_S is the number of secondary-winding turns. From Fig. 4(a) it can be seen that during this topological stage voltage v_{AB} must be zero since voltage sources V_{CB1} and V_{CB2} are connected in opposition through closed switches S_1 and S_3. Furthermore, because of the coupled inductor winding orientation (dot positions in Fig. 4(a)), $v_{AB}=v_{AC}+v_{CB}=0$ can only be maintained if the voltages across the coupled inductor windings are zero, i.e. only if $v_{AC}=v_{CB}=0$. Therefore, since in this topological stage the voltage potential of points A, B, and C in Fig. 4(a) must be the same, primary voltage $v_P=V_{IN}-V_{IN}/2=V_{IN}/2$, as shown in Fig. 5(j). It also should be noted that in this topological stage, magnetizing current of the coupled inductor i_M is constant because $v_{AC}=v_{CB}=0$, i.e., the voltage across the windings of L_C is zero, as illustrated in Fig. 5(i). In addition, because the turns ratio of the windings of L_C is unity ($n_{LC}=1$), current i_3 flowing through winding AC is equal to current i_2 flowing through winding BC, i.e. $i_3=i_2$. Finally, from Fig. 3, it can be seen that $i_1=i_2+i_M=(i_P+i_M)/2$ and $i_2=(i_P-i_M)/2$.

When at $t=T_1$ switch S_1 is turned off, current i_1 is diverted from the transistor of switch S_1 to its output capacitance C_1, as shown in Fig. 4(b). In this topological stage, current i_1 charges capacitor C_1 and discharges capacitor C_2 at the same rate since the sum of the capacitor voltages is equal to constant voltage V_{IN}, as illustrated in Figs. 5(e) and (f). As a result, the potential of point A starts decreasing causing a decrease of voltages v_{AB} and v_P. Namely, voltage v_{AB} decreases from zero toward negative V_{IN}, whereas voltage v_P decreases from $V_{IN}/2$ toward zero, as illustrated in Figs. 5(i) and (j). After capacitor C_2 is fully discharged, i.e., when voltage v_{S2} reaches zero, current i_1 starts flowing through antiparallel diode D_2 of switch S_2, as shown in Fig. 4(c). Due to negative voltage $V_{IN}/2$ applied across winding AB of coupled inductor L_C, its magnetizing current i_M decreases with a rate of $V_{IN}/(2L_M)$. Since during this topological stage primary current i_P does not change, i.e. it stays constant at I_O/n_{TR}, current $i_1=(i_P+i_M)/2$ decreases while current $i_2=(i_P-i_M)/2$ increases at the same rate. To achieve zero-voltage turn-on of switch S_2, it is necessary to turn-on switch S_2 while its antiparallel diode D_2 is conducting. In Fig. 5, switch S_2 is turned on immediately after voltage v_{S2} has fallen to zero.

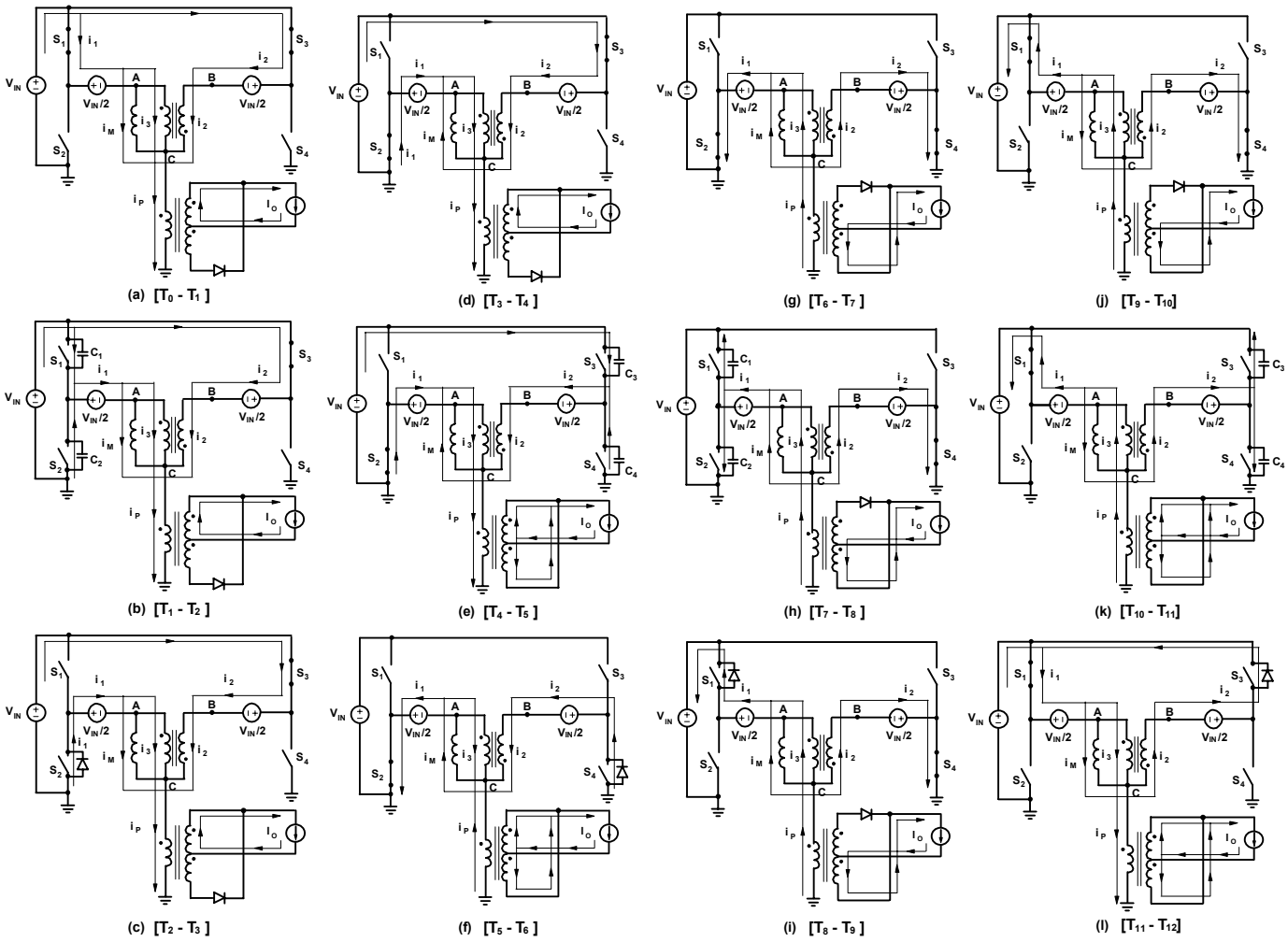

Fig. 4. Topological stages of proposed converter power stage.

Magnetizing current i_M reaches zero at $t=T_3$ and it continues to increase in the negative direction, as shown in Fig. 4(d). As a result, current i_1 continues to decrease, whereas current i_2 continues to increase, as seen from waveforms (m) and (n) in Fig. 5. At $t=T_4$ switch S_3 is turned off so that current i_2 is diverted from the transistor of switch S_3 to its output capacitance C_3, as shown in Fig. 4(e). Because during this transition C_3 is charging, while C_4 is discharging at the same rate, voltage v_{S3} increases from zero toward V_{IN}, whereas voltage v_{S4} decreases from V_{IN} to zero, as illustrated in Figs. 5(g) and (h). Since during this topological stage the potential of point B decreases from $V_{IN}/2$ toward zero, while potential of point A is constant at $V_{IN}/2$, voltage v_{AB} increases from $-V_{IN}/2$ toward zero. At the same time, primary voltage v_P increases in the negative direction from zero to $-V_{IN}/2$ forcing the commutation of the load current from the upper secondary to the lower secondary. If the interconnect inductances and the leakage inductances of transformer TR and coupled inductor L_C were zero, this commutation would be instantaneous. However, due to the inevitable existence of various parasitic inductances on both the primary and secondary side, the commutation of the load current from one secondary to the other when the primary voltage changes sign is not instantaneous, as shown in Fig. 5. In fact, when primary voltage v_P becomes negative, the load current is carried by both secondary windings, as shown in Fig. 4(e), i.e., the transformer windings are effectively shorted. Because during this commutation period, current in the upper secondary i_{S1} decreases, primary current $i_P=(i_{S1}-i_{S2})/n_{TR}$ changes direction at the moment the current in the lower secondary i_{S2} becomes larger than current in the upper secondary i_{S1}. At $t=T_6$ the load current completes the commutation from the upper to the lower secondary, as shown in Fig. 4(g). During the topological stage in Fig. 4(g), currents i_M, i_P, i_1, and i_2 are constant and flow in the negative direction. To achieve ZVS of switch S_4, it is necessary to turn on switch S_4 while current i_2 is positive, i.e. while it still flows through antiparallel diode

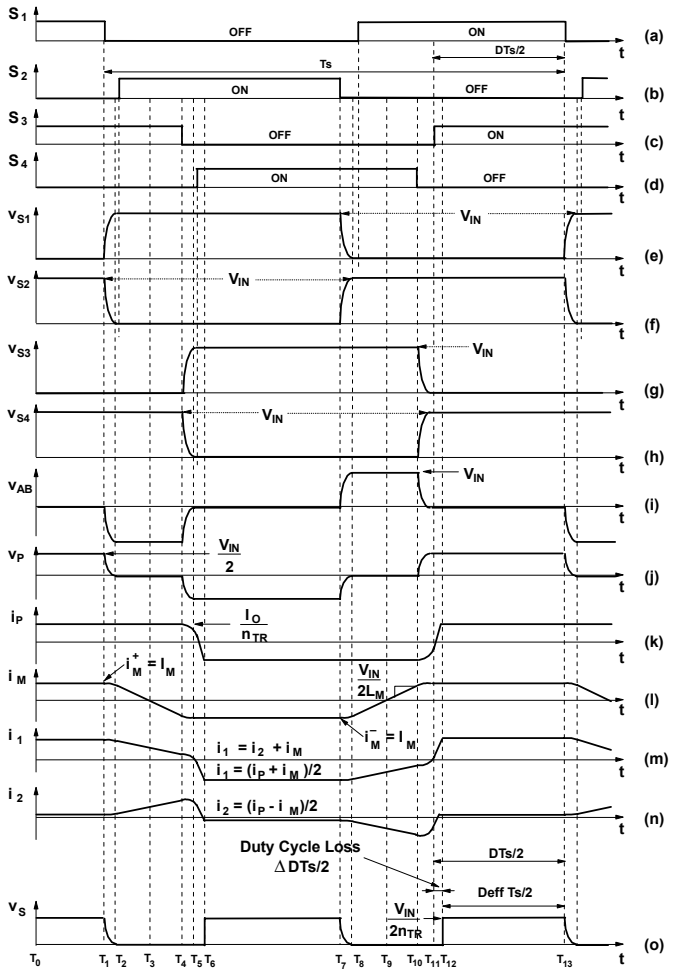

Fig. 5. Key waveforms of proposed converter power stage.

D_4 of switch S_4. In Fig. 5, switch S_4 is turned on immediately after $t=T_5$, i.e., immediately after voltage v_{S4} falls to zero.

The second half of a switching cycle starts at $t=T_7$ when switch S_2 is turned off, which initiates the charging of capacitance C_2 of switch S_2 and discharging of capacitance C_1 of switch S_1, as shown in Fig. 4(h). During this switching transition voltage v_{AB} increases from zero toward V_{IN}, while primary voltage v_P increases from $-V_{IN}/2$ to zero. This topological stage ends at $t=T_8$ when voltage v_{S1} across switch S_1 reaches zero and antiparallel diode D_1 of switch S_1 starts conducting current i_1, as shown in Fig. 4(i). To achieve ZVS of switch S_1, switch S_1 needs to be turned on while diode D_1 is conducting. In Fig. 5, switch S_1 is turned on immediately after voltage v_{S1} has fallen to zero. Because after switch S_2 is turned off voltage v_{AB} starts increasing, magnetizing current i_M starts increasing as well, as can be seen from Fig. 5(l). From instant $t=T_8$, this increase is linear since constant voltage $v_{AC}=v_{AB}/2=V_{IN}/2$ is applied across magnetizing inductance L_M. At $t=T_9$, current i_M becomes positive, as shown in both Fig. 4(j) and Fig. 5(l). Finally, at $t=T_{10}$, switch S_4 is turned off, which initiates switching transition in the S_3-S_4 leg. Because during this transition capacitor C_3 is discharging and capacitor C_4 is charging, potential of point B is increasing from $-V_{IN}/2$ to $V_{IN}/2$. Since during this time potential of point A is constant at $V_{IN}/2$, voltage v_{AB} is decreasing from V_{IN} toward zero, while primary voltage v_P is increasing from zero toward $V_{IN}/2$. As a result, positive primary voltage forces the commutation of the load current from the lower secondary to the upper secondary, as shown in Fig. 4(k). At $t=T_{11}$ capacitance of switch S_3 is fully discharged and current i_2 starts flowing through antiparallel diode D_3 of switch S_3, as shown in Fig. 4(l). To achieve ZVS, switch S_3 is turned on shortly after D_3 starts conducting. During the topological stage in Fig. 4(l), primary current i_P, current i_1, and current i_2 continue to increase from negative values toward positive, as seen from waveforms in Figs. 5(k), (m), and (n). Finally, at $t=T_{12}$, the commutation of the S_3-S_4 leg is completed so that the circuit enters the same topological stage as shown in Fig. 4(a), awaiting the next switching cycle to be initiated by the controller.

It should be noted that in the proposed circuit, the value of the magnetizing inductance of coupled inductor L_C has no effect on commutation time of the primary current from one direction to the other. This commutation time is proportional to the leakage inductance of the transformer. Therefore, to minimize the secondary-side duty-cycle loss and optimize the performance of the circuit, it is necessary to minimize the leakage inductance of the transformer. The minimization of the leakage inductance also minimizes the secondary-side parasitic-ringing energy, which further improves the circuit performance.

3. Design Guidelines

As can be seen from the waveforms in Fig. 5, the commutation of the switches in the S_1-S_2 leg is initiated when current $i_1=i_2+i_M=(i_P+i_M)/2$ is maximum, i.e. when $i_1=(I_O/n_{TR}+I_M)/2$. Also, the commutation of the switches in the S_3-S_4 leg is initiated when current $i_2=(i_P-i_M)/2$ is maximum, i.e., when $i_2=(I_O/n_{TR}+I_M)/2$. Therefore, in the proposed circuit, all primary switches are commutated with the same magnitude current. However, the charging and discharging of the capacitances of switches S_1 and S_2 is done by the sum of the energy stored in the output filter inductor, which is proportional to $(I_O/n_{TR})^2$, and the energy stored in the magnetizing inductance of coupled inductor L_C, which is proportional to $(I_M)^2$. On the other hand, the charging and discharging of the capacitances of switches S_3 and S_4 are done by the sum of the energy stored in the leakage inductance of the transformer and the energy stored in the magnetizing inductance of coupled inductor L_C. Therefore, switches in the S_1-S_2 leg can achieve ZVS in a wide range of input voltage and load current even without assistance from the energy stored in magnetizing inductance L_M of coupled inductor L_C since plenty of energy is available from filter

inductor L_F . However, ZVS of the switches in the S_3-S_4 leg is entirely dependent on the energy stored in the magnetizing inductance of coupled inductor L_C since, for optimal performance, it is desirable to minimize the leakage inductance of the transformer so that the secondary-side duty-cycle loss and the energy of the secondary-side parasitic ringing is also minimized. Generally, to achieve ZVS of all bridge switches in the entire input-voltage and load range, it is necessary to satisfy

$$\frac{1}{2}L_M I_M^2 \geq CV_{IN}^2 + \frac{1}{2}C_{LC}V_{IN}^2 + \frac{1}{2}C_{TR}\left(\frac{V_{IN}}{2}\right)^2, \quad (1)$$

where $C=C_3=C_4$ is the capacitance across primary switches S_3 and S_4, C_{LC} is the interwinding capacitance of coupled inductor L_C, and C_{TR} is the capacitance seen across the primary of transformer TR that includes interwinding capaitance of the transformer and any reflected capacitance of the secondary-side circuit. If capacitances C_{LC} and C_{TR} are neglected, Eq. (1) simplifies to

$$L_M I_M^2 \geq 2CV_{IN}^2 . \quad (2)$$

As can be seen from Eq. (2), if the value of inductor L_M is selected so that ZVS is achieved at no load and maximum input voltage $V_{IN(max)}$, ZVS is achieved in the entire load and input-voltage range.

The value of inductor L_M required to achieve ZVS at no load can be calculated by observing the waveform during time interval T_8-T_{10} in Fig. 5. Magnetizing current i_M changes linearly from maximum negative value $I^-_M=I_M$ to maximum positive value $I^+_M=I_M$, i.e., i_M changes for $2I_M$, due to a positive voltage of $V_{IN}/2$ induced across the winding AC of inductor L_C. Since according to Fig. 5, the time interval T_8-T_{10} is approximately equal to $(1\text{-}D)T_S/2$, where D is duty cycle and T_S is a switching period, I_M can be calculated from

$$\frac{V_{IN}}{2} = L_M \frac{2I_M}{(1-D)\frac{T_S}{2}}, \quad (3)$$

as

$$I_M = \frac{(1-D)V_{IN}}{8L_M f_S}, \quad (4)$$

where $f_S=1/T_S$ is the switching frequency. Since at no load $D\approx 0$ because the two bridge legs must be out of phase to reduce volt-sec product across the primary winding, the ZVS condition at no load and high line from Eqs. (2) and (4) is

$$L_M\left(\frac{V_{IN(max)}}{8L_M f_S}\right)^2 \geq 2CV_{IN(max)}^2 . \quad (5)$$

Finally, from Eq.(5), the value of L_M required to maintain ZVS at no load and high line is

$$L_M \leq \frac{1}{128Cf_S^2} . \quad (6)$$

As can be seen from Fig. 3, current i_M flowing through magnetizing inductance L_M introduces a current asymmetry in the two bridge legs. Namely, because of the coupling of windings AC and BC, current i_2 flowing through winding BC is equal to current i_3 flowing through winding AB so that $i_1=i_2+I_M$. Therefore, in the proposed circuit, leg S_1-S_2 always carries a higher current than the leg S_3-S_4, the difference being magnetizing current i_M. To simultaneously achieve ZVS at no load and minimize the bridge conduction loss in the proposed circuit in Fig. 2, it is necessary to select the maximum magnetizing inductance L_M determined from Eq. (6). Furthermore, if for such a selected magnetizing inductance, current i_2 in the S_3-S_4 leg is significantly lower than current i_1 in the S_1-S_2 leg, different size switches can be selected for the two legs, which may reduce the cost of the implementation without sacrificing the circuit performance.

Finally, it should be noted that to achieve maximum efficiency improvement, the turns ratio of the transformer must be maximized. In fact, since the duty-cycle loss in the converter in Fig. 2 is negligible due to the minimized leakage inductance of the transformer, the converter can be designed with a larger turns ratio compared to a converter that uses the leakage inductance and/or external inductance to extend the ZVS range. Moreover, the minimized leakage inductance greatly reduces the secondary–side ringing between the leakage inductance of the transformer and the junction capacitance of the rectifier so that any residual parasitic ringing can be damped by a small snubber circuit as, for example, the RCD-snubber circuit shown in Fig. 6.

The control of the circuit in Fig. 2 is the same as the control of any other constant frequency FB ZVS converter. In fact, any of the integrated phase-shift controllers available on the market can be used implement the control of the proposed circuit. However, it should be noted that in the circuit in Fig. 2 the maximum output voltage is obtained when the bridge legs are operated in phase, which is the opposite from the behavior of the conventional FB ZVS converter shown in Fig. 1 that achieves the maximum output voltage when the bridge legs are switched out of phase. This difference in the control characteristic of the converter has a minor effect on the control-loop design since a simple control-signal inversion in the voltage control loop circumvents the problem.

It also should be noted that the proposed circuit in Fig. 2 can be implemented with any type of secondary-side rectifier. Specifically, it can be also implemented with full-wave, full-bridge rectifier, or current-doubler rectifier.

4. Experimental Results

The performance of the proposed circuit was verified on a 670-W experimental prototype operating at 112 kHz. The experimental converter was designed to operate from 400-V dc input and deliver 14 A from a 48-V output. The component values of the experimental circuit are shown in Fig. 6. The phase-shift control circuit was implemented using the UC3875 controller. For performance comparison purposes, an experimental prototype of the conventional FB

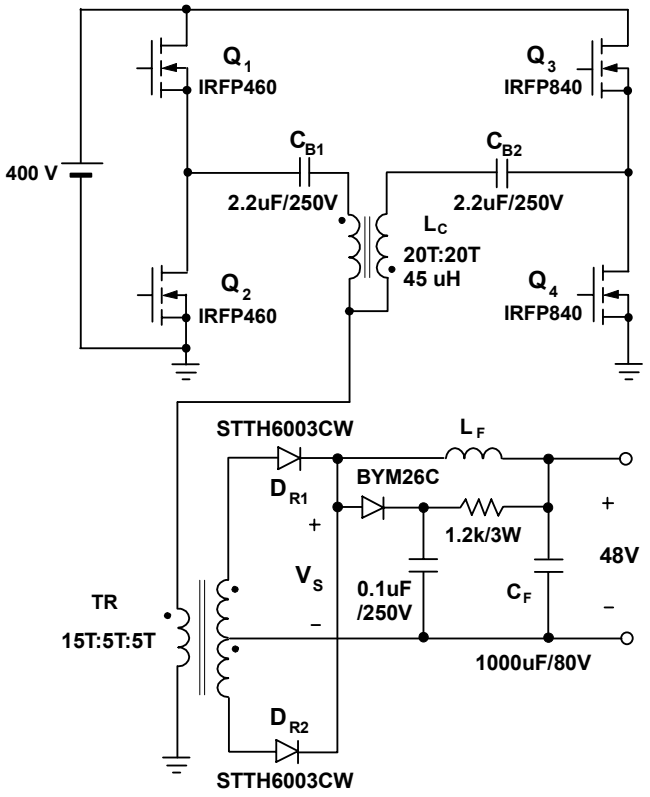

Fig. 6. Experimental 670 W, proposed converter power stage with coupled inductor.

ZVS converter shown in Fig. 1 was also built. The conventional FB ZVS converter was designed with an external inductance of 18 μH in series with the primary winding of the transformer (28T:5T:5T) to achieve ZVS over the load range from 50% to 100%.

Figures 7(a) and 7(b) show the oscillograms of key waveforms of the conventional FB ZVS converter and the proposed FB ZVS converter, respectively. As can be seen from Fig. 7(a), in the conventional FB ZVS converter the parasitic ringing caused by the external leakage inductance with the rectifier's junction capacitance is severe even with a snubber circuit which dissipates approximately 20 W. Moreover, the duty cycle loss is approximately 0.5 μsec which is more than 18% of the secondary side duty cycle. As can be seen from the corresponding waveforms in Fig. 7(b), the proposed converter has a very small duty cycle loss (< 0.1 μsec), as well as a very much reduced parasitic ringing because of a minimized leakage inductance of the transformer that is less than 2 μH.

Figure 8 shows the measured efficiencies of the conventional FB ZVS converter and the proposed FB ZVS converter as functions of the output power. As can be seen from Fig. 8, the proposed converter shows a conversion efficiency improvement in the entire measured power range

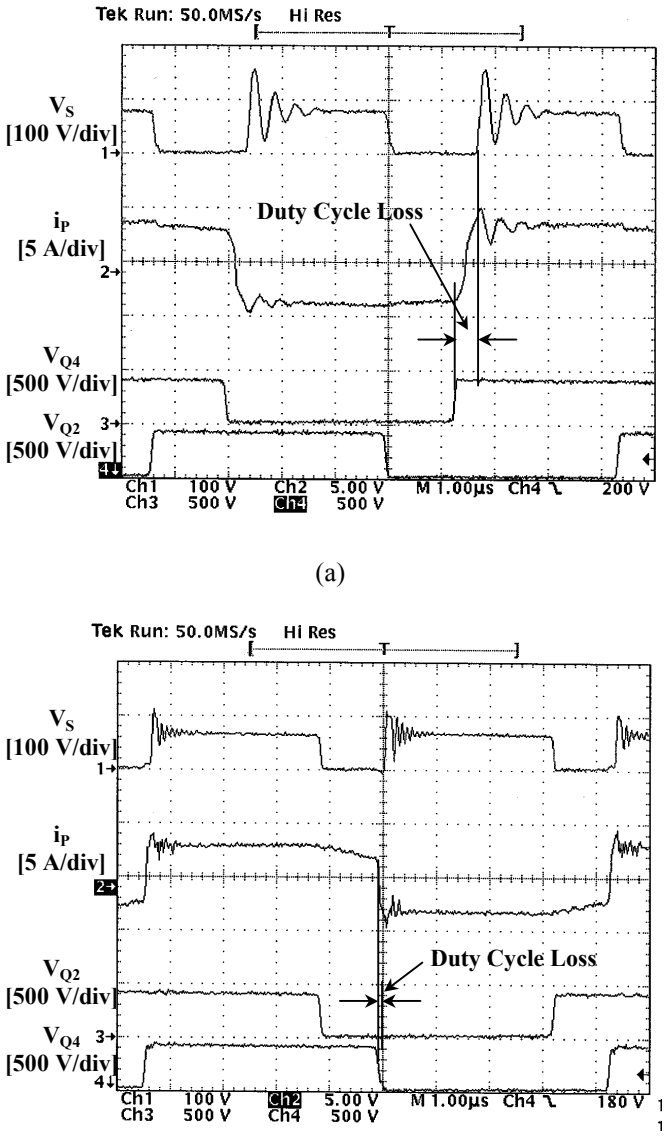

Fig. 7. Measured key waveforms at P_O = 670 W: (a) conventional FB ZVS converter; (b) proposed FB ZVS converter. From top to bottom: secondary voltage V_S [100V/div]; primary current i_P [5 A/div]; drain-to-source voltage V_{Q2} of Q_2 [500 V/div]; drain-to-source voltage V_{Q4} of Q_4 [500 V/div]. Time base: 1 μs/div.

from 50 W to 670 W. Generally, the efficiency improvement is more pronounced at light loads where the conventional FB ZVS converter operates with hard switching. Specifically, at light loads, the efficiency improvement is more than 20%. At full load, the proposed circuit shows a efficiency improvement of approximately 3%, which translates into approximately 30% reduction of the losses.

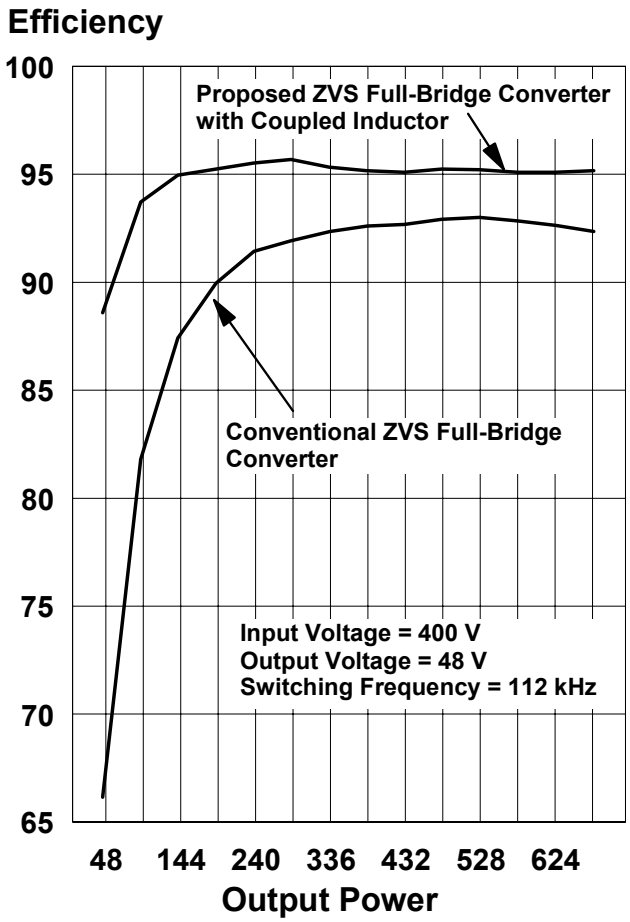

Fig. 8. Measured efficiencies of conventional FB ZVS converter and proposed FB ZVS converter as functions of output power.

5. Conclusion

In this paper, a new isolated, constant-frequency, FB ZVS converter which employs a coupled inductor on the primary side to achieve ZVS in a wide range of load current and input voltage with reduced circulating energy and conduction losses has been described. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifiers. The operation and performance of the proposed circuit was verified on a 670-W (48-V/14-A) prototype. The measured efficiency improvement of the proposed circuit with respect to the conventional FB ZVS converter was 3% at full load and more than 20% at light loads. The ability of the proposed circuit to maintain a high efficiency at light loads makes the proposed converter particularly attractive in applications where a number of power converters connected in parallel share the load current so that each converter operates with a load which is a fraction of its full load.

Notice

References

[1] O.D. Petterson, D.M. Divan, "Pseudo-Resonant Full Bridge DC/DC Converter," *IEEE Power Electronics Specialists' Conf. Rec.*, pp. 424 – 430, 1987.

[2] R.A. Fisher, K.D.T. Ngo, and M.H. Kuo, "A 500 kHz, 250 W DC-DC Converter with Multiple Outputs Controlled by Phase-Shifted PWM and Magnetic Amplifiers," *High Frequency Power Conversion Proceedings,* pp. 100 - 110, May 1988.

[3] L.H. Mweene, C.A. Wright, and M.F. Schlecht, "A 1 kW, 500 kHz Front-end Converter for a Distributed Power Supply System," *IEEE Applied Power Electronics Conf. (APEC) Proc.,* pp. 423 - 432, 1989.

[4] J. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-switched PWM Converter," *IEEE Applied Power Electronics Conf. (APEC) Proc.,* pp. 275 - 284, 1990.

[5] G. Hua, F.C. Lee, M.M. Jovanović, "An Improved Full-Bridge Zero-Voltage-Switched PWM Converter Using a Saturable Inductor," *IEEE Power Electronics Specialists' Conf. Rec.,* pp. 189 – 194, 1991.