ANALYSIS AND DESIGN OF MULTIPLE-OUTPUT CONVERTERS WITH STACKED SECONDARIES

ANALYSE ET CONCEPTION DE CONVERTISSEURS MULTISORTIES AVEC EMPILAGE DES SECONDAIRES

Qing Chen and Fred C. Lee
Virginia Power Electronics Center
The Bradley Department of Electrical Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

Milan M. Jovanović
DELTA Power Electronics Lab., Inc.
1872 Pratt Drive
Blacksburg, VA 24060

Résumé
Empiler les secondaires ou les sorties est un moyen efficace d'améliorer la régulation mutuelle des convertisseurs multisorties. Cet article présente quelques modes d'empilement des sorties et une analyse pour chaque mode. L'analyse montre que l'empilement des sorties introduit un mécanisme interne de compensation de tension qui fournit une régulation de la tension des sorties quand le courant change. Les effets d'empilement des sorties sur les pertes de puissance et les contraintes en courant sur les diodes sont analysés aussi. L'analyse est vérifiée avec un convertisseur forward à deux sorties.

Abstract
Stacking secondaries or outputs is an effective way to improve dc cross-regulation for multiple-output converters. In this paper, various stacking schemes are presented, and dc analysis is performed for each particular scheme. The analysis reveals that stacking introduces an internal voltage compensation mechanism which provides output voltage tracking as any load current changes. The effects of stacking on power loss and current stress of the rectifiers are also analyzed. The analyses are verified on an experimental two-output forward converter.

I. INTRODUCTION

Without post regulation, a multiple-output converter always exhibits dc cross-regulation errors at the outputs [1-5]. The imperfect dc regulation results from two sources: improper centering and internal voltage drops due to the secondary parasitic inductances and resistances. The centering problem can be solved by using an autotransformer [6] or a fractional number of turns [7]. Using weighted voltage control (WVC) [6,8-11], the dc regulation error can be redistributed among the outputs by adjusting the values of the weighting factors. Nevertheless, WVC does not reduce the total error since it does not provide a mechanism for outputs to track each other. Stacking secondaries can effectively reduce the voltage variation range and help to correctly center the secondary voltages [9-11].

The purpose of this paper is to analyze various stacking schemes and quantify their dc cross-regulation improvements. In addition, the effects of the stacking schemes on power loss and current stress of rectifiers are evaluated. Section II presents a dual-output converter with a single feedback control and WVC, respectively. In Section III, the analytical expressions of the output voltages for the stacking schemes are derived incorporating major parasitics, such as leakage inductances, forward voltage drops of the rectifier diodes, and the winding resistances of the transformer and the output filter inductors. Section IV compares the merits and demerits for each stacking scheme in terms of quality of dc cross-regulation, current stress, and internal power losses, helping to achieve optimum design. Key results are summarized in Section V.

The analyses and discussions are focused on the converter with dual-output. Nevertheless, the stacking schemes presented in this paper are by no means just limited to two outputs.

This work was supported in part by Delta Electronic Ind. Co., Ltd., Taiwan, and the Virginia Center for Innovative Technology.

II. SINGLE FEEDBACK CONTROL AND WEIGHTED VOLTAGE CONTROL

In this section, a dual-output converter, as shown in Fig. 1, is used as an example to illustrate the effectiveness of stacking secondaries in improving dc cross-regulation. The specifications of the converter are

- input voltage range: $170\ V \le V_{in} \le 270\ V$;
- 5 V output: $4.8\ V \le V_{o1} \le 5.2\ V$, $2\ A \le I_{o1} \le 15\ A$;
- 12 V output: $11.5\ V \le V_{o2} \le 12.7\ V$, $0.5\ A \le I_{o2} \le 3\ A$.

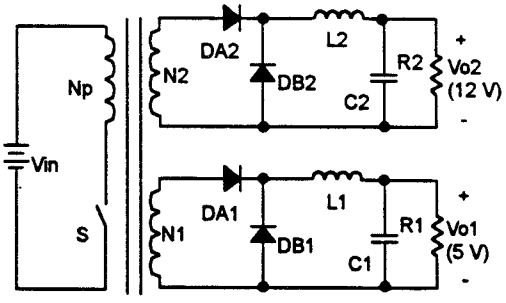

Fig. 1. Dual-output forward converter.

Following the well-established design procedure for the power stage of a forward converter [12], the experimental forward converter operating at 100 kHz was built with the following components:

- active switch S, IRFP450;
- 5 V output rectifier diodes (D_{A1} and D_{B1}), IR60CNQ035;
- 12 V output rectifier diodes (D_{A2} and D_{B2}), IR8T100 ;
- power transformer:

- core TDK PQ32/30Z,
- primary winding, 45 turns 3xAWG29 wire,
- 5 V secondary, 3 turns 0.005x0.65" copper foil, and
- 12 V secondary, 7 turns 4xAWG29 wire.

First, single feedback control is applied. The 5 V output is sensed and fed back to modulate the duty cycle. The 12 V output is cross-regulated. The calculated and measured outputs are plotted in Fig. 2. The sensed output (5 V) is tightly controlled, whereas the unsensed output (12 V) varies over a large range. The design specifications are not met.

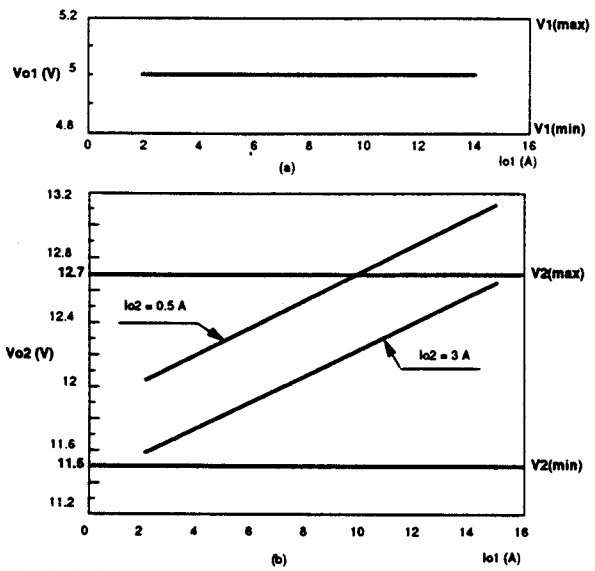

Fig. 2. DC regulation characteristics of single feedback control at 170 V: (a) 5 V output which is sensed and tightly regulated; (b) 12 V output which is cross-regulated.

The dc regulation for 12 V output can be improved by invoking WVC [6]. The calculated and measured output voltages are shown in Fig. 3. Unlike single feedback control where the 5 V output is virtually kept constant, here both 5 V and 12 V outputs vary over certain ranges, but both are within the design specifications.

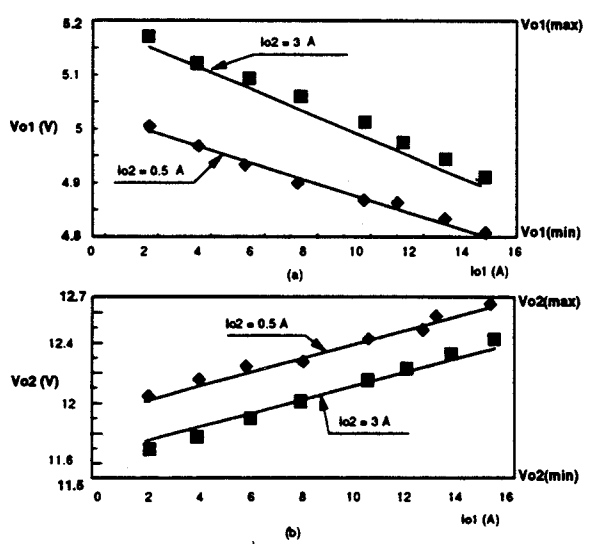

Fig. 3. Regulation characteristics of weighted voltage control: (a) 5 V output; (b) 12 V output. The square dots are the measurements.

If the design specifications are further tightened, *e.g.*,

- 5 V output: $4.9\ V \le V_{o1} \le 5.1\ V, 2\ A \le I_{o1} \le 15\ A$, and
- 12 V output: $11.7\ V \le V_{o2} \le 12.5\ V, 0.5\ A \le I_{o2} \le 3\ A$.

the output regulations cannot meet the design specifications even if WVC is used.

In essence, WVC only redistributes the error between the outputs rather than reduces voltage variation range. Any improvement of dc regulation for one output is at the cost of the other output. The deviation of each output from its desired value depends on how much it is weighted in the feedback signal. Since there is little coupling between the outputs, there is virtually no tracking between the outputs as either of the load currents varies. The output voltages vary over a wide range.

If the one secondary is stacked on another, as shown in Fig. 4, the output voltages fall into the design specifications, as shown in Fig. 5. Obviously, stacking secondaries narrows the output variation range for both outputs.

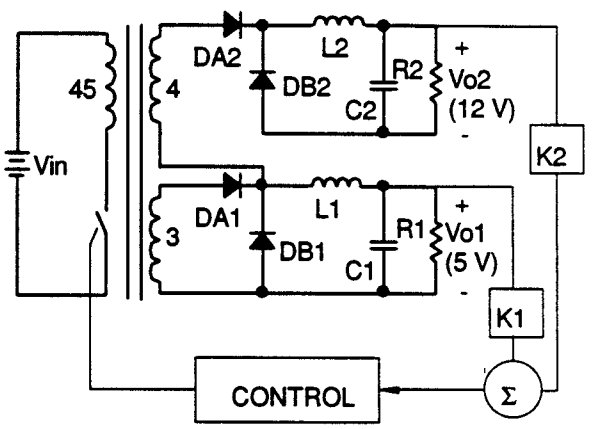

Fig. 4. Dual-output converter with stacked secondaries and WVC.

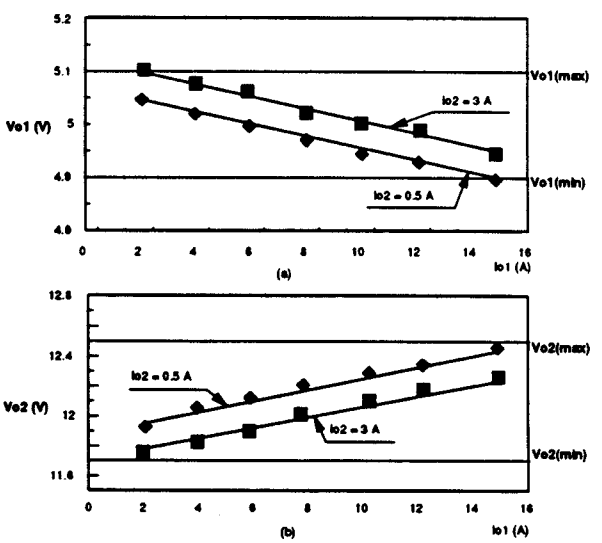

Fig. 5. Output voltages with stacked secondaries and WVC for V_{in}=170 V: (a) 5 V output, and (b) 12 V output. The square dots are the measurements.

It is shown, through the illustration, that the conventional single feedback control scheme and weighted voltage control

are suitable for the applications where the dc regulation specifications are relatively loose. Only stacking secondaries can accommodate the tighter regulation specifications. In next section, the multiple-output converter with stacked secondaries is analyzed, and the mechanism of improving cross-regulation is explained.

III. ANALYSIS OF STACKED POWER STAGE

Figure 6 shows the equivalent circuit of the multiple-output converter with stacked secondaries. The power stage dc model is obtained by substituting each component with its corresponding circuit model [6]. The major parasitics included in the circuit model are

R_{ds}- on-resistance of the MOSFET,
C_{ds}- junction capacitance of the MOSFET,
R_p - primary winding resistance of the transformer,
R_{si} - secondary winding resistance of the transformer,
V_{di} - offset voltage of the rectifier diodes,
R_{di} - on-resistance of the rectifier diodes, and
R_{Li} - resistance of the output filter inductors.

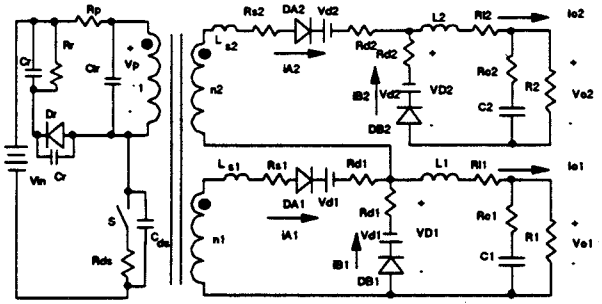

Fig. 6. Equivalent circuit of the multiple-output converter with stacked secondaries.

In the analysis, the magnetizing current is assumed to be small compared with the sum of the reflected load currents; therefore, its effect is neglected.

When the active switch is on, the voltage across the primary winding of the transformer is

$$V_p = V_{in} - I_p R_{ds} - \Delta V_{pcu}, \tag{1}$$

where

V_{in} - line voltage,
R_{ds} - on-resistance of the switch,
I_p - magnitude of the current in the primary, $I_p = N_1 I_{o1} + N_2 I_{o2}$,
ΔV_{pcu}- voltage drop across the primary winding resistance. If the radius of the winding is less than the skin depth, $\Delta V_{pcu} \approx I_p R_{pdc}$.

After the active switch is turned off, it takes finite time Δt_p for the voltage across the primary to change the polarity due to the parasitic capacitances (including the junction capacitance of the MOSFET, the transformer capacitance, and the stray capacitance). The process of charging these capacitances causes a duty cycle extension, as shown in Fig. 7, which can be calculated based on the equivalent volt-second product:

$$\Delta D_p = \frac{C_t V_{in} + 10 C_o \sqrt{V_{in}}}{2 I_p} f_s, \tag{2}$$

where

C_t - total capacitance of the transformer and the reset circuitry,
C_o- junction capacitance of the MOSFET at V_{ds}=25 V, and
f_s - switching frequency.

With this simplification, the voltage across the transformer windings (both primary and secondary sides) have an effective duty cycle:

$$D_e = D + \Delta D_p, \tag{3}$$

where D is the duty cycle provided by the controller.

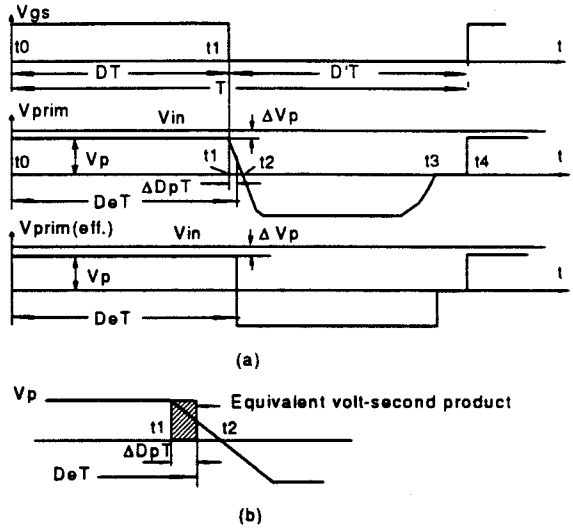

Fig. 7. Primary waveforms over a complete switching period: The circuit parasitic capacitances cause duty cycle extension which can be quantified by equivalent volt-second product. (a) the primary waveforms; (b) magnification of V_{prim} during t_1- t_2.

Every secondary of the transformer can be modeled by a voltage source with magnitude equal to the reflected primary voltage and effective duty cycle, D_e. To simplify the analysis, the current through each inductor is assumed constant. The waveforms over a complete switching period are shown in Fig. 8.

The procedure to derive the output voltages is to find the voltages across the freewheeling diodes (D_{B1} and D_{B2}), V_{D1} and V_{D2}. The output voltages are then obtained by averaging V_{D1} and V_{D2} over a switching period.

As the active switch is turned on, the voltages across the freewheeling diodes, V_{D1} and V_{D2}, cannot change instantaneously due to the leakage inductances L_{s1} and L_{s2}. The effective duty cycle losses are

$$\Delta D_1 = \frac{I_{o1} + I_{o2}}{V_{s1}} L_{s1} f_s, \tag{4}$$

and

$$\Delta D_2 = \frac{I_{o2}}{V_{s2}} L_{s2} f_s. \tag{5}$$

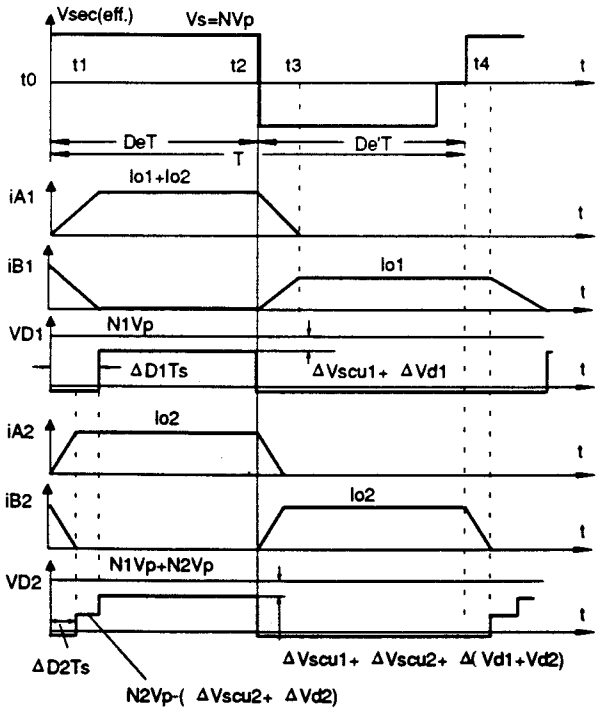

Fig. 8. Secondary waveforms over a complete switching period.

After the leakage inductances are charged to their corresponding load currents, V_{D1} and V_{D2} become

$$V_{D1} = V_{s1} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - V_{d1}, \tag{6}$$

and

$$V_{D2} = V_{s1} + V_{s2} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - V_{d1} - V_{d2} - I_{o2}(R_{s2} + R_{d2}), \tag{7}$$

Averaging voltages V_{D1} and V_{D2} yields the output voltages:

$$V_{o1} = [V_{s1} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - V_{d1}](D_e - \Delta D_1) - (V_{d1} + I_{o1}R_{d1})(1 - D_e + \Delta D_1) - R_{L1}I_{o1}, \tag{8}$$

and

$$V_{o2} = [V_{s2} - V_{d1} - V_{d2} - I_{o1}R_{d1} - I_{o2}(R_{s2} + R_{d2})](\Delta D_1 - \Delta D_2) + [V_{s1} + V_{s2} - V_{d1} - V_{d2} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - I_{o2}(R_{s2} + R_{d2})](D_e - \Delta D_1) - (V_{d2} + I_{o2}R_{d2})(1 - D_e + \Delta D_2) - I_{o2}R_{L2}. \tag{9}$$

By neglecting the 2nd order terms, the output voltages become

$$V_{o1} \approx [V_{s1} - (I_{o1}R_{s1} + I_{o2}(R_{s1} + R_{d1})]D_e - [V_{d1} + I_{o1}(L_{s1}f_s + R_{d1} + R_{L1}) + I_{o2}L_{s1}f_s], \tag{10}$$

or

$$V_{o1} \approx V_{s1}D_e - V_{d1} - I_{o1}Z_{11} - I_{o2}Z_{12}, \tag{11}$$

and

$$V_{o2} \approx [V_{s1} + V_{s2} - V_{d1} - I_{o1}(R_{s1} + R_{d1}) - I_{o2}(R_{s1} + R_{d1} + R_{s2})]D_e - [V_{d2} + I_{o1}L_{s1}f_s + I_{o2}[(L_{s1} + L_{s2})f_s + R_{d2} + R_{L2}]], \tag{12}$$

or

$$V_{o2} \approx (V_{s1} + V_{s2})D_e - (V_{d1}D_e + V_{d2}) - I_{o1}Z_{21} - I_{o2}Z_{22}, \tag{13}$$

where the internal impedances are defined as:

$$Z_{11} = L_{s1}f_s + R_{s1}D_e + R_{d1} + R_{L1}, \tag{14}$$

$$Z_{12} = (R_{s1} + R_{d1})D_e + L_{s1}f_s, \tag{15}$$

$$Z_{21} = L_{s1}f_s + (R_{s1} + R_{d1})D_e, \text{ and} \tag{16}$$

$$Z_{22} = (L_{s1} + L_{s2})f_s + (R_{s1} + R_{d1} + R_{s2})D_e + R_{d2} + R_{L2}. \tag{17}$$

Each output voltage is dependent not only on its load current but also on the load current of the other output. This is different from the non-stacked case where the output voltages are

$$V_{o1} = V_{s1}D_e - V_{d1} - I_{o1}(L_{s1}f_s + R_{s1}D_e + R_{d1} + R_{L1}), \tag{18}$$

and

$$V_{o2} = V_{s2}D_e - V_{d2} - I_{o2}(L_{s2}f_s + R_{s2}D_e + R_2 + R_{L2}). \tag{19}$$

For the non-stacked case, as shown in Fig. 9(a), there is no coupling between the outputs. If one load current increases and its output voltage drops, the feedback control will render the duty cycle to increase. As a result, the voltage of another output will also increase even though its load current is kept constant. On the other hand, stacking the secondaries, as shown in Fig. 9(b), introduces coupling between the outputs. Whenever a load current variation occurs at any output, it results in a voltage change at that output, and another output voltage changes in the same direction. Now a duty cycle change produced by the feedback control loop adjusts all the output voltages in the same direction, thereby producing smaller overall excursion of both outputs in steady state.

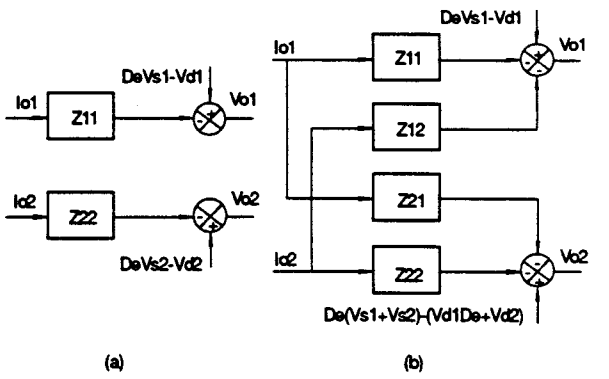

Fig. 9. Illustration of internal voltage compensation mechanism: (a) Non-stacked secondaries; (b) Stacked secondaries.

The internal voltage compensation mechanism makes the outputs track each other. The ability of tracking between the output voltages depends on transimpedances Z_{12} and Z_{21}. The larger the transimpedances, the better the tracking between the output voltages.

Stacking secondaries not only introduces an internal voltage compensation, resulting better voltage tracking, but it also has the function of voltage centering. For most applications, transformer windings take integer turns. Therefore, the secondary voltages are seldom correctly centered to the desired values. By applying stacking scheme, a constant voltage drop (

the constant part of the rectifier diodes, V_d) is introduced, and the stacked output voltage can be down shifted. It can be seen that all the stacking schemes presented later on introduce certain amount of constant voltage drop for the stacked output except for direct stacking of the secondary windings.

Besides improving cross-regulation, stacking of secondaries makes it possible for the transformer to use fewer turns for the higher voltage output. When stacking the 12 V secondary on the 5 V secondary, for instance, the 12 V secondary can use 4 turns instead of 7 turns before stacking. Fewer turns directly translate to less leakage inductance, and therefore the adverse effects of leakage inductance are reduced. Furthermore, fewer turns make it possible to use copper foil, avoiding expensive litz wire for high frequency-application.

Improvement of dc regulation for stacked secondaries is not without penalty. As can be seen from Fig. 4, the load current for 12 V output goes through the 5 V secondary winding and the forward rectifier diode, D_{A1}, in addition to the 12 V secondary winding and the forward rectifier diode, D_{A2}, during on-time. The power losses are obviously increased. So is the current stress on D_{A1}. These can be analytically calculated.

The primary power losses can be approximated as:

$$P_p = (n_1 I_{o1} + n_2 I_{o2})^2 (R_{ds} + R_p) D_e, \tag{20}$$

where the turns ratios are

$$n_1 = \frac{N_1}{N_p}, \quad n_2 = \frac{N_2}{N_p}.$$

The secondary losses before stacking are

$$P_1 = I_{o1} V_{d1} + I_{o1}^2 (R_{L1} + R_{d1} + R_{s1}) D_e, \tag{21}$$

and

$$P_2 = I_{o2} V_{d2} + I_{o2}^2 (R_{L2} + R_{d2} + R_{s2}) D_e. \tag{22}$$

After stacking the secondary of V_{o2} on the secondary of V_{o1}, the secondary losses become

$$\begin{aligned} P_1 &= I_{o1} V_{d1} + I_{o1}^2 (R_{L1} + R_{d1} + R_{s1}) D_e \quad \leftarrow \text{same as NS} \\ &+ I_{o2} V_{d1} + (2 I_{o1} I_{o2} + I_{o1}^2)(R_{d1} + R_{s1}) D_e \leftarrow \text{increased part} \end{aligned} \tag{23}$$

and

$$P_2 = I_{o2} V_{d2} + I_{o2}^2 (R_{L2} + R_{d2} + R_{s2}) D_e. \tag{24}$$

Compared with Eq. (22), it can be seen that the expression for P_2 is the same as that before stacking, but the winding resistance, R_{s2}, is smaller. Therefore, the power loss for V_{o2} is decreased. The power losses in V_{o1} output, however, are increased by:

$$\Delta P_1 = I_{o2} V_{d1} + (2 I_{o1} I_{o2} + I_{o1}^2)(R_{d1} + R_{s1}) D_e. \tag{25}$$

If I_{o2} is small compared with I_{o1} (usually the case) the increased power losses are insignificant.

The current stress of D_{A1} is increased from I_{o1} to $I_{o1}+I_{o2}$. Again, if the load current of V_{o2} is small, the current stress is increased by only a small amount.

IV. VARIATIONS OF STACKING METHODS

In the above discussion, the 12 V secondary winding is stacked at the input of the output filter of the 5 V output. However, stacking can be realized in different ways. The various stacking schemes are summarized, analyzed, and compared in the following.

(a) Stacking at the input of the output filter, Fig. 4.

This scheme has been fully analyzed in the last section, and it is listed here again to facilitate comparison. Internal voltage compensation occurs during turn-on of the active switch. The transimpedances and the increased losses are moderate among all the stacking schemes.

(b) Stacking at the output of V_{o1}, Fig. 10.

This scheme provides the best output voltage tracking since the transimpedances are the largest. The power losses, nevertheless, are also the largest. The current stresses for both D_{A1} and D_{B1} are increased from I_{o1} to $I_{o1}+I_{o2}$.

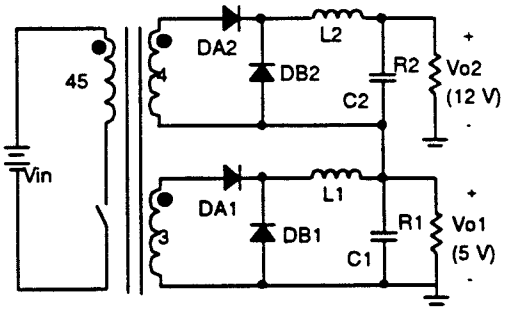

Fig. 10. Stacking the secondaries at the output.

(c) Stacking the secondary freewheeling diodes, Fig. 11.

Internal voltage compensation occurs during turn-off of the active switch. The transformer is same as that of non-stacked case, *i.e.*, the 12 V secondary winding is 7 turns. The losses are smaller compared with (a) and (b). The current stress of D_{B1} is increased to $I_{o1}+I_{o2}$.

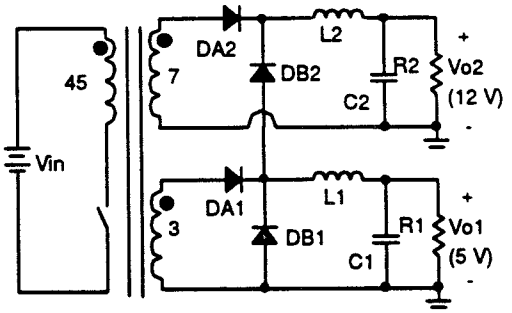

Fig. 11. Stacking the secondary freewheeling diodes.

(d) Stacking the secondary windings only, Fig. 12.

The coupling between two outputs are established only through the transformer. The transimpedances and the losses are the smallest among all the schemes. The current stress for each rectifier diode is unchanged compared with the non-stacked case.

Table 1. Analytical Expressions of the Internal Impedances and the Off-Set Voltage for V_{o2}.

Type	Z_{11}	Z_{12}	Z_{21}	Z_{22}	V_{off}
(a)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{d1})D_e + L_{s1}f_s$	$(R_{s1} + R_{d1})D_e + L_{s1}f_s$	$(R_{s1} + R_{d1} + R_{s2})D_e + R_{d2} + R_{L2} + (L_{s1} + L_{s2})f_s$	$V_{d1}D_e + V_{d2}$
(b)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{s1}D_e + R_{d1} + L_{s1}f_s + R_{L1}$	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{s2})D_e + (L_{s1} + L_{s2})f_s + R_{d1} + R_{d2} + R_{L1} + R_{L2}$	$V_{d1} + V_{d2}$
(c)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{d1}(1 - D_e)$	$R_{d1}(1 - D_e)$	$R_{d1}(1 - D_e) + R_{d2} + L_{s2}f_s + R_{L2}$	$(1 - D_e)V_{d1} + V_{d2}$
(d)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{s1}D_e + L_{s1}f_s$	$R_{s1}D_e + L_{s1}f_s$	$(R_{s1} + R_{s2})D_e + R_{d2} + R_{L2} + (L_{s1} + L_{s2})f_s$	V_{d2}
(e)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{L1})D_e + R_{d1}(1 - D_e) + L_{s1}f_s$	$R_{s1}D_e + (1 - D_e)R_{d1} + L_{s1}f_s$	$(R_{s1} + R_{s2})D_e + (1 - D_e)R_{d1} + R_{d2} + R_{L2}(L_{s1} + L_{s2})f_s$	$V_{d1}(1 - D_e) + V_{d2}$

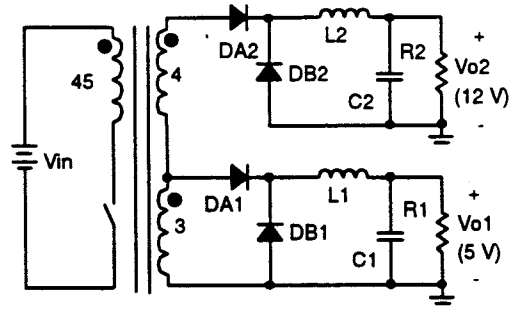

Fig. 12. Stacking the secondary windings only.

(e) Stacking the secondary windings and the freewheeling diodes, Fig. 13.

This is the combination of schemes (c) and (d). The transimpedances and power losses are similar to those of (a). The current stress of D_{B1} is $I_{o1}+I_{o2}$.

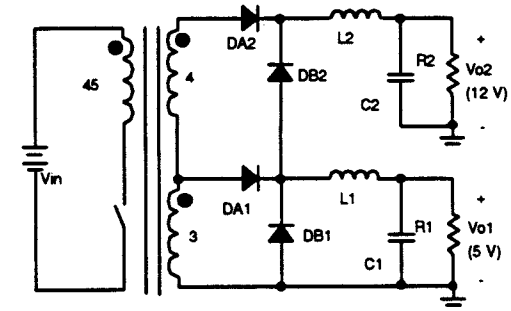

Fig. 13. Stacking the secondary windings and the freewheeling diodes.

The analytical expressions of output voltages for all discussed stacking schemes can take the form as given in Eqs. (10) and (12):

$$V_{o1} = V_{A1}D_e - V_{B1}, \tag{26}$$

$$V_{o2} = V_{A2}D_e - V_{B2}. \tag{27}$$

These expressions, together with the condition that the feedback signal is equal to the reference voltage, facilitate control design [6]. The output voltages, however, can also be expressed in terms of the impedances as shown in Eqs. (11) and (13). The impedance form makes it easier to compare the voltage tracking ability, voltage offset amount, and power losses for various stacking schemes. The output voltages with impedance form can be generally expressed as:

$$V_{o1} = V_{s1}D_e - V_{d1} - I_{o1}Z_{11} - I_{o2}Z_{12}, \tag{28}$$

$$V_{o2} = (V_{s1} + V_{s2})D_e - V_{off} - I_{o1}Z_{21} - I_{o2}Z_{22}. \tag{29}$$

Table 1. summarizes the expressions for the constant offset voltage, V_{off}, and the impedances, Z_{ij}. The dc cross-regulation for each stacking scheme is calculated as shown in Fig. 14. Stacking at the output, scheme (b), gives the highest transimpedances, and therefore voltage tracking between the outputs is the best among the above-mentioned schemes. Stacking the freewheeling diodes, scheme (c), or stacking secondary windings, scheme (d), yields the smallest transimpedances and the worst voltage tracking. Stacking at the input of the output filter, scheme (a), or stacking the secondary windings and the freewheeling diodes simultaneously, scheme (e), gives intermediate transimpedances and voltage tracking ability. In terms of efficiency, the results are exactly opposite. Scheme (b) has maximum power loss, and schemes (c) and (d) have minimum power losses. Table 2 shows the comparison of power losses for different stacking schemes.

Table 2. Comparison of Power Losses for Various Schemes. (Total power loss before stacking: P=13.34 W)

Scheme	(a)	(b)	(c)	(d)	(e)
ΔP (W)	15.12	16.86	14.36	13.38	14.42
$\Delta P/P$ (%)	13.4	26.4	7.7	0.4	8.1

V. SUMMARY

Stacking of secondaries is a simple but effective method to improve dc cross-regulation for multiple-output converters without severely sacrificing efficiency. By stacking the secondaries, coupling between the power channels is introduced and the outputs can track each other as any load currents change. The voltage tracking ability depends on the transimpedances. Larger transimpedances yield good voltage tracking but poor efficiency. There is a trade-off between dc cross-regulation and efficiency. Analyses are performed for five stacking schemes, and the analytical results are experimentally verified on a dual-output forward converter.

ACKNOWLEDGEMENT

The authors wish to thank Mr. Juan Sabate and Mr. Phuong Huyuh for their help to translate the title and the abstract into French.

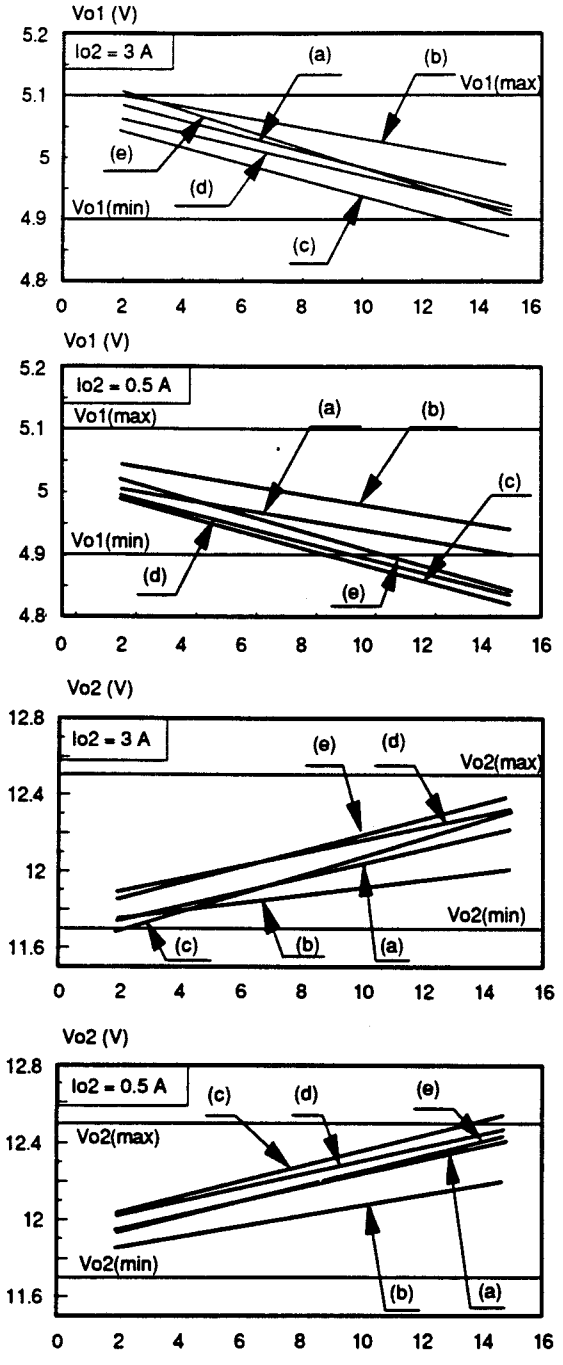

Fig. 14. Comparison of the dc regulation for different stacking schemes: (a) - (e) correspond to the 5 stacking schemes discussed above.

REFERENCES

[1] T. G. Wilson, Jr., "Cross Regulation in an Energy-Storage DC-to-DC Converter with Two Regulated Outputs," *IEEE Power Electronics Specialists Conf. Rec.*, 1977, pp. 190-199.

[2] T. G. Wilson, Jr., "Cross Regulation in a Two-Output DC-to-DC Converter with Application to Testing of Energy-Storage Transformer," *IEEE Power Electronics Specialists Conf. Rec.*, 1978, pp. 124-134.

[3] K. Harada, T. Nabeshima, and K. Hisanaga, "State-Space Analysis of the Cross-Regulation," *IEEE Power Electronics Specialists Conf. Rec.*, 1979, pp. 186-192.

[4] H. Matsuo, "Comparison of Multiple-Output DC-DC Converters Using Cross Regulation," *IEEE Power Electronics Specialists Conf. Rec.*, 1979, pp. 169-185.

[5] F. Kurokawa and H. Matsuo, "A New Multiple-Output Hybrid Power Supply," *IEEE Trans. Power Electronics*, vol. 3, no. 4, pp. 412-419, 1988.

[6] Q. Chen, M.M. Jovanović, and F.C. Lee, "DC Analysis and Design of Multiple-Output Forward Converters with Weighted Voltage-Mode Control," *Proc. IEEE Applied Power Electronics Conf.*, March 1993.

[7] G. Perica, "Elimination of Leakage Effects Related to the Use of Winding with Fractions of Turns," *IEEE Trans. Power Electronics*, vol. 1, no. 1, pp. 39-47, 1986.

[8] C.C. Liu, K.H. Ding, J.R. Young, and J.F. Beutler, "A Systematic Method for the Stability Analysis of Multiple-Output Converters," *IEEE Trans. Power Electronics*, vol. 2, no. 4, pp. 343-353, 1989.

[9] G. C. Johari, "An Incremental Output Dual Sense Scheme to Improve Cross Regulation of a Multiple Output Switching Regulator," *Power Conversion International*, pp. 9-18, 1979.

[10] C. E. Mullett, "Evaluating Approach to Multi-Output Power Converter Designs," *Proc. of PCI*, Sept. 1987, pp. 304-323.

[11] C. L. Jamerson, "Post-Regulation Techniques for 100 kHz to 300 kHz Multiple-Output PWM Supplies," *Proc. of High Frequency Power Conversion*, May 1989, pp. 260-273.

[12] G. C. Chryssis, "High-Frequency Switching Power Supplies: Theory and Design," 2nd edition, McGraw-Hill, New York,1989.

[13] L. H. Dixon, Jr, "The Effects of Leakage Inductance on Switching Power Supply Performance," *Unitrode Power Supply Design Seminar Book*, 1988, pp. p2-1 - p2-7.

[14] K. H. Liu, "Effects of Leakage Inductances on the Cross Regulation in a Discontinuous-Mode Flyback Converter," *Proc. of High Frequency Power Conversion*, May 1989, pp. 254-259.