Interleaved PFC Boost Converter with Intrinsic Voltage-Doubler Characteristic

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Abstract — A novel, two-inductor, interleaved PFC boost converter that exhibits voltage-doubler characteristic when it operates with a duty cycle greater than 0.5 is introduced. The voltage-doubler characteristic of the proposed converter makes it quite suitable for universal-line (90-264 V_{RMS}) PFC applications. Because the proposed PFC boost rectifier operates as a voltage doubler at low line, its low-line range efficiency is greatly improved compared to that of its conventional counterpart. The performance of the proposed PFC rectifier was evaluated on an experimental 1.3-kW universal-line PFC prototype.

I. INTRODUCTION

To comply with various worldwide specifications governing the harmonic limits of the line current in off-line power supplies, the front-end power-factor-corrected (PFC) boost converter has been used almost exclusively in off-line power supplies for computer and telecom applications. However, in universal-line (90-264 V_{RMS}) PFC applications, the boost converter exhibits a significant degradation of performance over the line-voltage range, [1]. Specifically, the low-line (90 V_{RMS}) operation of the boost rectifier is much less efficient than high-line (264 V_{RMS}) operation. Generally, an improvement of the low-line efficiency of the conventional PFC boost rectifier can be obtained by configuring the rectifier to work as a voltage doubler at low line.

Several boost voltage-doubler topologies have been introduced in [2] and [3]. However, the topologies described in [2] are not suitable for PFC applications in universal-input computer/telecom power supplies since they require the PFC stage output voltage to be at least twice that of the maximum line voltage, *i.e.*, approximately 800 V. This increased voltage at the output of the PFC front end puts undue burden on the cost and performance of the downstream dc/dc converters. The boost PFC voltage-doubler circuit introduced in [3] can work in the entire universal-line range with an output voltage slightly higher than the maximum line voltage, *i.e.*, around 400 V. However, the circuit requires a number of range-select switches to reconfigure the converter to the voltage doubler at low line. Generally, the employment of mechanical range-select switches is not allowed in server applications and electronic range-select switches are not desirable because of their detrimental effect on efficiency, as well as possible reliability issues and increased cost.

In high-power applications, interleaving of two boost converters is very often employed to improve performance and reduce size of the PFC front end. Namely, because interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, the size of the energy-storage inductors and differential-mode EMI filter in interleaved implementations can be reduced [4], [5].

This paper presents a two-inductor, interleaved, boost PFC converter with voltage-doubler characteristic that does not require any range-select switches and that can regulate the output voltage at around 400 V in the entire universal-range line voltage.

II. ANALYSIS OF OPERATION

The conventional interleaved PFC boost rectifier is shown in Fig. 1, whereas Fig. 2 shows the proposed interleaved PFC boost converter with voltage-doubler characteristic. As can be seen from Figs. 1 and 2, the proposed circuit is quite similar to the conventional interleaved PFC boost converter. Since the proposed rectifier also operates with interleaved gate signals, the input current waveform and the differential-mode EMI performance of the proposed circuit in Fig. 2 are nearly identical to those of the conventional interleaved PFC rectifier in Fig. 1. It should also be noted that the proposed boost converter shares similar characteristics with the high-gain dc/dc boost converter circuit introduced in [6].

To facilitate the explanation of the circuit's operation, Fig. 3 shows a simplified circuit diagram of the circuit in Fig. 2. Assuming that blocking capacitor C_B and filter capacitor C_F are large enough that the voltage ripples across them are small compared to their dc voltages, blocking capacitor C_B and filter capacitor C_F are modeled as voltage

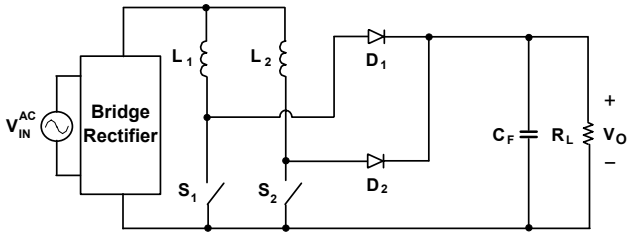


Fig. 1. Conventional interleaved PFC boost converter.

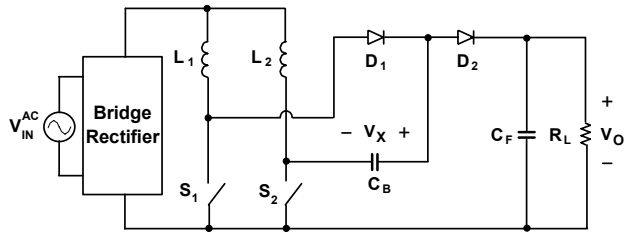


Fig. 2. Proposed interleaved PFC boost converter with voltage-doubler characteristics.

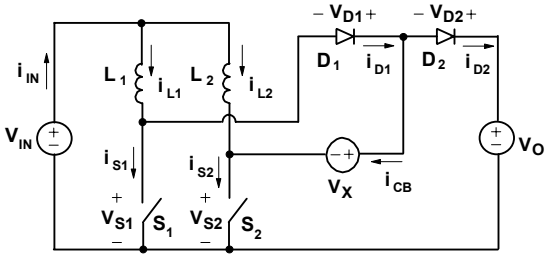


Fig. 3. Simplified circuit diagram of the proposed circuit along with reference directions of key currents and voltages.

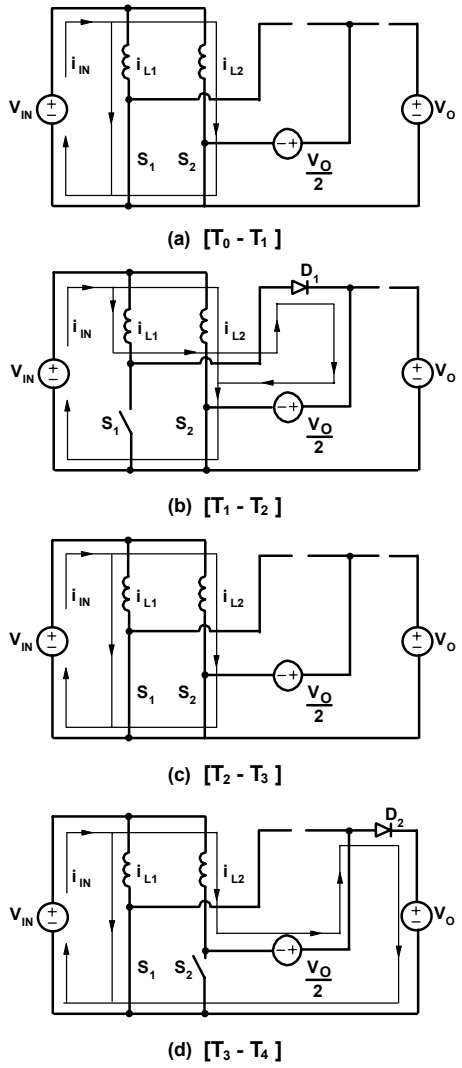


Fig. 4. Topological stages (0.5≤D<1).

sources V_X and V_O, respectively. In this analysis it is also assumed that all semiconductor components are ideal, *i.e.*, they represent zero impedances in the on state and infinite impedances in the off state.

To further facilitate the analysis of operation, Fig. 4 shows the topological stages of the circuit in Fig. 3 during a switching cycle when the rectifier operates with a duty cycle greater than 0.5, whereas Fig. 5 shows its key waveforms.

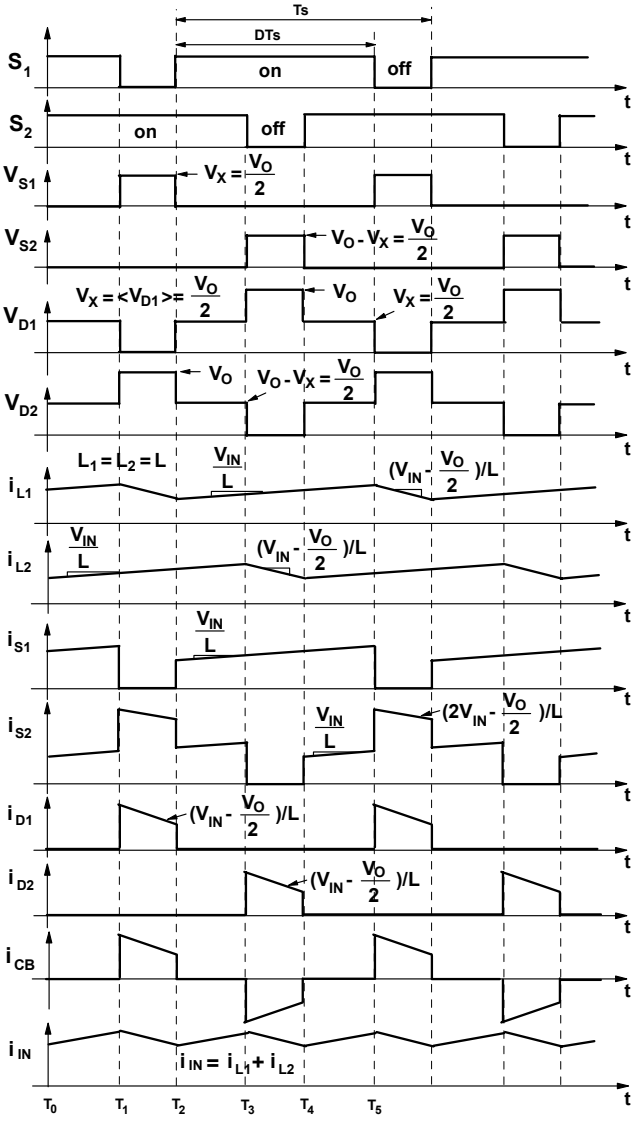


Fig. 5. Key ideal waveforms (0.5≤D<1).

The reference directions of currents and voltages plotted in Fig. 5 are shown in Fig. 3. As can be seen from the timing diagrams of the control signals for switches S_1 and S_2 shown in Fig. 5, switches S_1 and S_2 conduct simultaneously, *i.e.*, they operate with overlapping control signals. It should be noted that during this mode of operation, voltage V_X across blocking capacitor C_B is equal to the average voltage across diode D_1 because the average voltages across inductors L_1 and L_2 are zero. By simple observations from the voltage across diode D_1 in Figs. 3 and 5, voltage V_X across blocking capacitor C_B can be easily derived. Namely, during the period when switch S_1 is off, the voltage across diode D_1 is zero because diode D_1 conducts the current of boost inductor L_1. During the period when switch S_2 is off, the voltage across diode D_1 is output voltage V_O because diode D_2 conducts the current of boost inductor L_2 and switch S_1 is on. Finally, the voltage across diode D_1 is equal to capacitor voltage V_X during the period when both switches

S_1 and S_2 are on. Because the off time of switches S_1 and S_2 are identical as shown in Fig. 5, the voltage across blocking capacitor C_B is one-half of the output voltage, *i.e.*, $V_X=V_O/2$.

The topological stages in a switching cycle are shown in Fig. 4. During the time interval when both switches are on, *i.e.*, during the time interval $T_0 - T_1$ in Fig. 5, inductor currents i_{L1} and i_{L2} are increasing at the same rate. The rate of change of i_{L1} and i_{L2} can be calculated from Fig. 4(a), which represents the equivalent circuit diagram of the converter during the time interval $T_0 - T_1$. According to Fig. 4(a),

$$V_{IN} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt}. \quad (1)$$

If both inductances have the same value $L=L_1=L_2$, it follows that

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{IN}}{L}, \quad (2)$$

as illustrated in Fig. 5.

The output is decoupled from the input when both switches are on and rectifiers D_1 and D_2 are reverse biased. As a result, during this stage the load current is supplied from the filter capacitor C_F.

When at $t=T_1$, switch S_1 is turned off, inductor current i_{L1} is diverted from the switch to rectifier D_1, as shown in Fig. 4(b), and the energy stored in inductor L_1 starts to discharge into blocking capacitor C_B. During this stage, current i_{L1} decreases. The rate of current decrease can be found from the equivalent circuit shown in Fig. 4(b) as

$$V_{IN} = L_1 \frac{di_{L1}}{dt} + \frac{V_O}{2}. \quad (3)$$

From Eq. (3), assuming $L=L_1$, it follows that

$$\frac{di_{L1}}{dt} = \frac{1}{L}\left(V_{IN} - \frac{V_O}{2}\right). \quad (4)$$

During the topological stage shown in Fig. 4(b), current i_{L1} charges blocking capacitor C_B.

When at $t=T_2$, switch S_1 is turned on again and the circuit enters the topological stage shown in Fig. 4(c), which is identical to the topological stage in Fig. 4(a). During this stage, both switches are on and both inductor currents i_{L1} and i_{L2} increase at the same rate given by Eq. (2).

The converter enters the final topological stage shown in Fig. 4(d) at $t=T_3$ when switch S_2 is turned off and current i_{L2} is commutated from switch S_2 into rectifier D_2. During this stage, energy stored in inductor L_2 during the preceding topological stages discharges into filter capacitor C_F through blocking capacitor C_B. The rate of current decrease can be found from the equivalent circuit shown in Fig. 4(d) as

$$V_{IN} = L_2 \frac{di_{L2}}{dt} - \frac{V_O}{2} + V_O. \quad (5)$$

From Eq. (5), assuming $L=L_2$, it follows that

$$\frac{di_{L2}}{dt} = \frac{1}{L}\left(V_{IN} - \frac{V_O}{2}\right). \quad (6)$$

The rate of decrease of current i_{L2} is equal to that of current i_{L1}. The circuit enters a new switching cycle at $t=T_4$ when switch S_2 is turned on again.

The voltage conversion ratio of the circuit can be calculated from the volt-second balance on the boost inductors. From Fig. 5 and Eqs. (2) and (4), the volt-second balance equation for both boost inductors L_1 and L_2 is

$$V_{IN} D T_S = \left(\frac{V_O}{2} - V_{IN}\right) \cdot (1 - D) T_S, \quad (7)$$

so that

$$\frac{V_O}{V_{IN}} = \frac{2}{1 - D}, \ (0.5 \le D < 1). \quad (8)$$

As can be seen from Eq. (8), the proposed rectifier operates as a boost converter with a voltage doubler when its duty cycle is greater than 0.5. It should be noted that the duty cycle of a universal line PFC boost rectifier is greater than 0.5 for the most of line cycle when it operates from the minimum operating voltage that is typically 85 V_{RMS}.

Because the voltage step-up ratio of the proposed rectifier at low line is only one-half of the step-up ratio of the conventional interleaved PFC boost rectifier, the RMS switch current of the proposed interleaved boost rectifier is smaller than that of the conventional interleaved PFC boost rectifier. The ratio of the RMS switch currents during a switching cycle is

$$\frac{I_{RMS,\,interleaved\_doubler}}{I_{RMS,\,interleaved\_boost}} = \sqrt{\frac{M-2}{M-1}}, \ (0.5 \le D < 1), \quad (9)$$

where $M = V_O/V_{IN}$, and $M \ge 4$. The switch conduction loss of the proposed rectifier at M=4 is approximately 67% of the switch conduction loss of the conventional interleaved PFC boost rectifier. Moreover, the blocking voltage of the switches and diodes are only one-half of the output voltage. The turn-on and turn-off losses of the switches and the reverse recovery losses of the diodes in the proposed rectifier are much smaller than those of the conventional interleaved PFC boost rectifier. As a result, the proposed rectifier achieves the same advantages of the conventional boost voltage doubler converter, such as low conduction loss and smaller switching losses, at low line.

Figure 6 shows the topological stages of the circuit in Fig. 3 during a switching cycle when the rectifier operates with a duty cycle smaller than 0.5, whereas Fig. 7 shows its key waveforms. By simple observations from the voltage across diode D_1 in Figs. 3 and 7, voltage V_X across blocking capacitor C_B can be easily derived. In this mode of operation, the voltage across diode D_1 is equal to output voltage V_O during the period when switch S_1 is on, *i.e.*, DT_S. The voltage across diode D_1 is zero during the period when switch S_1 is off, *i.e.*, $(1-D)T_S$. As a result, voltage V_X across blocking capacitor C_B is DV_O, which is equal to the average voltage across diode D_1, *i.e.*, $V_X=DV_O$.

During the time interval when both switches are off, *i.e.*, during the time interval $T_0 - T_1$ in Fig. 7, inductor currents i_{L1} and i_{L2} are decreasing. The rate of change of i_{L1} can be calculated from Fig. 6(a), which represents the equivalent circuit diagram of the converter during the time interval $T_0 - T_1$. According to Fig. 6(a),

$$V_{IN} = L_1 \frac{di_{L1}}{dt} + V_O. \quad (10)$$

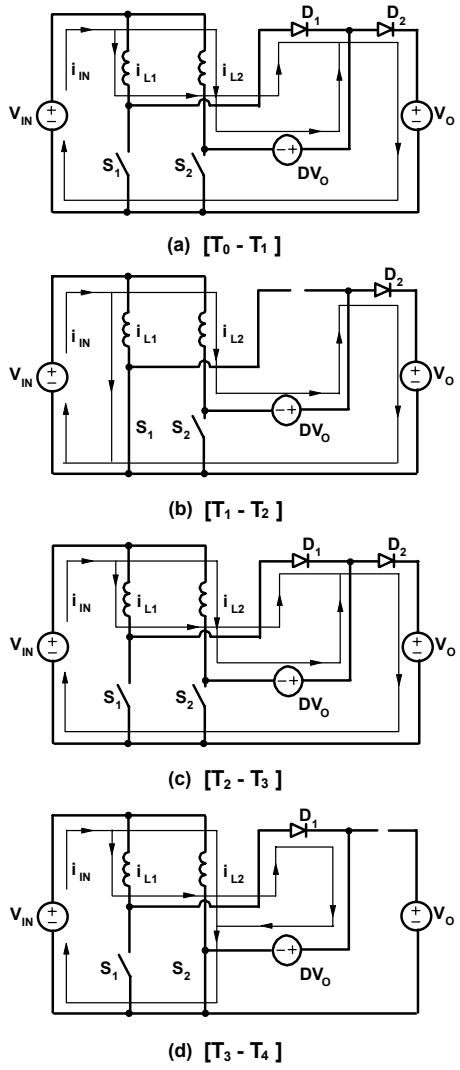


Fig. 6. Topological stages (0≤D≤0.5).

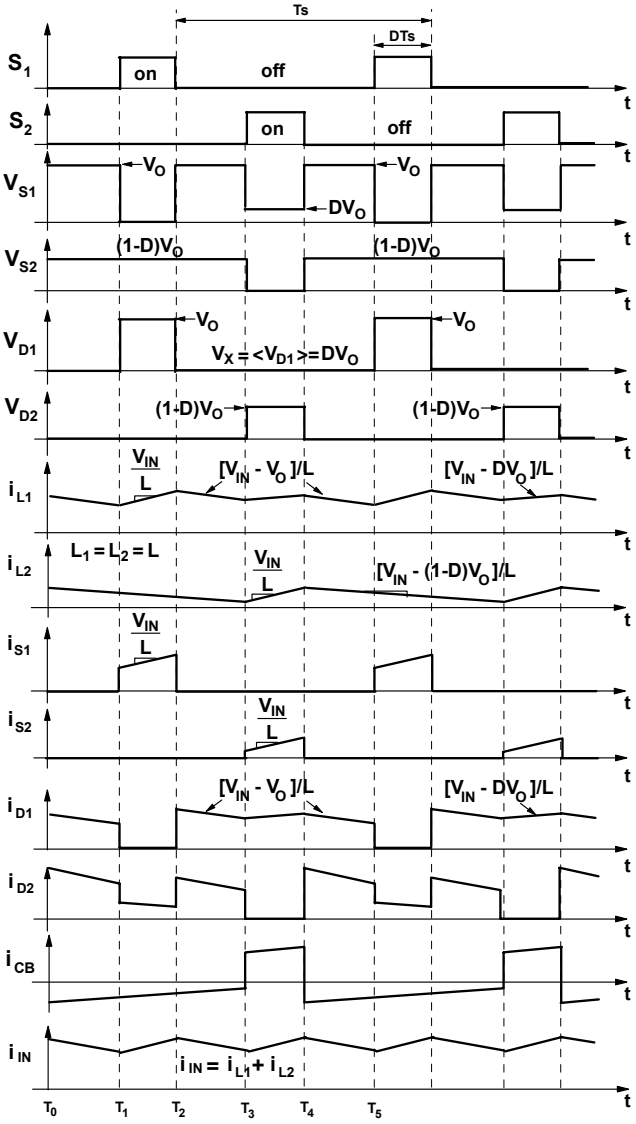


Fig. 7. Key ideal waveforms (0≤D≤0.5).

From Eq. (10), assuming $L=L_1$, it follows that

$$\frac{di_{L1}}{dt} = \frac{1}{L}\left(V_{IN} - V_O\right). \quad (11)$$

The rate of change of i_{L2} can be also calculated from Fig. 6(a). According to Fig. 6(a),

$$V_{IN} = L_2 \frac{di_{L2}}{dt} - DV_O + V_O. \quad (12)$$

From Eq. (10), assuming $L=L_2$, the rate of change of i_{L2} follows that

$$\frac{di_{L2}}{dt} = \frac{1}{L}\left[V_{IN} - (1-D)V_O\right]. \quad (13)$$

When at $t=T_1$, switch S_1 is turned on. During the time interval $T_1 - T_2$ in Fig. 7, inductor current i_{L1} increases. The rate of change of i_{L1} can be calculated from Fig. 6(b), which represents the equivalent circuit diagram of the converter during the time interval $T_1 - T_2$. According to Fig. 6(b),

$$V_{IN} = L_1 \frac{di_{L1}}{dt}. \quad (14)$$

From Eq. (14), assuming $L=L_1$, the rate of change of i_{L1} follows that

$$\frac{di_{L1}}{dt} = \frac{V_{IN}}{L}, \quad (15)$$

as indicated in Fig. 7. During this stage, current i_{L2} continuously decreases with the slope given by Eq (13).

When at $t=T_2$, switch S_1 is turned off again and the circuit enters the topological stage shown in Fig. 6(c), which is identical to the topological stage in Fig. 6(a). During this stage, both switches are off and both inductor currents i_{L1} and i_{L2} decrease at the rates given by Eq. (11) and Eq. (13), respectively.

The converter enters the final topological stage shown in Fig. 6(d) at $t=T_3$ when switch S_2 is turned on and current i_{L2} is commutated from diode D_2 into switch S_2. During this time interval $T_3 - T_4$ in Fig. 7, inductor currents i_{L1} and i_{L2} are increasing. The rate of change of i_{L1} can be calculated from Fig. 6(d). According to Fig. 6(d),

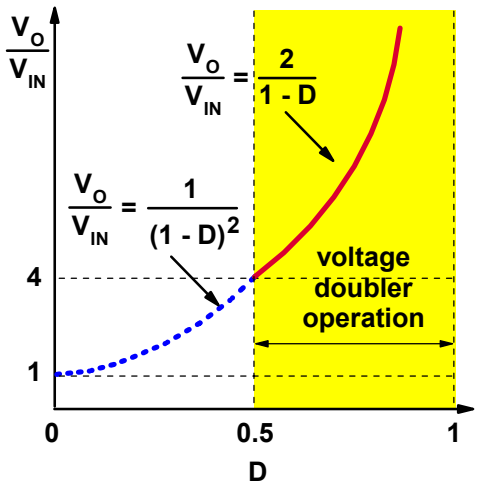


Fig. 8. Voltage gain of proposed rectifier.

$$V_{IN} = L_1 \frac{di_{L1}}{dt} + DV_O . \quad (16)$$

From Eq. (16), assuming L=L_1, it follows that

$$\frac{di_{L1}}{dt} = \frac{1}{L}\left(V_{IN} - DV_O\right). \quad (17)$$

The rate of change of i_{L2} can be calculated from Fig. 6(d). According to Fig. 6(d),

$$V_{IN} = L_2 \frac{di_{L2}}{dt} . \quad (18)$$

From Eq. (16), assuming L=L_2, the rate of change of i_{L2} follows that

$$\frac{di_{L2}}{dt} = \frac{V_{IN}}{L} . \quad (19)$$

The circuit enters a new switching cycle at t=T_4 when switch S_2 is turned off again.

The voltage conversion ratio of the circuit can be calculated from the volt-second balance of the boost inductors. From Fig. 7 and Eqs. (11), (15), and (17), the volt-second balance equation for boost inductors L_1 is

$$\left(2V_{IN} - DV_O\right)DT_S = \left(V_O - V_{IN}\right)\cdot\left(1 - 2D\right)T_S , \quad (20)$$

so that

$$\frac{V_O}{V_{IN}} = \frac{1}{(1 - D)^2} , \ (0 \le D \le 0.5). \quad (21)$$

From Eq. (21), it should be noted that the minimum voltage gain of the proposed rectifier is unity when the duty cycle is zero. Because of this voltage gain characteristic, the proposed rectifier can regulate its output voltage at high line without using any range-select switches.

The voltage gain of the proposed rectifier is shown in Fig. 8. Since the voltage gain is monotonically changed by the duty cycle and is identical to those of the conventional boost converter at each minimum and maximum duty cycle, any commercially available PFC control IC can be employed for the proposed rectifier. In fact, the proposed rectifier requires a PFC control circuit and a gate drive circuit that are identical to those of the conventional interleaved PFC rectifier. However, there is an exception for the current sharing circuit. Because blocking capacitor C_B automatically balances the average currents of inductors L_1 and L_2, the proposed rectifier does not require an active current sharing circuit that is required in the conventional interleaved PFC boost rectifier.

III. EXPERIMENTAL RESULTS

The performance of the proposed interleaved PFC boost converter in Fig. 2 was evaluated and compared to the performance of the conventional interleaved converter in Fig. 1 by building a 1.3-kW prototype circuit designed to operate from a universal ac-line input (85 V_{RMS}-265 V_{RMS}) and deliver up to 3.25 A of load current at a 400-V output. The prototype was constructed to test both proposed and conventional circuits by a simple modification since both power stage circuits are similar to each other.

In both implementations, an SPW47N60C3 MOSFET (V_{DSS} = 600 V, I_{D25} = 47 A, R_{DS} = 0.07 Ω) from Infineon was used for each switch, whereas an STTH1506 Tandem diode (V_{RRM} = 600 V, I_{FAVM} = 15 A) from ST was used for each output diode. Each boost inductor was built using two toroidal cores (Magnetics, high flux 58894-A2) and a 57 turns of magnet wire (AWG #18). Two aluminum capacitors (560 μF, 450 VDC) were used as output capacitor C_F. In the prototype of the proposed circuit in Fig. 2, two paralleled polypropylene capacitors (2.2 μF, 250 VDC) were used to implement capacitor C_B.

Figure 9 shows the measured efficiencies of the conventional interleaved PFC boost rectifier (dashed lines) and the proposed PFC rectifier (solid lines) for minimum line voltage V_{IN}=85 V and maximum line voltage V_{IN}=265 V. As can be seen in Fig. 9, at minimum line voltage V_{IN}=85 V, the efficiency of the proposed PFC rectifier is

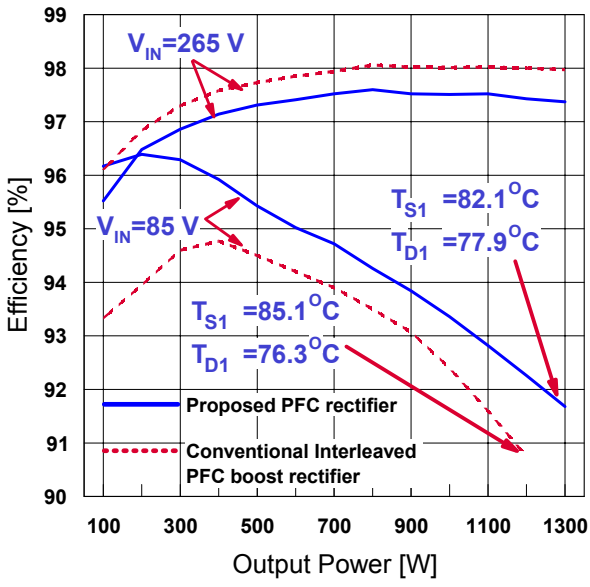


Fig. 9 Measured efficiency of the 100-kHz, 1.3-kW experimental rectifiers at V_{IN}=85 and 265 V_{AC} and V_O=400 V as functions of output power.

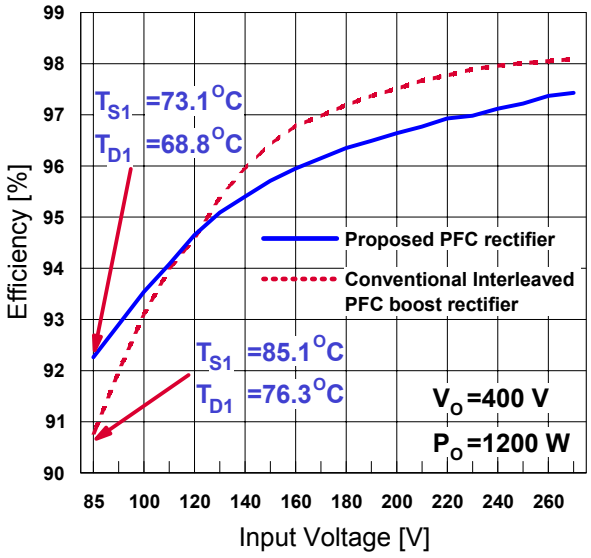


Fig. 10 Measured efficiency of the experimental rectifiers at P_O=1.2 kW and V_O=400 V as functions of line voltage. It should be noted that the conventional interleaved PFC boost rectifier couldn't deliver 1.3 kW output power because of high switch temperature at the minimum line voltage.

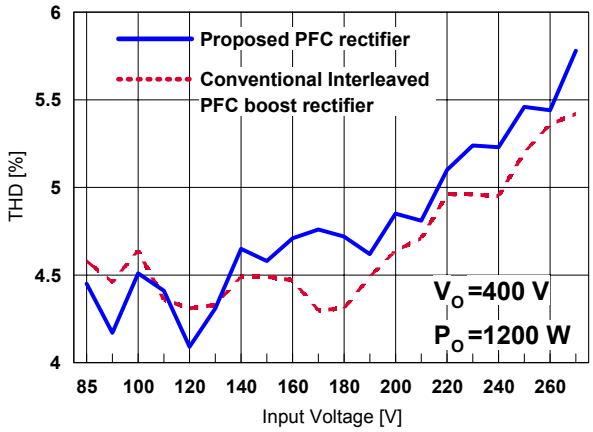


Fig. 11 Measured THD of the experimental rectifiers at P_O=1.2 kW and V_O=400 V as functions of line voltage.

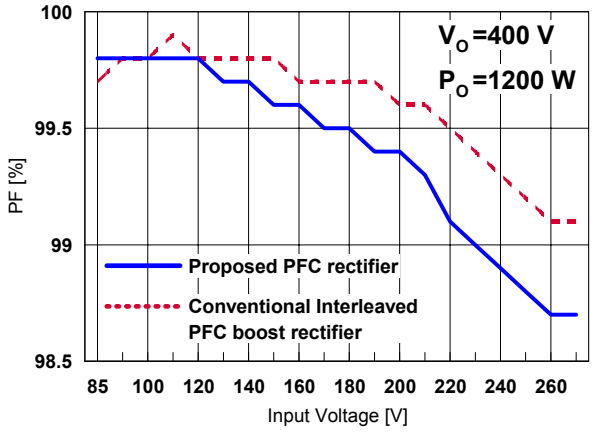


Fig. 12 Measured PF of the experimental rectifiers at P_O=1.2 kW and V_O=400 V as functions of line voltage.

significantly higher than that of the conventional interleaved PFC boost rectifier over the entire load range. Because the duty cycle of the proposed PFC rectifier is always greater than 0.5 at minimum line voltage, the circuit operates as a voltage doubler over the whole line cycle. As indicated in Eq. (9), the switch conduction loss of the proposed rectifier is approximately two-thirds of the switch conduction loss of the conventional interleaved PFC boost rectifier. In addition, the turn-on and turn-off losses of the switches and the reverse recovery losses of the diodes in the proposed rectifier are much smaller than those of the conventional interleaved PFC boost rectifier because the voltages across the switches and the diodes are one half of output voltage V_O when they are switching as shown in Fig. 5. It should be noted that the efficiency improvement at lighter loads is more pronounced because switching losses are dominant at this condition.

From Fig. 9 it can be seen that at maximum line voltage V_{IN}=265 V, the proposed rectifier exhibits a lower efficiency than the conventional interleaved boost rectifier because the proposed circuit has increased conduction losses in series-connected rectifiers D_1 and D_2 when it operates with duty cycle less than 0.5. It should be noted that this slightly reduced efficiency at maximum line has no tangible effect on the overall performance of the converter since the thermal design and, therefore, the power-density of the converter is determined by the minimum full-load efficiency that occurs at minimal line voltage. In fact, due to an improved efficiency at minimal line voltage, the proposed converter has the potential to achieve a higher power density than its conventional counterpart.

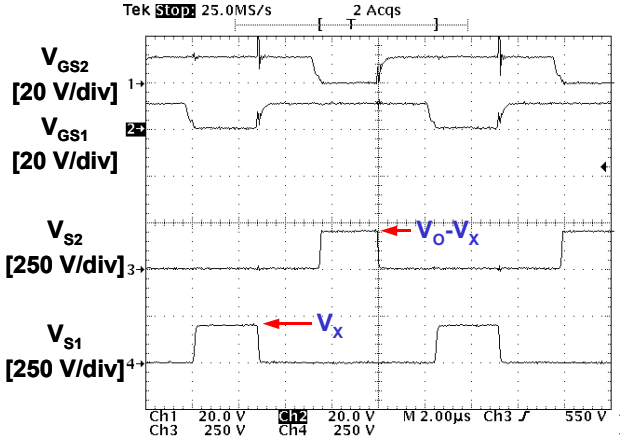
Figure 10 shows measured efficiencies as functions of the input voltage. To compare the efficiencies, both rectifiers were operated at 1.2 kW since the conventional interleaved rectifier could not deliver 1.3 kW at the acceptable switch temperature.

Figures 11 and 12 show measured total harmonic distortion (THD) and power factor (PF) as functions of the input voltage, respectively. The differences of the measured THD and PF between the proposed PFC boost converter and the conventional interleaved PFC boost converter are insignificant.

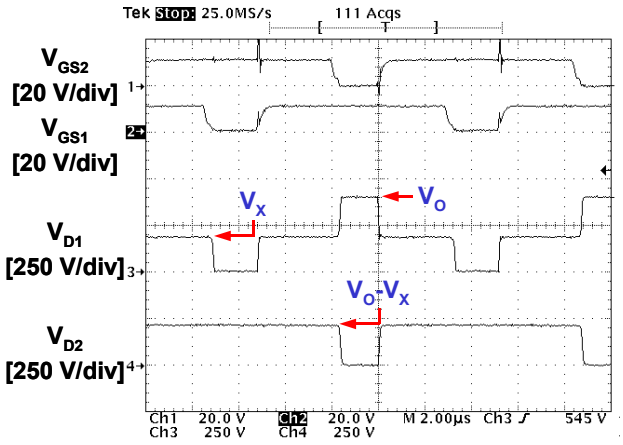
The oscillograms of key waveforms of the experimental prototype at full power and low line (D>0.5) are shown in Fig. 13. As can be seen from Fig. 13(a), the voltages across switches S_1 and S_2 are one half of output voltage V_O. The voltages across diodes D_1 and D_2 are shown in Fig. 13(b).

Finally, Fig. 14 shows the oscillograms of key waveforms of the experimental prototype at full power and high line (D<0.5). As can be seen from Fig. 14(a), the voltages across switches S_1 and S_2 are close to output voltage V_O. The voltages across diodes D_1 and D_2 are shown in Fig. 14(b).

It should be noted that at low line the proposed converter is expected to show better common-mode EMI performance

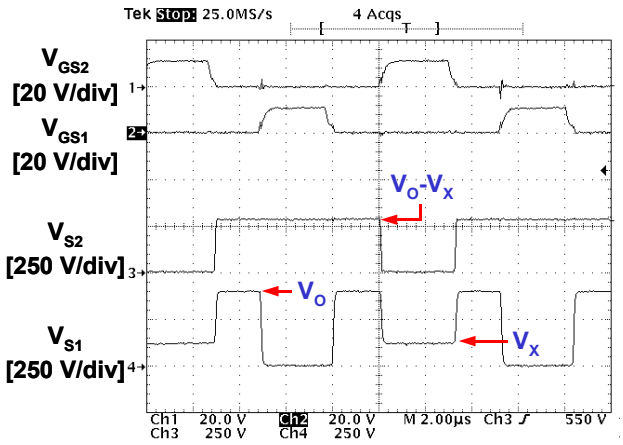


(a)

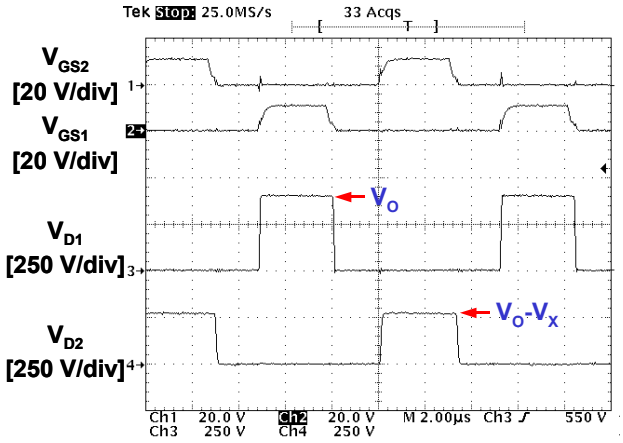


(b)

Fig. 13. Measured waveforms of the proposed circuit when duty cycle is greater than 0.5. Time base: 2 µs/div.



(a)



(b)

Fig. 14. Measured waveforms of the proposed circuit when duty cycle is smaller than 0.5. Time base: 2 µs/div.

compared to that of the conventional interleaved converter because as shown in Fig. 13 at low line all switches operate with lower drain-to-source voltages.

IV. SUMMARY

A novel two-inductor, interleaved boost PFC converter that exhibits voltage-doubler characteristic for duty cycles greater than 0.5 has been introduced. The voltage-doubler characteristic of the proposed converter makes it quite suitable for universal-line (90-264 V_{RMS}) PFC applications. The performance of the proposed PFC rectifier was evaluated on an experimental 1.3-kW PFC prototype that was designed to operate from a universal-line input and deliver up to 3.25 A at a 400-V output. The efficiency improvement at full load and low line is approximately 1.5%.

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