

Power Supply Technology – Past, Present, and Future

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Abstract — Technology for power systems of modern computer/telecom equipment is facing extremely tough challenges due to continuously increasing power-density and efficiency requirements. Meeting these requirements will require significant technology advancements in system architectures, devices and materials, topology optimization, and packaging/thermal design. In this paper, major technology challenges and future trends in each of these key technology areas are identified and briefly discussed.

I. INTRODUCTION

Ever since the start of the miniaturization era spurred on by the microelectronics revolution in the late fifties and early sixties, power conversion equipment employed in computer and telecommunication power systems has been facing continuously increasing power density and efficiency challenges. However, it was not until the introduction of high-voltage bipolar power transistors in the late sixties, which made replacing linear power supplies with high-frequency switch-mode power supplies possible, that a real opportunity for decreasing the size and weight and increasing the efficiency of power conversion circuits had been created [1].

Generally, linear power supply technology does not offer any significant opportunity for weight and size reduction because the size and weight is mainly determined by a line-frequency transformer and heatsink. Moreover, the opportunities to improve the efficiency are also very limited because the efficiency of linear power supplies is determined solely by the ratio of the output and input voltage. On the other hand, switch-mode power supply technology offers a significant size and weight reduction because it eliminates the need for bulky line-frequency magnetics and also decreases the size of heatsinks due to a much improved efficiency compared to that of linear power supplies. Generally, the efficiency and size optimization of switch-mode power supplies is based on finding a switching frequency where the trade-off between the conduction and switching losses is optimized.

Although switch-mode power supply technology has brought about dramatic power density improvements compared to linear power supply technology, further power density increases were enabled by the introduction of power MOSFET devices in the early and mid seventies. MOSFET technology together with advancements in power magnetics made it possible to significantly increase the switching frequency and, thus, reduce the size of magnetic components. While the frequency range of early switch mode power supplies implemented with bipolar power devices was limited to several kilohertz, MOSFET devices have allowed for switching frequencies to be pushed into the hundred-kilohertz and even megahertz range. Because the maximum switching frequency of a power converter is related to its output power level, input voltage range, and galvanic isolation requirements, the typical switching frequency range of dc-dc converters is higher than that of off-line converters, as illustrated in Fig. 1. As can be seen from Fig. 1, today's low-power, non-isolated voltage regulators (VRs) and point-of-load (POL) converters whose input voltage is in the 5-V to 12-V range operate at switching frequencies in excess of 1 MHz, whereas ac-dc converters that require transformer isolation and whose rms line voltage is from 90 V to 265 V typically operate with switching frequencies in the 80-200-kHz range.

Historically, the major improvements of power densities first occurred in dc/dc converters in the mid eighties with the introduction of a family of high-frequency dc-dc modules by Vicor Corporation. Employing a proprietary zero-

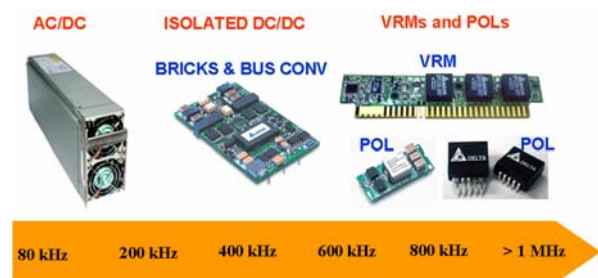


Fig. 1 Typical switching frequency ranges of today's power converters.

current switching quasi-resonant technology that had enabled the operation in the megahertz range together with advanced packaging, Vicor managed to push the power density of 48-V input dc/dc modules, also known as “bricks,” into an unprecedented power density range of 10-20 W/in³ [2]. This increasing power-density trend has been sustained ever since so that today’s dc/dc “bricks” can deliver much more power from the same volume, or the same power from a much smaller volume, as shown in Fig. 2. It should be noted that for low output-voltage bricks, specifically for those with output voltage 3.3 V and below, a more appropriate metrics for the brick capability is the maximum output current rather than the maximum output power, i.e., power density.

Off-line power supplies did not see a dramatic change in power density until the beginning of the rapid growth of the Internet in the late nineties that has led to an unprecedented escalation in the employment of data-processing, networking, and storage equipment and has created strong demand for equipment and, therefore, for power supplies with much higher power densities. As shown in Fig. 3, over the past five-six years the power density of ac/dc power supplies such as notebook adapters, multiple-output power supplies, and server front ends for distributed power systems had been significantly increased. For example, while a typical power density of server front-end power supplies was in the 5 W/in³ range just five-six years ago, the power density of these power supplies today is in the 20 W/in³ range. As this trend continues, power supplies in excess of 30W/in³ will be available in a few years. These dramatic power density gains have been primarily enabled by the availability of better

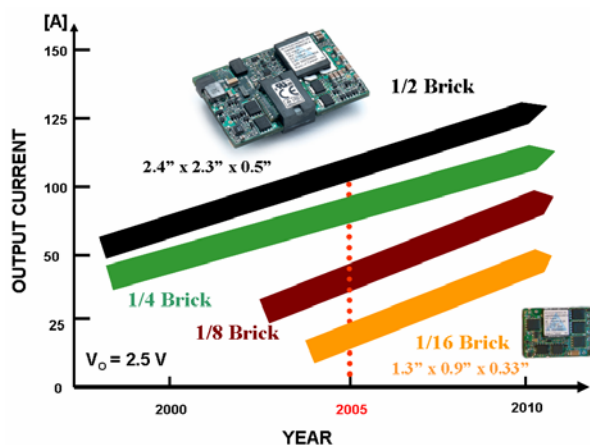


Fig. 2 Past, present, and projected output current capability of dc/dc bricks. Data given for bricks with 2.5-V output and 36-75-V input voltage range.

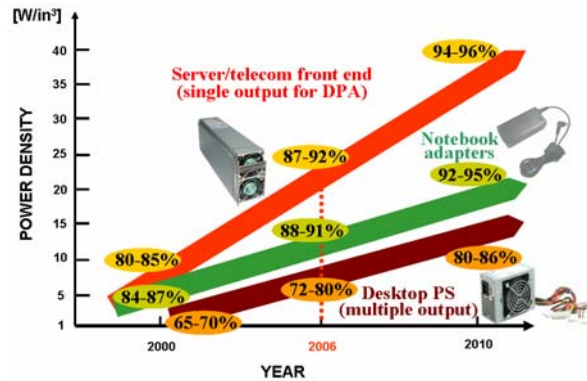


Fig. 3 Past, present, and projected power densities and efficiencies of ac/dc notebook adapters, multiple-output power supplies, and server front ends for distributed power systems.

components and improved understanding of design optimization trade-offs that has helped increase efficiency, as well as by the use of advanced packaging techniques.

II. PARADIGM SHIFT

Until recently, efficiency increases of power conversion circuits were primarily driven by increased power density requirements since power density increases are only possible if appropriate incremental improvements in full-load efficiency are achieved so that the thermal and acoustic performance are not adversely affected. As a result, maximization of the full-load efficiency has been a design focus all along. However, in the early nineties, the explosive growth of consumer electronics and data-processing equipment had prompted the introduction of various, mostly voluntary, requirements aimed at minimizing the idle-mode, i.e., light-load, power consumption. Meeting these ever-stringent light-load efficiency requirements, most notably those defined in German Blue Angle, U.S. Energy Star, Japan Top Runner, and ECoC (European Code of Conduct) specifications [3], pose major design challenges to power supply manufacturers. As a result, significant R&D resources have been dedicated by both power supply manufacturers and control IC providers to developing technologies to comply with these specifications [3]-[6].

Today, the power supply industry is at the beginning of a major focus shift that puts efficiency improvements across the entire load range in the forefront of customers’ performance requirements. This focus on efficiency has been prompted by economic reasons and environmental concerns caused by the continuous, aggressive growth of the Internet infrastructure and a relatively low energy

efficiency of power delivery systems of large Internet-equipment hosting facilities.

As illustrated in Fig. 4, which shows a block diagram of the power delivery system of a typical large data center (server farm/hotel), for each Watt consumed by data processing, more than two Watts are wasted in power conversion and cooling. With steadily decreasing prices of datacom equipment, the cost of electricity over the equipment lifetime has become a significant fraction of the initial acquisition cost, especially for low-end equipment such as “blade”, 1U, and 2U servers (where “U” is a unit of height measuring 1.75 inches or 4.45 cm), where presently the cost of power and cooling exceeds the acquisition cost in approximately three years [7]. As a result of the increasing impact of energy cost on the total cost of ownership, efficiency considerations have started to have a significant influence on equipment acquisition decisions.

In addition, ever-increasing power consumption of IT equipment and in particular that of fast-growing large data center facilities has started to have a serious environmental impact. For example, the 2006 power consumption of IT equipment in the U.S. was estimated at approximately 90 TWhr, which is equivalent to 1.2 million barrels of oil and contributes to around 100 million tons of CO₂ emission [8]. With projected future annual power consumption increases of data centers in the 10-15% range, the environmental concerns have

prompted various initiatives to compel makers of IT equipment to increase the power conversion efficiency of their equipment. In fact, incentive programs, such as 80Plus [9], are already in place to entice power supply companies to start offering power supplies for computer/telecom applications that maintain efficiency above 80% in the entire load range from full load down to 20% of full load. The 80Plus specifications will be incorporated into U.S. Environmental Protection Agency’s (EPA) Energy Star specifications scheduled to go into effect on July 20, 2007 [10].

However, minimizing the electric power waste in large data centers not only requires significant technology advancements in the power conversion and delivery area, but also in the cooling system, as well as in the power consumption of data-processing circuits themselves. The major processor makers are already working on technologies that are aimed at reducing the power consumption without degrading the performance. Technologies such as load dependent processor speeds, native multi-core processors, and internal memory controllers are some of the latest approaches in power consumption minimization at the component and equipment level [11]-[12]. At the system level, software technologies that will reduce power consumption of data centers by dynamic optimization of data-processing-capacity utilization are being developed [13]. This so-called server virtualization technologies reduce the power consumption in large datacom systems during periods when their capacity is not fully utilized by concentrating processing activity in a minimal number of servers and turning the excess servers off. This approach that is based on predicted demand and real-time data saves energy by removing the power consumption of idling equipment.

Cooling equipment manufacturers and system designers are also working on technologies to improve the cooling efficiency of data centers. The optimization of fans/blowers, cooling medium, and data center floor layout are currently the areas of major focus. System level techniques such as system-integrated intelligent cooling that is based on actual thermal load and predicted demand are also being rapidly developed [13].

III. TECHNOLOGY CONSIDERATIONS

The major activities aimed at improving the performance of the power conversion and delivery system of data centers are always focused on four key technology areas, as shown in Fig. 5.

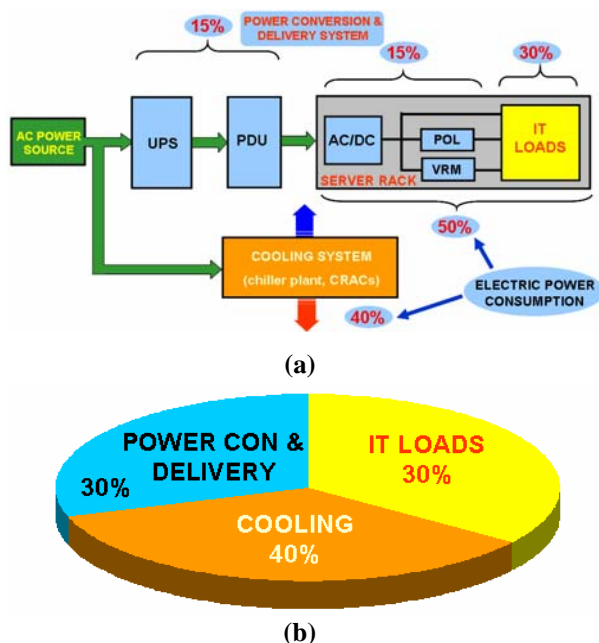


Fig. 4 Power delivery system for large data centers (server farms / hotels): (a) block diagram; (b) power consumption breakdown.

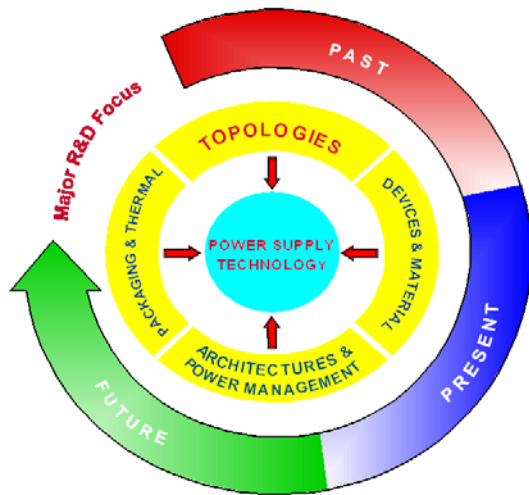


Fig. 5 Major power supply technology areas past, present, and future focus.

While in the past the major performance improvements had been primarily brought about by refinements in power converter topologies and advancements in semiconductors and magnetic materials, the future efficiency and power density improvements are expected to come mostly from system architecture and power management optimization, as well as from advancements in packaging and thermal management techniques. As a result, the current R&D focus has shifted from converter-level topology optimization to system-level architecture optimization and implementation of load-activity-based power management [14]-[15]. Recognizing that power management (PM) capability will be an indispensable and integral part of future power systems, the digital power management bus has already been standardized by PMBus Implementers Forum [16]. The major objective of this new open communication standard for power system management is to facilitate product development based the PMBus specifications. Presently, a number of suppliers of ICs for power conversion applications have introduced PMBus compliant products [17]-[21]. In addition to PMBus compliance for digital power management, some of the ICs offer digital control as well [17]-[21]. Generally, while digital power management can optimize performance at the system level, i.e., through dynamic bus voltage optimization [14]-[15], digital control makes it possible to optimize the converter-level efficiency in the entire load range by implementing adaptive, load-dependent control algorithms and/or adaptive dead-time control of switches [19]. In addition, with digital technology, customization of control, monitoring, protection, and house-keeping features of power converters

is shifted from hardware to software, which significantly shortens product design time, reduces the cost, and also allows for easy adjustment (tweaking) of parameters even after the product is deployed.

A. Architectures

Generally, power delivery systems of data processing and telecommunication equipment are built around two distinct architectures – centralized and distributed power architecture (DPA). At the system level, power delivery systems employed in data centers and telecom facilities are inherently distributed because of the distributed nature of the load. As illustrated in Fig. 4(a), DPA in datacenters uses ac-bus distribution, whereas telecom facilities use -48-V DPA with dc-bus distribution, as shown in Fig. 6.

At the equipment level, centralized power architecture (CPA) has been exclusively employed in cost-sensitive, low-to-medium power applications such as personal computers and workstations, whereas in high-power systems such as mainframe computers and high-end servers, as well as in networking equipment, dc-bus distributed power architecture (DPA) has been used. The major differences between these dc-bus DPAs is the voltage of the dc bus. Generally, to minimize the distribution losses, a higher dc-bus voltage is desirable at higher power levels. As a result, the DPA in mainframe computers that typically consume tens of kW of power is implemented with a high-voltage bus, typically, 350 V. Power systems of high-end servers whose power consumption is usually limited to several kW are implemented with either 48-V or 12-V dc-bus. Finally, the DPAs in networking equipment such as routers and modems use the 48-V dc bus.

As a result of continuously decreasing cost and improving performance of dc/dc converters,

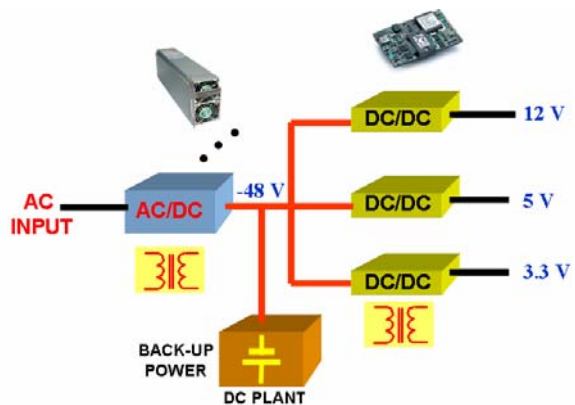


Fig. 6 Distributed power architecture (DPA) in telecom systems.

especially of the non-isolated, synchronous-buck, point-of-load (POL) converters, DPA has recently started to be employed in applications that in the past were exclusively implemented with multiple-output “silver box,” centralized power supplies such as low-end servers and high-end workstations. As the price and performance of POLs make further improvements and with emerging requirements for power management, it can be expected that DPA will soon find applications even in low-end equipment such , for example, desktop computers.

In addition, the availability of cost-effective POLs has been instrumental in the emergence of intermediate-bus architecture (IBA), shown in Fig. 7, that has been extensively employed in networking applications. In the IBA, the ac-line voltage is converted by an ac/dc front-end to a 48-V dc voltage that is then stepped-down by an isolated bus converter (BC) to a lower intermediate-bus voltage (IBV) in the range of 8-12 V. Finally, non-isolated POL regulators are used to convert the IBV to the desired load voltages. Generally, the IBV value, i.e, the step-down ratio of the BC, is determined so that the conversion efficiency of the power system is optimized. Since POLs offer the output voltage regulation, the IBV does not need to be tightly regulated, i.e., bus variations of $\pm 10\%$ are acceptable. As a result, the IBA can be implemented either with regulated or non-regulated BCs. Typically, BCs with non-regulated output, also known as dc/dc transformers, exhibit a slightly higher efficiency and lower cost compared to the efficiency and cost of their regulated counterparts.

It should be noted that in applications which do not use a 48-V battery back-up, or do not require a 48-V bus for any other reason, the IBA may not be the optimal architecture. Namely, in the IBA, the number of conversion stages is not minimal since power is processed by two cascaded isolated converters. As can be seen in Fig. 7, first the front-end converter dc/dc stage steps the 380-V output of the PFC down to 48 V and then this voltage is stepped down by BC to the final IBV value. However, by stepping the 380-V PFC output voltage directly to the desired IBV value

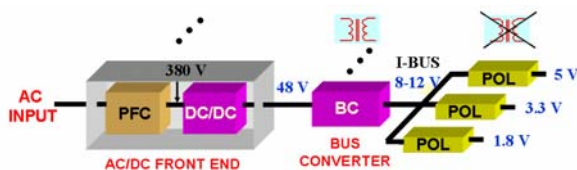


Fig. 7 Intermediate-bus architecture (IBA).

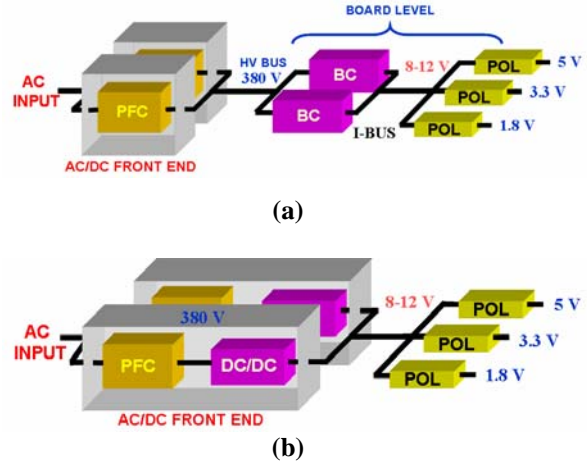


Fig. 8 AC/DC DPA system architectures with minimal number of conversion steps : (a) high-voltage (HV) distribution bus IBA; (b) low-voltage (LV) DPA

employing a high-voltage (HV) BC, the number of conversion stages can be minimized, as illustrated in Fig. 8. Depending on the system partition, i.e., whether the HV BC is left on the board or is incorporated in the front-end, the HV dc-bus IBA and low-voltage dc-bus (LV) DPA are obtained, as illustrated in Figs. 8(a) and (b), respectively. The minor performance difference between these two architectures are related to slightly different distribution losses. The vast majority of today’s servers supplied from single-phase ac lines employ the LV dc-bus architecture in Fig. 8(b).

To further improve the power conversion efficiency of datacom equipment, especially that of high-end equipment that typically requires relatively large power, the latest R&D work is focused on the evaluation of architectures with two LV dc buses [22]. The preliminary evaluation results suggest that this dual-bus architecture implemented with semi-regulated bus converters may offer better efficiency compared to that of the conventional single-bus implementation.

While improving the conversion efficiency at the equipment level by optimizing the power system architecture is certainly contributing to the lowering of power consumption in large data centers, even more dramatic energy savings may be possible to achieve by optimizing the power conversion and distribution systems of data center facilities. As shown in Fig. 4(a), large data centers employ redundant ac uninterruptible power supplies (UPSs) to provide uninterrupted service in case of power blackouts. On-line operation of UPSs are preferred over off-line operation because of a significantly better reliability. However, due to continuous power

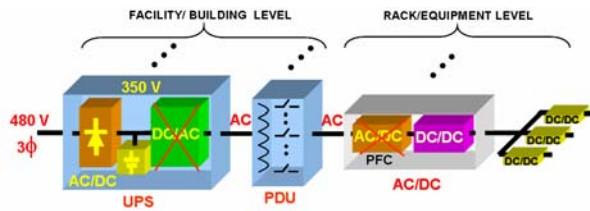


Fig. 9 Simplified block diagram of data center power conversion and delivery system.

processing, the on-line UPS back-up is less efficient than the off-line approach.

As shown in Fig. 9, the on-line AC-UPS backed-up power delivery system does not seem optimal since the number of conversion stages is not minimized. Specifically, the dc/ac conversion in the UPS followed by the ac/dc conversion in the PFC stage of equipment's ac/dc power supply certainly seem unnecessary. In fact, these two conversion stages can be eliminated by resorting to the HV dc-bus distribution shown in Fig. 10. This HV DC-UPS power system not only offers increased efficiency compared to that of the AC-UPS power system, but also exhibits much better reliability, which is comparable with that of the telecom -48-V dc-bus system. Finally, because ac/dc converters can also operate from a HV dc-bus, the HV dc-bus is a universal-current bus in the sense that it can accept both dc/dc and ac/dc powered equipment.

A number of HV dc-bus architecture implementations have been under consideration [23]-[31]. Generally, the implementations that use a non-isolated ac/dc stage [23]-[27], i.e., direct line rectification, exhibit higher conversion efficiencies compared to the implementations that employ isolated ac/dc front end to generate the HV bus [26]-[31]. However, the use of non-isolated rectifiers raises a number of concerns related to the safety of distributing high voltage around the data center so that isolated rectifiers seem more suitable for this application. Another major issue in the HV DC-UPS architecture that has yet to be completely resolved is related to

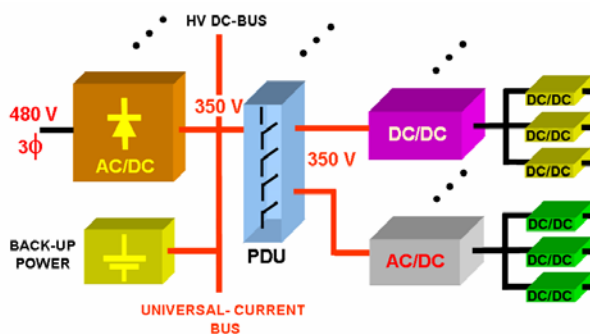


Fig. 10 High-voltage dc-bus data center power system.

the fault removal, specifically to the availability and performance of HV dc breakers that are required in HV dc-bus systems [23], [27], [30].

It has been demonstrated that the HV DC-UPS architecture offers a 5-15% power system efficiency improvement compared to that of the AC-UPS system, depending on the ac/dc front end implementation and the mix of dc and ac loads (equipment) [23], [27]-[28]. Including the cooling system power consumption, the electric energy savings of HV DC-UPS over the corresponding AC-UPS counterpart are in the 10-25% range. Because of higher efficiency and reduced heat dissipation, HV dc-bus architecture can improve the power conversion and delivery system power density by 20-30% , which allows for placement of more equipment in the existing data center facility.

B. Topologies

Ever since the introduction of switch-mode power supplies, major R&D effort has been dedicated to finding topologies that offer improved conversion efficiencies and power densities. With the introduction of the MOSFET switches that have enabled significantly higher switching frequencies compared to BJT devices, the topology investigation and design optimization had become one of the key areas for the advancement of switch-mode power conversion technology.

In the late seventies and early-to-mid eighties, the opportunity to significantly reduce the size of power converters by increasing the switching frequency created by steadily advancing MOSFET technology had focused topology development and optimization activities on the reduction of switching losses of the semiconductor devices, which were perceived as the major hindrance to maximizing the switching frequency of "hard"-switched pulse-width-modulated (PWM) converters. Generally, this extensive R&D effort was centered around resonant power conversion that eventually led to the development of new families of resonant converters such as zero-current-switching (ZCS) and zero-voltage-switching (ZVS) quasi-resonant (QR) and multi-resonant converters (MR), as well as class-E converters [31]-[35]. By 1988, power converter prototypes operating in the megahertz range and achieving power densities over 20 W/in³ were reported [36]-[37]. However, despite the initial keen interest in these technologies, the power supply industry has generally failed to cost-effectively incorporate these technologies in their products, except for the ZVS QR (variable-frequency CCM/DCM boundary) flyback

converter [38]. In fact, Vicor Corp., the company that did pioneering work in the development of ZCS QR technology, has been the only power supply manufacturer to offer a line of high-density dc/dc converters employing this technology [2].

The failure of high-frequency QR and MR technologies to seriously challenge the conventional PWM technology stems from the lack of clear performance advantage of QR and MR circuits. While the QR and MR power converters operate at much higher frequencies compared to their PWM counterparts and may use smaller magnetics, they may not exhibit better efficiencies because of increased conduction losses. Namely, very often in QR and MR converters the power loss savings due to ZCS and/or ZVS are more than offset by increased conduction losses in the semiconductor devices and magnetic components due to circulating currents introduced by the resonant-tank components and an increased copper resistance due to skin and proximity effects. Moreover, because of variable-frequency control, the performance deterioration of QR and MR converters is more pronounced in applications with a wide input-voltage range than in those with a narrow input-voltage range, i.e., the QR and MR technologies are more suitable for applications with relatively small or even no input voltage variations. In addition, variable-frequency operation of QR and MR converters is deemed less desirable by some power converter users than constant-frequency operation due to possible system-level interaction issues.

Nevertheless, the development of QR and MR converters has been an important milestone in the advancement of high-frequency switch-mode power supply technology because it resulted in a much better understanding of the effects of parasitics on switching losses. This knowledge has been key to the development of components with minimized parasitics that eventually led to significant performance improvements of conventional “hard”-switched PWM converters at higher switching frequencies.

Recognizing that increasing the switching frequency and power density must be done without performance degradation, the focus of R&D effort in the late eighties has shifted to finding topologies that offer a favorable trade-off between switching and conduction losses. Specifically, numerous topologies that combine the desirable features of square-wave PWM converters such as constant-frequency operation and minimal component stress and conduction

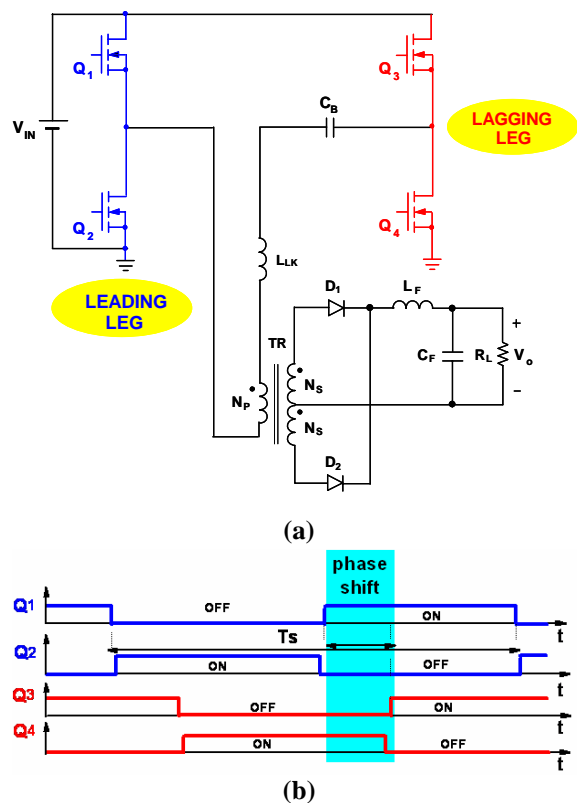


Fig. 11 FB ZVS PWM converter: (a) circuit diagram; (b) phase-shift control timing.

loss with soft-switching of resonant converters have been introduced [35]. The most prominent member among these topologies, known as soft-switched topologies, is the full-bridge (FB) ZVS PWM converter that employs constant-frequency phase-shift control [39]-[40]. This topology, shown in Fig. 11, has been extensively used in high-power server, telecom, and networking power supplies because of its excellent performance and scalability. Also, a number of soft-switched boost converters that are used in PFC implementations have found wide acceptance in commercial ac/dc power supplies [41]-[42]. The main feature of these boost converters is the reduction of reverse-recovery-related losses by soft switching of the boost rectifier [42]. However, since the introduction of silicon carbide (SiC) rectifiers that exhibit virtually no reverse-recovery charge, the employment of these soft-switching boost converters has been slowly declining.

Driven by today's extremely challenging requirements for simultaneous maximization of both the entire-load-range efficiency and power density, finding topologies that can operate at significantly higher switching frequencies and also achieve high efficiencies is the major focus of current topology optimization efforts. As a

result, resonant techniques are presently being revisited because advancements in semiconductor and magnetic devices, introduction of DPAs, changes in power supply specifications, and improved design optimization tools and knowledge are all making the resonant topologies more attractive now than ten-twenty years ago. For example, due to a relatively constant bus voltage in DPAs, the resonant converters are suitable for use in BCs, especially in unregulated BC (dc/dc transformer) implementations because of constant frequency operation. Currently, BCs employing the LLC resonant converter shown in Fig. 12 that operate in the megahertz range are available [43].

Similarly, the introduction of the PFC front end in ac/dc power supplies that serves as a pre-regulator to the output dc/dc stage has created favorable input-voltage conditions for application of resonant converters. As a result, the resonant technique, specifically, the LLC topology, has found application in high-density, high-efficiency notebook adapters and server power supplies [44]. Finally, the extensive use of synchronous rectifiers has also been a significant driving force in reviving the interest in resonant power conversion, in particular, in the LLC topology. Namely, the LLC topology offers ZCS of the secondary side rectifiers which is the preferred switching condition for the synchronous rectifier because it reduces/eliminates switching losses caused by the slow recovery characteristic of their body diode.

Another approach of getting power-density and performance benefits of increased switching frequencies without compromising the efficiency is the interleaving technique [45]-[48]. Generally, interleaving offers a size reduction of magnetic components and other performance benefits by processing power in a number of power-conversion stages that are connected in parallel and operate at lower frequencies, as shown in Fig. 13. By phase shifting (interleaving) the switching instances of the parallel modules, the apparent switching frequency of the converter increases as many times as the number of the interleaved modules. Besides the size reduction

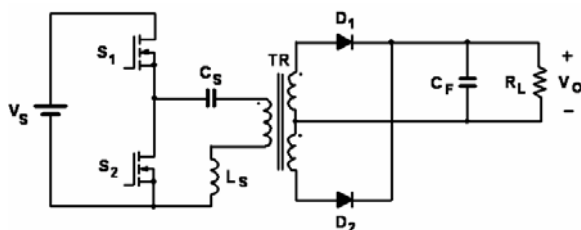


Fig. 12 LLC series-resonant converter.

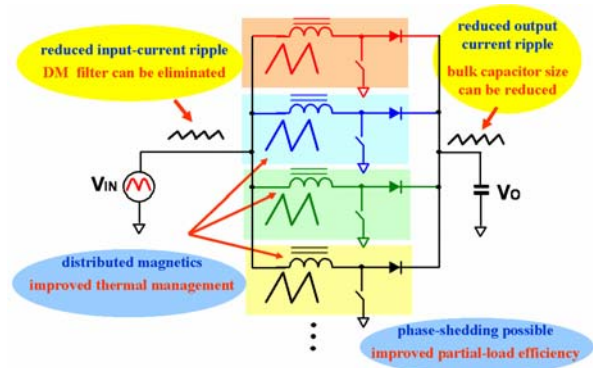


Fig. 13 Interleaving technique benefits.

of magnetic components, the interleaving technique offers reduced input current and output-filter capacitor current due to a ripple-cancellation effect, which reduces the size of the input filter and the number and size of output-filter capacitors. In addition, the interleaving technique makes it possible to implement the phase-shedding control algorithm that can improve a partial-load efficiency by progressively turning off phases of an interleaved converter as the load gets lighter.

The interleaving technique has been extensively used in VRM and POL applications [48]. In fact, the interleaved synchronous-buck converters are still the only approach that can deliver the required efficiency, power density, and transient-response performance required in VRM applications. In addition, in low-profile converters the interleaving approach is very often used because it distributes magnetic components and, consequently, enables smaller-size magnetic cores to be used. The interleaving technique is also gaining traction in the boost PFC front-end implementations. It is reasonable to expect that with the future broader employment of digital technology, which makes the implementation of the interleaving control much easier, the use of the interleaving technique will be increased.

Generally, one should not expect that future R&D work will turn up any new “miracle” topology with a superior performance over the existing circuits. Instead, the well known and established non-isolated and isolated topologies such as buck, boost, flyback, and various forward and bridge topologies and their variations will continue to be employed in an overwhelming majority of power supplies. However, due to the increasing use of synchronous rectifiers in low-output-voltage applications, the major future development effort will be dedicated to the implementation and performance optimization issues of synchronous rectifiers in these

topologies. Specifically, the lack of adequate synchronous-rectifier drivers is emerging as one of the major obstacles in further improvement of efficiency of high-frequency isolated power converters [49]-[50].

Finally, in ac/dc power supplies, the size of the energy-storage (bulk) capacitor and EMI filter are becoming major limitations to increasing the power density over 30 W/in^3 [42]. Moreover, in applications with a hold-up time requirement, there is a strong trade-off between the conversion efficiency and power density. As a result, minimization of the bulk-capacitor and EMI filter size will be one of the priorities of design engineers involved with ac/dc converters [51]-[52]. Finding solutions to increasing the energy utilization of bulk capacitors and minimizing their size without penalizing efficiency, as well as coming up with topology, layout, and component refinements to optimize the size of the EMI filter will be in the forefront of future R&D effort. As a result, active filtering techniques for reduction of common-mode EMI and hold-up time extension techniques for optimization of bulk capacitor size will be getting much more attention in the future [53]-[54].

C. Components and Materials

Generally, advancements in semiconductor technology have always been the major thrust behind efficiency and power density improvements in power conversion circuits. Specifically, the dramatic improvements in ac/dc power supply performance that have been achieved in the past decade or so have been primarily brought about by extraordinary reduction of the on-resistance of high-voltage MOSFETs and equally impressive improvements in reverse-recovery characteristics of high-voltage silicon (Si) rectifiers. As illustrated in Fig. 14, the super-junction technology has enabled a reduction of the on-resistance of 600-V today's MOSFETs down to $45 \text{ m}\Omega$, which is approximately ten times lower compared to the on-resistance of state-of-the-art 600-V devices available in the nineties [55]. Similarly, today's high-voltage Si rectifiers exhibit a significantly lower reverse-recovery charge, which has improved efficiency and simplified the design of the boost PFC front ends in ac/dc power supplies.

In applications with a low output voltage, further efficiency improvements has been made possible by continuous reduction of on-resistance of low-voltage MOSFETs that are

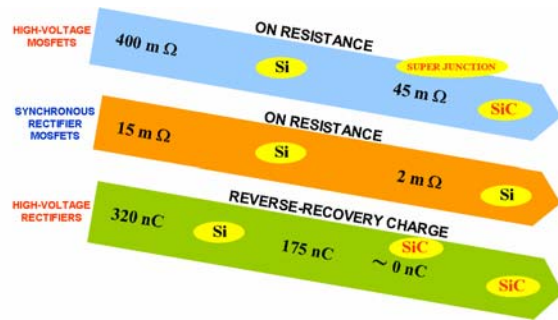


Fig. 14 Illustration of advancements of semiconductor technology.

used as synchronous rectifiers. Currently, the on-resistance of the state-of-the-art 20-30-V synchronous rectifiers is in the milliohm range, as shown in Fig. 14. Such a small on-resistance poses a serious packaging challenge since it requires a packaging technique that offers an ultra-low package resistance so that the package resistance does not significantly affect the total component resistance.

Future major improvements in high-voltage semiconductor components are expected to come from the silicon carbide (SiC) technology. In fact, the recently introduced high-voltage SiC Schottky rectifiers that exhibit no reverse-recovery charge characteristic has already demonstrated their superior performance in high-frequency front-end boost PFCs [56]-[58].

However, primarily due to a relatively high cost compared to that of their Si counterparts and also because of some lingering issues with their long-term reliability, the current acceptance of the SiC Schottky rectifiers is relatively low. Typically, it is limited to challenging high power density applications that require increased switching frequency and efficiency which cannot be achieved by conventional Si rectifiers. Recently, gallium nitride (GaN) Schottky rectifiers have been introduced as low-cost alternative to SiC Schottkies [59]. However, GaN technology still needs to be applied in commercially available power supplies.

The extensive employment of SiC technology can be expected once SiC MOSFET devices become available in the future. With SiC MOSFETs that are projected to have much lower terminal capacitances and the on-resistances of an order of magnitude lower than their Si counterparts, operation at much higher switching frequencies will be possible without efficiency degradation. This would allow for significant size reduction of magnetic components and further power density increases. The current design approach employed in PFC front-end boost

converters of pairing SiC rectifiers and super junction MOSFETs has generally failed to bring significant power density improvements because of efficiency degradation at higher switching frequencies caused by switching losses in super junction devices due to their increased terminal capacitances. With today's requirements for maximum efficiency driven by environmental and economic reasons, the standard design approach to performance optimization of ac/dc power supplies is to reduce the switching frequency. Since at low frequencies the performance of SiC rectifiers is marginally better than that of optimized fast-recovery Si rectifiers, the current usage of more expensive SiC rectifiers is limited to few applications where Si technology cannot deliver the required performance.

Generally, advancements in magnetic and capacitor technology have not kept the pace with the advancements in semiconductor technology. Essentially, no new power magnetic material for power transformers and inductors has been introduced in a long time [60]. The major effort of magnetics manufacturers has been focused on the optimization of the existing materials in certain frequency ranges and expanding the portfolio of core shapes and sizes, in particular low-profile planar cores. While improved magnetic materials would certainly help further optimization of power supply performance, the major fundamental obstacle in high-frequency magnetic components is the copper loss due to skin and proximity effects. In fact, these losses along with the switching losses of semiconductor devices are the major obstacle in increasing the switching frequencies much beyond their current ranges shown in Fig. 1. Unlike the switching losses of semiconductor devices that can be reduced and even virtually eliminated through circuit techniques such as ZVS and ZCS, the skin- and proximity-effect losses can only be minimized to a certain extent through winding optimization techniques.

Primarily driven by VRM requirements for smaller and better filter capacitors, low-voltage capacitor technology has made major advancements in the past decade [61]. The most notable improvements have been made in the area of multi layer ceramic (MLC) and solid electrolytic chip (POS) capacitors mainly by increasing their capacitance and reducing their equivalent-series resistance (ESR). However, no similar dramatic advancements have been seen in the high-voltage electrolytic capacitors used as energy-storage (bulk) capacitors. In fact, their volumetric efficiencies (capacitance/volume) are

not much better than that of a decade ago. As the size of bulk capacitors continues to emerge as a major limitation to increasing the power density in applications with a hold-up time requirement, the capacitor manufactures are expected to focus their future effort in improving the volumetric efficiency of high-voltage electrolytic capacitors.

D. Packaging

Advancements in the packaging technology and thermal management will be of paramount importance for future power-density improvements [62]-[63]. In fact, the packaging and thermal issues are already the major hindrance to attaining higher power densities.

Generally, packaging and thermal concerns need to be addressed at each and every level, i.e., from the component level to the board and power-supply box level all the way up to the system level. Of course, at different levels the optimization focus is on different packaging and thermal aspects. For example, while at the device level the focus is on the minimization of package parasitics and thermal impedance, at the system level it may be the power density and cooling efficiency.

Because of higher power levels, more stringent safety and EMI requirements, and cost pressure, packaging techniques employed in off-line ac/dc power supplies have always been different than those used in dc/dc converters, as illustrated in Fig. 15. Typically, ac/dc power supplies have been built with both through-hole and SMT components, conventional magnetics with a wire-wound windings, semiconductor devices in TO-220 and TO-247 packages mounted on heatsinks vertical to the main board, and electrolytic capacitors. On the other hand, dc/dc converter modules have typically been built with all SMT components, planar magnetics with integrated windings into the multilayer board, horizontally placed semiconductor components in small packages (SOIC, DPAK, and similar), and chip capacitors [64]. Furthermore, some of today's low-power POLs are already built using

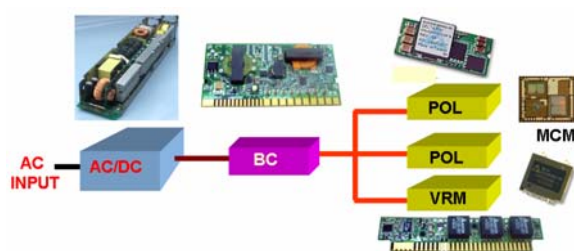


Fig. 15 Current packaging of ac/dc power supplies and dc/dc converters.

multi-chip-module (MCM) packaging techniques, as well as by employing monolithic integration of semiconductor components [65]-[66].

Component integration, both functional and physical, is emerging as one of the key packaging technologies. At the physical level, monolithic integration and/or chip co-packaging of semiconductor components such as switches, drivers, and control circuits is becoming increasingly employed [67]. This trend will certainly accelerate in the future as the available number of these integrated devices continue to grow. Similarly, the use of magnetics with integrated PCB winding(s) will find more extensive use in the future because this functional integration benefits power density [68]. Moreover, it is just a matter of time before advancement in packaging technology make integration of energy storage capacitors into the substrate/PCB a reality. This will certainly create new opportunities for power density improvements such, for example, the integration of the EMI filter [69]-[70].

In dc/dc converters the packaging optimization objective is to minimize the board area, especially the area taken by low power protection, monitoring, and control circuitry. This can be accomplished either by component integration or the employment of microcontrollers and the implementation of the functions in firmware. Once the board area is minimized, the packaging density may be further increased by resorting to 3D packaging by stacking of low-power passive or active components.

While package-on-package (PoP) approach may be used to implement 3D packaging and improve the power density at higher power levels, monolithic integration and/or power MEMS technology as the ultimate 3D packaging technologies are already employed in low-power

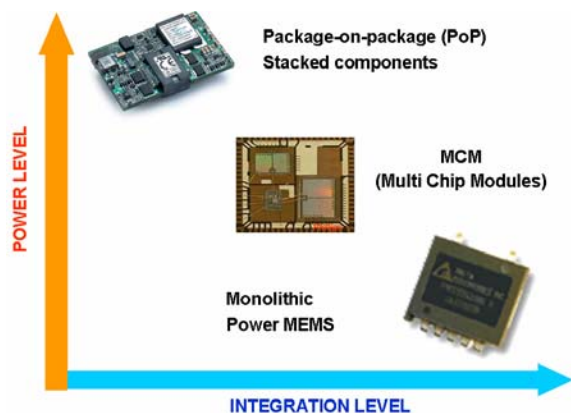


Fig. 16 Packaging integration level and power level relationship.

POLs [66]. In between these two power levels, MCM approach is emerging as a solution, as illustrated in Fig. 16. It can be expected that both MCM and monolithic integration will be applied at progressively higher power levels as these two packaging technologies are further improved.

In ac/dc power supplies the major objective of the packaging/thermal R&D effort is to improve the cooling efficiency. Namely, as the size of the power supply shrinks, the airflow impedance increases due to the increased volume utilization, i.e., due to the increased volume of the power supply taken by the components, as shown in Fig. 17. As the airflow impedance increases, if cooling efficiency is not increased, the fan speed must be increased, which also increases the acoustic noise. Therefore, the major challenge in packaging and thermal design at the box level is to increase the volume utilization without significantly affecting the acoustic noise performance.

Solving this extremely difficult challenge may require radically different placement of heat dissipating devices, preferably along the sides of the power supply box, as well as direct heat-sinking of magnetic component that will probably require the use of planar magnetic structures.

IV. SUMMARY

A sustained aggressive growth of the Internet infrastructure and a relatively low energy efficiency of power delivery systems of internet equipment along with a rising cost of energy and environmental concerns has brought the efficiency optimization across the entire load range into the forefront of today's datacom equipment performance requirements. This extremely challenging task further compounded by the ever-present requirement for higher power densities can only be met by future significant advances in the power supply technology. While

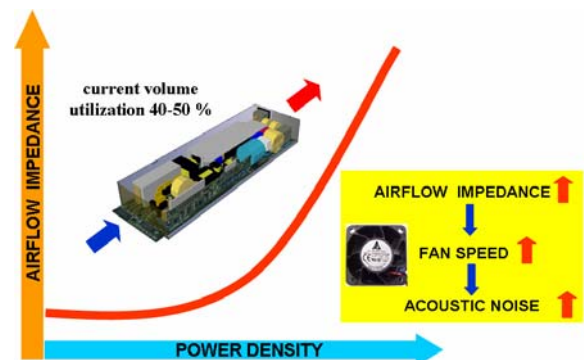


Fig. 17 Power supply airflow-impedance trend as function power density.

in the past, the major performance improvements had been primarily achieved by topology refinements and improvements in performance of semiconductor magnetic components, the future efficiency and power density improvements are expected to primarily come from system architecture optimization and power management, as well as from the advancements in packaging and thermal management techniques.

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