

DESIGN CONSIDERATIONS FOR FORWARD CONVERTER WITH SYNCHRONOUS RECTIFIERS

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Abstract – Design trade-offs and performance comparisons of different implementations of the forward converter with synchronous rectifiers are presented. Effects of the synchronous rectifier driving method on the conversion efficiency are evaluated. Specifically, the merits and limitations of the RCD-clamp and active-clamp reset approaches for the converter with self-driven synchronous rectifiers are discussed. Finally, experimental comparisons of efficiencies for an off-line, 3.3 V/20 A forward-converter power stage are presented.

1 Introduction

In a continuing effort to decrease power consumption and increase the speed of data-processing circuits, their power supply requirements are being reduced from 5 V to 3.3 V. The increased availability and use of 3.3 V logic ICs have spurred significant development and research efforts in the area of low-voltage power supplies. A number of approaches with different goals and levels of complexity have been taken in these designs. They range from simple dc/dc buck-converter add-on modules that convert outputs of existing power supplies to the required low voltage, to more sophisticated ac/dc converters with

synchronous rectifiers (SRs).

A number of SR implementations have been described so far [1] - [13]. Based on the method employed in driving SRs, all of them can be classified in two groups: control-driven and self-driven. In a control driven SR implementation, the SRs are driven by gate-drive signals derived from the gate-drive of the main switch. In a self-driven SR implementation, the SRs are driven directly with the secondary voltage of the transformer. As a result, the self-driven SR approach is very attractive since it is simple and requires a minimum number of components.

However, the performance of self-driven SRs is dependent on the resetting method of the power transformer since the freewheeling synchronous rectifier is driven by the reset voltage. Ideally, it would be desirable that the resetting time be equal to the off-time of the primary switch. Then the output current would freewheel through the SR for the entire off (freewheeling) time.

The objective of this paper is twofold. The first is to theoretically determine the limit of efficiency improvements that can be obtained from SRs. This limit is primarily a function of the output voltage, output current, on-resistance of the SR, and the forward-voltage drop of Schottky rectifiers replaced by SRs. The second objective is to compare conversion efficiencies of control-driven SRs with those of different self-driven SR implementa-

tions. Specifically, performance comparisons of the forward converter with RCD-clamp and active-clamp reset are performed.

2 SR Implementations

2.1 Forward converter with RCD clamp and self-driven SRs

The forward converter with self-driven SRs and key waveforms are shown in Fig. 1. In this circuit, synchronous rectifiers SR2 (Q_2 and D_2) and SR3 (Q_3 and D_3) are crosscoupled to the secondary winding of the transformer and are directly driven by the secondary voltage. Since no driver or control circuit is used to provide the gate-drive signals, this implementation of synchronous rectification is the simplest possible. However, its performance is strongly dependent on the method of the transformer core resetting, because the gate-drive signal for synchronous rectifier SR3 is derived from the reset voltage.

As can be seen from the waveform in Fig. 1(f), once the transformer reset is completed, the freewheeling current, which initially was flowing through transistor Q_3 , is diverted to body diode, D_3 , of SR3. Due to a relatively high forward-voltage drop of the body diode, the efficiency of synchronous rectification is reduced. The efficiency loss due to the body-diode conduction depends on the duration of the dead time (T_{dead}) and the forward-voltage drop of the diode (V_{BD}). This loss can be minimized by connecting a Schottky diode in parallel with SR3 or by minimizing the conduction time of D_3 . The conduction time of D_3 can be minimized either by driving Q_3 by an external gate-drive signal or by minimizing the dead time by employing a different reset scheme [13, 14]. The later method will be discussed in more detail in the following subsection.

The efficiency of synchronous rectifier SR2 is not dependent on the reset voltage since this rectifier is conducting during the on-time

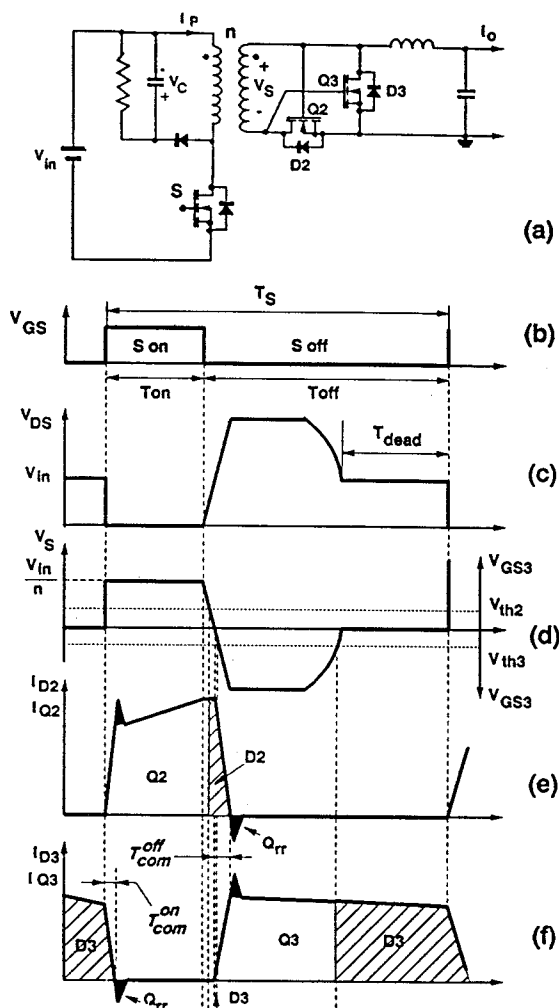


Fig. 1: Forward converter with RCD clamp and self-driven SRs: (a) circuit diagram; (b) gate-drive signal; (c) drain-to-source voltage of primary switch; (d) secondary winding voltage; (e) current through SR2; and (f) current through SR3.

of the switch. In fact, the body diode of SR2, D_2 , is conducting only during a brief period immediately after the primary switch is turned off. The conduction time of D_2 depends on the fall time of the secondary voltage (Fig. 1(d)) and the commutation time (T_{com}^{off}) of the output current from diode D_2 to transistor Q_3 . The commutation time is dependent on the secondary-side inductance that consists of the leakage inductance of the

transformer, the packaging inductance of SRs, and the secondary-side interconnect inductance. The secondary-side inductance also determines the commutation time (T_{com}^{on}) which is required to commutate current from diode D_3 to transistor Q_2 after the primary switch is turned on. To minimize the commutation times, the total inductance of the secondary side should be minimized. Moreover, it is especially important to make the leakage inductance of the transformer small relative to the other circuit inductances to avoid a loss of gate-drive voltage for SRs as explained in reference [9].

Finally, it should be noted that the conduction of the body diodes of SRs is not only increasing the conduction loss but also introducing the power loss due to their reverse recovery. This loss, which appears on the body diode and the transistor of the opposite SR during the diode turn-off, is proportional to the recovered charge Q_{rr} indicated in Figs. 1(e) and (f), frequency, and secondary voltage [16]. Therefore, it is relatively significant at full load and high line. The only method of eliminating this loss is to parallel the Schottky diodes to SR2 and SR3.

2.2 Forward converter with active clamp and self-driven SRs

The forward converter with active-clamp reset and its key waveforms are shown in Fig. 2. As can be seen, the active-clamp-reset approach minimizes the duration of the dead time since the transformer core is reset during almost the entire off-time of the primary switch [14]. As a result, the conduction time of transistor Q_3 is maximized, and consequently, the conversion efficiency is improved relative to the RCD-clamp counterpart. Also, the active-clamp reset approach minimizes voltage stress on the primary switch. In addition, the primary switch in this circuit can be turned on at zero voltage by properly adjusting the magnetizing inductance of the transformer [15]. However, the active clamp approach requires

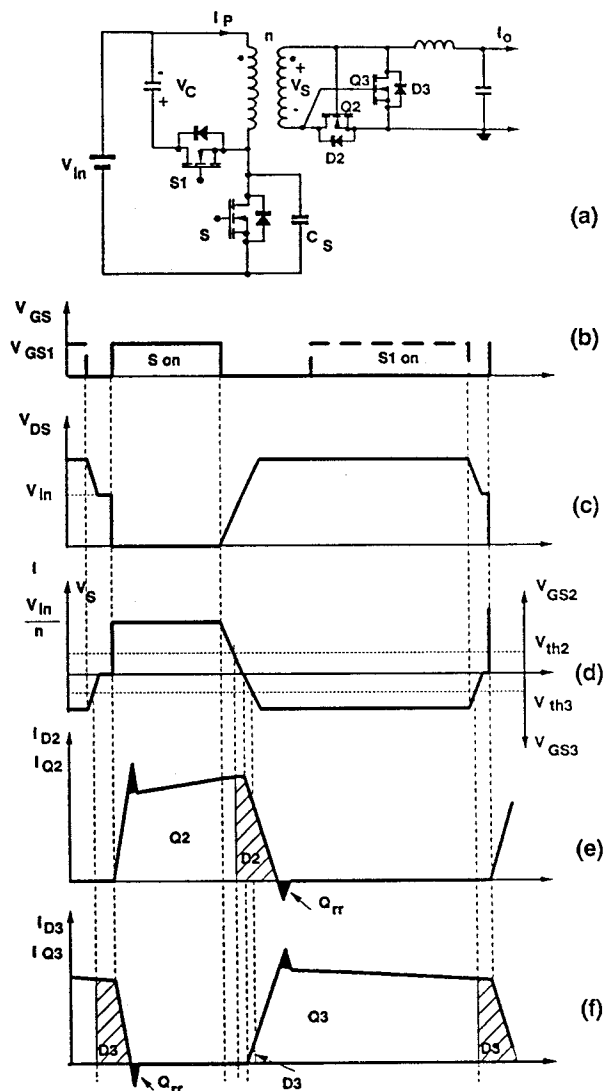


Fig. 2: Forward converter with active-clamp and self-driven SRs: (a) circuit diagram; (b) gate-drive signals; (c) drain-to-source voltage of primary switch; (d) secondary winding voltage; (e) current through SR2; and (f) current through SR3.

an extra switch and its associated gate drive, compared to the same circuit with the RCD-clamp reset. From this perspective, it is much simpler and more economical to use a Schottky diode in parallel with SR2 to improve the efficiency of the RCD-clamp circuit than it is to implement the active clamp. Therefore, the active-clamp approach is a viable choice in synchronous-rectifier applications where voltage stress and soft-switching are important

design considerations.

Generally, while self-driven SRs are simpler to implement, they are not suitable for applications with wide input-voltage variations. For the crosscoupled SRs shown in Figs. 1 and 2, the maximum feasible input-voltage range depends strongly on the output voltage. For higher output voltages, the input-voltage range is narrower. Namely, the gate-drive voltage of SR2 is proportional to the input voltage, and therefore, it varies in the same range as the input voltage. Also, the minimum secondary (*e.g.*, gate-drive) voltage that occurs at low line is dependent on the desired output voltage and the maximum duty cycle. If the input-voltage range is wide (*e.g.*, $> 3:1$) and if the output voltage is relatively high (*e.g.*, > 5 V), the gate-drive voltage at high line might exceed (or come close to) the maximum allowable gate-drive voltage. The effect of the output voltage on the amplitude of the gate-drive voltage can be eliminated by deriving the gate-drive signal for Q_2 from a separate winding with a smaller number of turns than the secondary winding. Also, the maximum gate-drive voltage can be limited by implementing a gate-to-source voltage-clamp circuit. However, all these modifications require additional components and/or a transformer with an increased number of windings, making the self-driven approach more complex. Therefore, the self-driven SRs are best suited for applications with a relatively narrow voltage range ($\leq 2:1$) and low output voltages.

2.3 Forward converter with control-driven SRs

The forward converter with control-driven SRs and its key waveforms are shown in Fig. 3. In this circuit, transistors Q_2 and Q_3 are driven by gate-drive signals derived from the primary-switch gate drive. As a result, the conduction times of the rectifiers are independent of the transformer-resetting method but solely depend on the timing of the gate-drive signals.

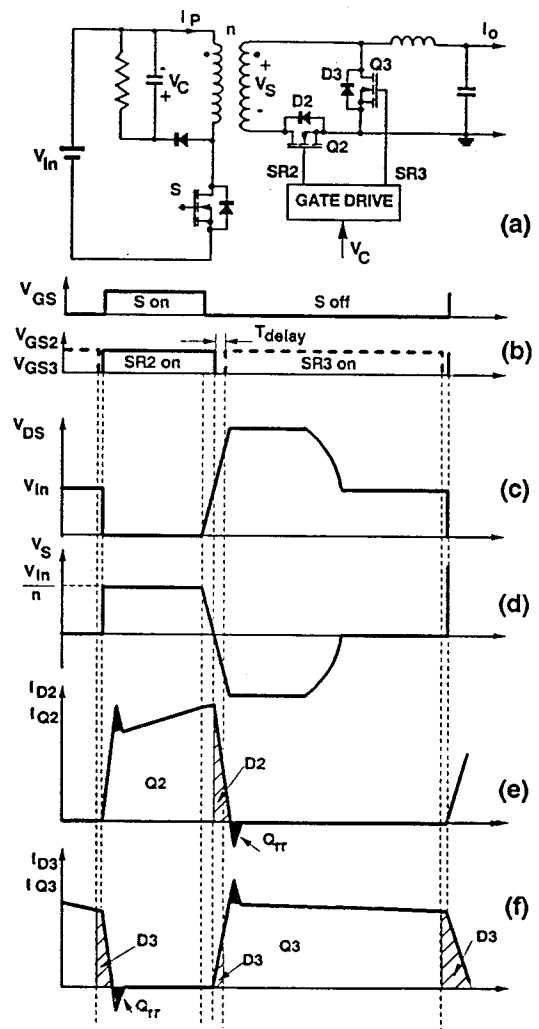


Fig. 3: Forward converter with control-driven SRs: (a) circuit diagram; (b) gate-drive signals; (c) drain-to-source voltage of primary switch; (d) secondary winding voltage; (e) current through SR2; and (f) current through SR3.

Ideally, the gate-drive timing should allow no conduction of the body diodes of the SRs. This is only possible with a very precise gate-drive timing where the gate-drive of one SR is applied or terminated at the same instant the gate-drive of the other SR is terminated or applied. In practical applications, this ideally complementary drive is not possible. Accidental, brief overlapping of the gate-drive signals that turn on both SRs simultaneously

would short the secondary causing an increased secondary current, and thus lower efficiency or in severe cases, cause converter failure. To avoid simultaneous conduction of SRs in practical applications, a delay between the gate-drive signals must be introduced. Since during the delay period no gate-drive signal is applied to the SRs, the body diodes of the SRs are conducting. This not only increases conduction loss but also introduces reverse-recovery loss. Therefore, the performance of control-driven SRs is strongly dependent on the timing of the gate drive.

3 Efficiency Limits of Synchronous Rectification

The efficiency improvement that can be achieved by replacing Schottky rectifiers with SRs is a complex function of many parameters. The most important are the output voltage, output current, SR on-resistance, forward-voltage drop of Schottkies that are being replaced by SRs, the transformer resetting method, efficiency of the converter with Schottkies, and implementation of SRs (*i.e.*, with or without Schottkies in parallel with SRs). A thorough estimation of losses in Schottky rectifiers and self-driven SRs and their comparisons for a specific application are presented in [9]. In this section, an estimate of overall efficiency improvements that can be achieved with different SRs implementations is presented.

Generally, the efficiency of a converter can be expressed as:

$$\eta = \frac{P_O}{P_O + P_{loss} + P_{REC}}, \quad (1)$$

where P_O is the output power, P_{loss} is the total loss excluding the rectifier loss, and P_{REC} is the rectifier loss.

For a converter with Schottky rectifiers, the efficiency is:

$$\eta_{SH} = \frac{P_O}{P_O + P_{loss} + P_{SH}}. \quad (2)$$

Similarly, for the same converter with SRs, the efficiency is:

$$\eta_{SR} = \frac{P_O}{P_O + P_{loss} + P_{SR}}. \quad (3)$$

Eliminating P_{loss} from the above equations, the efficiency of the converter with SRs (η_{SR}) can be expressed as a function of the efficiency of the converter with the Schottkies (η_{SH}):

$$\eta_{SR} = \frac{P_O}{P_O/\eta_{SH} - P_{SH} + P_{SR}}. \quad (4)$$

The power loss in the Schottky rectifiers can be calculated as:

$$P_{SH} = V_{SH}I_O, \quad (5)$$

where V_{SH} is the forward-voltage drop of the Schottkies, and I_O is the output current.

The power loss on the SRs is given by:

$$P_{SR} = R_{DS(on)} I_O^2(1 - D_{dead}) + V_D I_O D_{dead} + P_{gate} + P_{RREC}, \quad (6)$$

where $R_{DS(on)}$ is the on-resistance of SRs, $D_{dead} = T_{dead}/T_S$ is the dead-time duty cycle, V_D is the forward-voltage drop of the diode used to freewheel the output current during the dead time, P_{gate} is the gate-drive loss, and P_{RREC} is the power loss associated with the reverse-recovery of the body diodes of the SRs.

For control-driven and self-driven SRs with active-clamp reset, the dead time is very short relative to a switching period; and therefore, $D_{dead} \approx 0$. However, for the converter with the RCD-clamp reset and self-driven SRs this duty cycle usually cannot be neglected. In this case, the loss is dependent on the duration of the dead time and V_D of the diode that is used to freewheel the output current. Generally, this diode can be the body diode of SR3 ($V_D = V_{BD}$) or an externally added Schottky in parallel with SR3 ($V_D = V_{SH}$).

The gate-drive loss (P_{gate}) is a function of the gate-to-source voltage of SR, frequency, and gate charge required to charge SR's capacitances to the gate-source voltage [9]. A method of estimating this loss for self-driven SRs was presented in [9]. According to those calculations, for low frequencies (< 300 kHz), the gate drive loss for today's SRs is small (< 0.5 W) and for converters with an output power > 50 W can be neglected. For control-driven SRs this loss is higher since it includes also the loss in the external drivers and their associated logic.

The reverse-recovery loss (P_{RREC}) is only presented in implementations where the body diode of the SR is conducting (no Schottky in parallel with SR). Even when the body diode is conducting, this loss is relatively small at low frequencies (< 100 - 150 kHz).

When the gate-drive loss and the reverse-recovery losses are neglected ($P_{gate} = P_{RREC} \approx 0$), the efficiency of the forward converter with the SR implementations with $D_{dead} \approx 0$ (control-driven SRs and self-driven SRs with active-clamp reset) is:

$$\eta_{SR} = \left\{ \frac{1}{\eta_{SH}} - \frac{V_{SH}}{V_O} \left[1 - \frac{I_O R_{DS(on)}}{V_{SH}} \right] \right\}^{-1} \quad (7)$$

Similarly for the forward converter with SRs and RCD clamp ($D_{dead} \neq 0$), the efficiency is:

$$\eta_{SR} = \left\{ \frac{1}{\eta_{SH}} - \frac{V_{SH}}{V_O} \left[1 - \frac{I_O R_{DS(on)}}{V_{SH}} (1 - D_{dead}) - D_{dead} \frac{V_D}{V_{SH}} \right] \right\}^{-1} \quad (8)$$

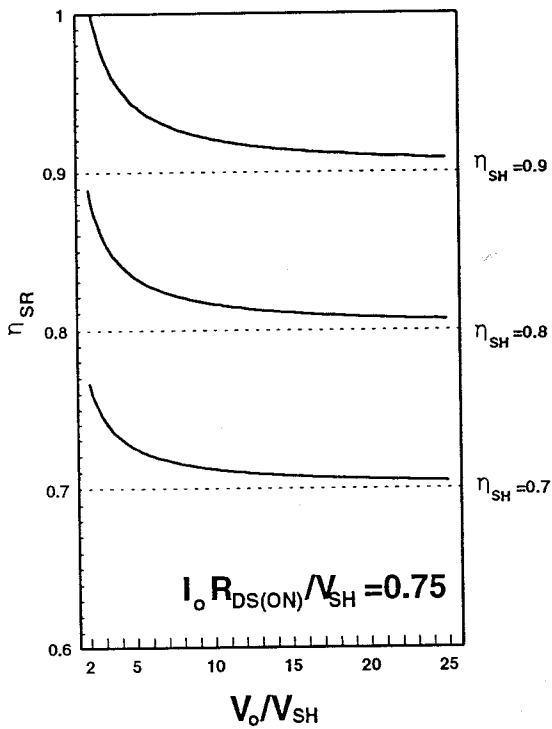
Equations (7) and (8) can be regarded as the best-case efficiency limits of different SR implementations. They are more accurate at low frequencies (< 300 kHz) where the gate-drive loss and the reverse-recovery loss are small.

Figure 4 shows plots of Eq. (7). These plots present the efficiency of a converter with

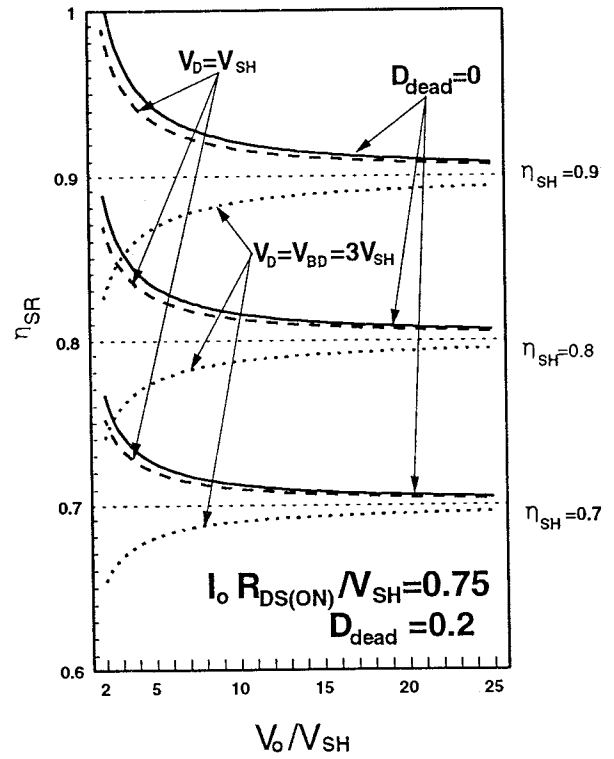
SRs (η_{SR}) as a function of the normalized output voltage (V_O/V_{SH}). The efficiency of the converter with Schottky rectifiers (η_{SH}) and $\alpha = I_O R_{DS(on)}/V_{SH}$ are the parameters. Parameter α represents the ratio of the forward-voltage drop of the SR at output current I_O to the forward-voltage drop of the Schottky. Obviously, α needs to be less than 1 to obtain an efficiency improvement when Schottkies are replaced by SRs.

As can be seen, the efficiency improvement for a given α and a given V_{SH} is lower at higher output voltages, V_O . Also, for the same output voltage, the efficiency gain achieved by synchronous rectification is higher for converters with higher efficiencies with Schottky diodes (η_{SH}), *i.e.*, for converters where the total loss is dominated by the loss in the Schottky rectifiers ($P_{SH} > P_{loss}$). Similarly, the efficiency improvement is larger for smaller α , *i.e.*, for better SRs (smaller on-resistance) or lower output currents. For example, for a converter with $V_O = 3.3$ V, $I_O = 20$ A, and the efficiency with Schottky rectifiers of $\eta_{SH} = 0.8$, assuming that $V_{SH} = 0.4$ V, $R_{DS(on)} = 15$ m Ω (*i.e.*, $\alpha = 0.75$ and $V_O/V_{SH} = 8.25$), it follows, from the plot in Fig. 4(a) that the best-case efficiency improvement is only 2%.

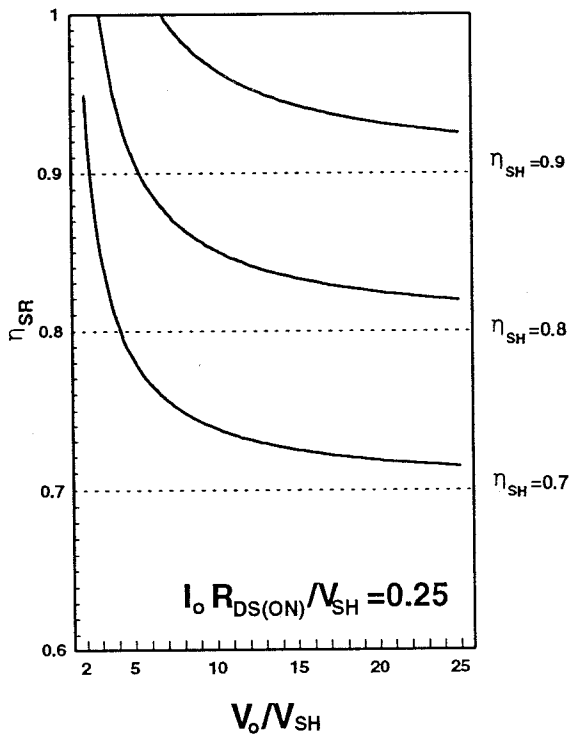
Figure 5 shows plots of Eq. (8) for $D_{dead} = 0.2$ for the SR implementation with a Schottky in parallel with SR3 ($V_D = V_{SH}$) and without a Schottky ($V_D = V_{BD} = 3V_{SH}$). Also, for reference, the curves for $D_{dead} = 0$ (Fig. 4) are shown. As can be seen, efficiency of the converter with the RCD-clamp reset is strongly dependent on the SR implementation. For the implementation with Schottky diodes the efficiency improvement is slightly lower than that of the control-driven SRs or self-driven SRs with an active-clamp reset. However, when the body diode of SR3 is used to freewheel the output current, the difference is very significant. In fact, under certain conditions the efficiency of synchronous rectification can be lower than that of Schottky diodes as illustrated in Fig. 5(a) for $V_D = V_{BD} = 3V_{SH}$.



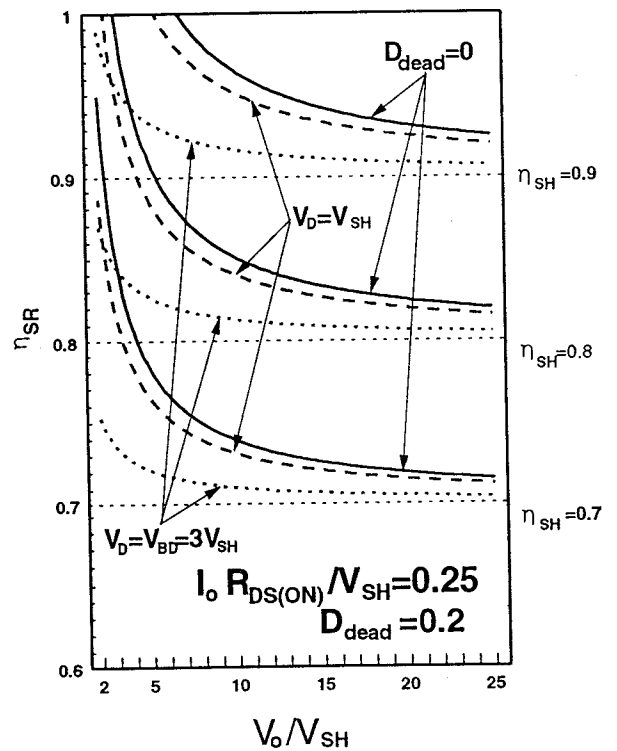
(a)



(a)



(b)



(b)

Fig. 4: Efficiency limits of forward converter with control-driven SRs or self-driven SRs and active-clamp reset: (a) $\alpha = R_{DS(on)} I_o / V_{SH} = 0.75$; and (b) $\alpha = 0.25$.

Fig. 5: Efficiency limits of forward converter with self-driven SRs and RCD-clamp reset for $D_{dead} = 0.2$: (a) $\alpha = R_{DS(on)} I_o / V_{SH} = 0.75$; and (b) $\alpha = 0.25$.

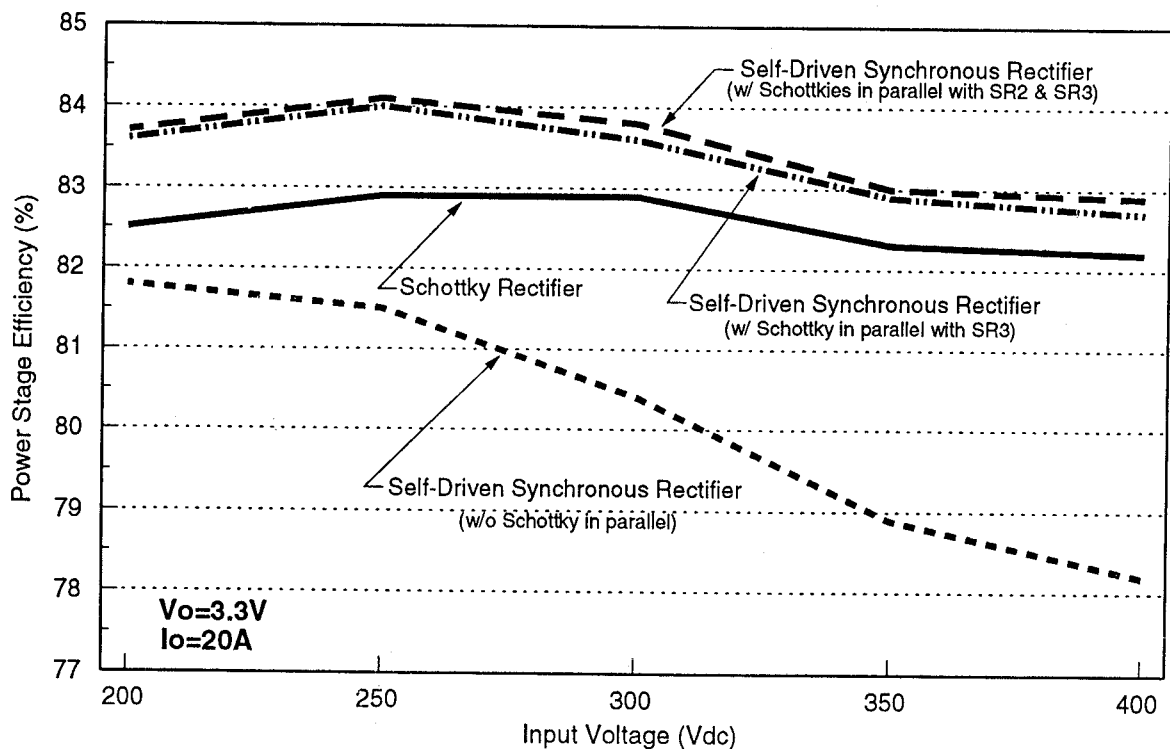


Fig. 6: Measured efficiency of forward-converter power stage with RCD-clamp reset and various self-driven SR implementations.

4 Evaluation Results

Evaluations of the discussed SR implementations were performed on an 100 kHz, 3.3 V/20 A forward-converter power stage designed to operate in the 200-400 Vdc input-voltage range.

Figure 6 shows the measured efficiency of the experimental converter with the RCD-clamp reset and self-driven SRs at full output current ($I_O = 20$ A) as a function of the input voltage. The efficiency of the converter with Schottky rectifiers is also shown for the reference.

As can be seen, the efficiency of the SR implementation without Schottky diodes connected in parallel with the SRs is lower than that of the converter with the Schottky rectifiers. As explained earlier, the efficiency loss is caused by the excessive power loss in the body diode of SR3 during the dead time. If a

Schottky diode in parallel with SR3 is used to freewheel the output current during the dead time, the efficiency of synchronous rectification is improved. It is 0.5-1% higher than that of the Schottky rectifiers. Also, from Fig. 6 it can be seen that the effect of a Schottky diode connected in parallel with SR2 is insignificant. It improves efficiency for less than 0.2%. This indicates that the conduction of the body diode of SR2 does not cause a significant power loss since the diode conducts for a very short time compared to the conduction time of Q_2 .

Figure 7 shows the measured efficiency of the experimental forward converter with active-clamp reset and the self-driven SRs. As can be seen, the efficiency of this converter with the Schottky rectifiers is approximately 1% (83.5% vs. 82.5%) higher compared to that of the converter with the RCD-clamp reset (Fig. 6). This is primarily due to a reduced

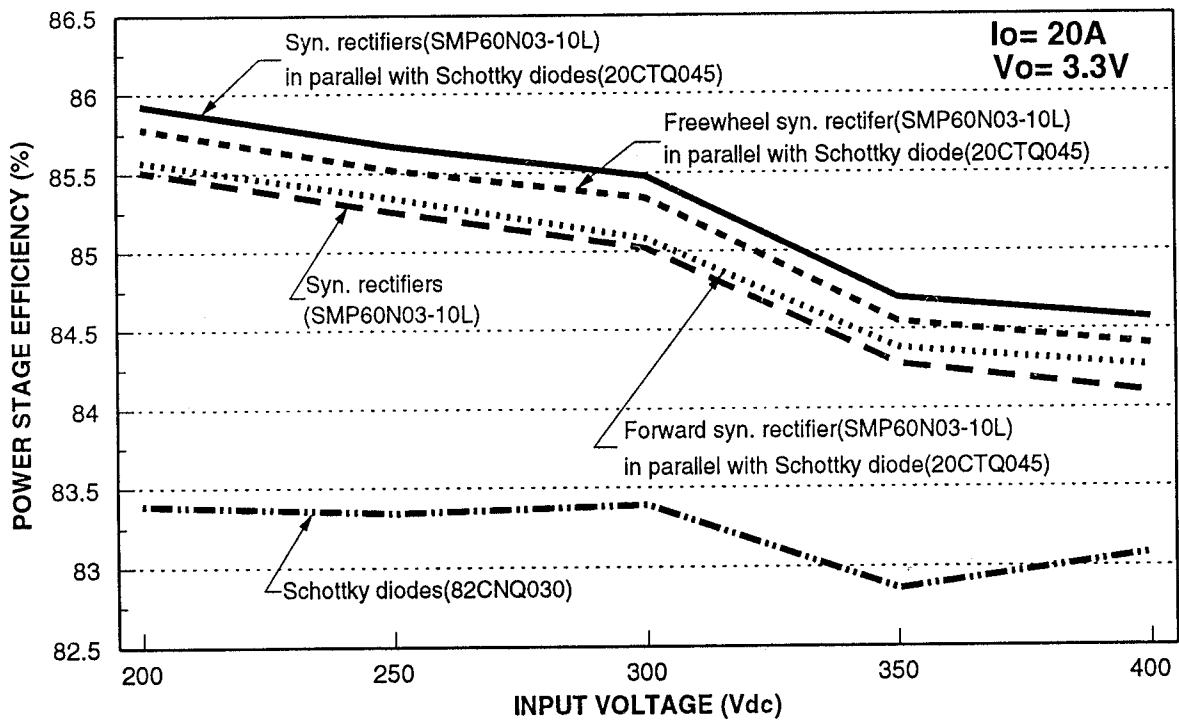


Fig. 7: Measured efficiency of forward-converter power stage with active-clamp reset and various self-driven SR implementations.

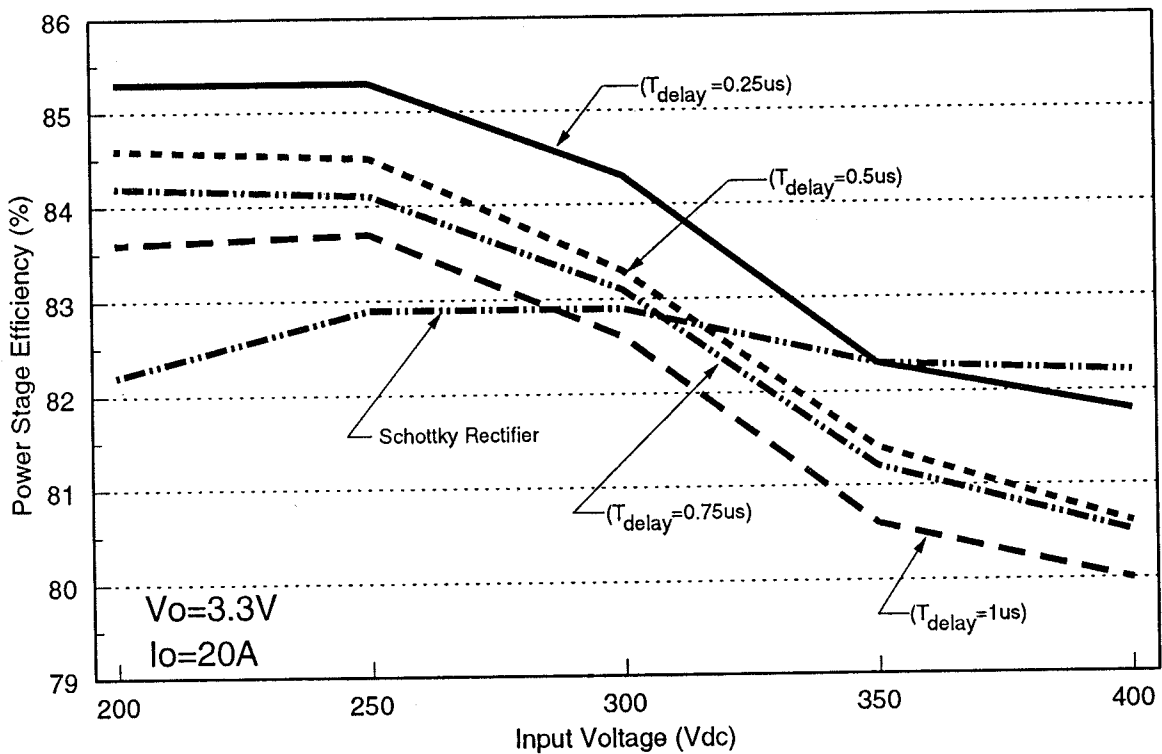


Fig. 8: Measured efficiency of forward-converter power stage with RCD-clamp reset and control-driven SRs with different delay times.

power loss on the primary side of the converter because of a higher maximum duty cycle, and consequently, higher turns ratio of the transformer. The achieved efficiency improvement by synchronous rectification is approximately 1-2% depending on the input voltage and SR implementation. However, the difference between the efficiencies of the SRs without and with Schottky diodes in parallel is less than 0.5% because the body diodes of the SRs are conducting for only short intervals.

Figure 8 shows the measured efficiency of the experimental forward converter with RCD-clamp reset and control-driven SRs for different delay times between the SR's gate-drive signals. As can be seen, the efficiency is very sensitive to the duration of the delay time. According to Fig. 8, the maximum efficiency improvement of around 3% is obtained at low line and for shortest delay time of 0.25 μ s. However, this figure does not take into account the power loss in the gate-drive circuits.

5 Summary

Different implementations of synchronous rectification in the forward-converter topology are discussed, and the effect of the transformer resetting mechanism on the performance of the self-driven synchronous rectifiers (SRs) is analyzed. An estimate of the upper limit of the efficiency improvement of synchronous rectification relative to the Schottky diode implementation is derived. The limit is a function of the output voltage, output current, on-resistance of SRs, forward-voltage drop of Schottkies that are being replaced with SRs, efficiency of the converter with Schottkies, and SR implementation. The discussed SR implementations are evaluated experimentally on a 3.3 V/20 A, off-line power stage. The achieved efficiency improvements for this application were, as predicted, relatively modest (1-2%).

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