

# DESIGN CONSIDERATIONS FOR LOW-VOLTAGE ON-BOARD DC/DC MODULES FOR NEXT GENERATIONS OF DATA PROCESSING CIRCUITS\*

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**Abstract:** By reducing the power supply voltage, a higher speed, lower power consumption, and higher integration density of data processing ICs can be achieved. Presently, a variety of ICs operating from 3.3 V are available. Next generations of ICs are expected to work even with lower voltages, i.e., in the 1-3 V range, to further enhance their speed-power performance. At the same time, during transients these new generations of data ICs will present very dynamic loads with high current slew rates. As a result, they will require point-of-load power supplies in order to minimize the effects of the interconnection parasitics. These on-board power supplies will be derived from the existing voltages available in the system (usually 5 V or 12 V), and will be required to have high power densities, high efficiencies, and good transient performance. This paper presents design considerations for these on-board power supplies and discusses their performance limits imposed by various circuit and system parasitics.

## I. Introduction

The ever-present demands for faster and more efficient data processing have prompted a significant development effort in the area of low-voltage ICs. Currently, 3.3-V ICs are gradually replacing the standard 5-V ICs due to their better speed/power-consumption performance and higher integration densities. However, the 3.3 V is only a transitional stage to ICs with even lower voltages that will not only further improve the speed and reduce the power consumption of ICs but also will enable a direct, single-cell battery operation. It is expected that next generations of the data processing ICs will require power supplies with voltages in the 1-3 V range. At the same time, these circuits are expected to be implemented with advanced power management functions to further reduce the power consumption in order to extend the battery-operation time in portable systems or to facilitate the compliance with various "energy star" ("green" power) requirements in office systems.

As the speed of the ICs increases, they are becoming more dynamic loads to their power supplies. Next generations of ICs are expected to exhibit current slew rates of 10 A/ $\mu$ s or even higher during transients. While these

slew rates do not pose significant problems for small load changes, they represent a major problem for large load changes that are usually encountered in systems with power management, when the system makes transition from the active mode to the sleep mode, and vice versa. In this case, parasitic impedance of the power supply connection to the load has a dramatic effect on the power supply voltage. If this impedance is not low enough, the supply voltage may fall out of the required range during the transients. To alleviate this problem, the power supply must be located next to the load (on-board conversion), and decoupling capacitors need to be connected across the load. However, no matter how close the power supply is placed to the load (e.g., a microprocessor), a certain amount of interconnect parasitics is always present. In addition, the amount of the decoupling capacitance (on-board capacitance) placed across the load (e.g., placed right across the microprocessor pins) is limited by the available space. As a result, the interconnect parasitics and the on-board capacitance values have a major effect on the performance of the dc/dc on-board converters [1].

The described dc/dc, on-board modules will be powered up from the voltages that already exist in the system and which are used for supplying other parts of the systems, for example, disk drives (12-V or 5-V) or the logic circuits operating from higher voltage (5-V). Since the board real estate is relatively expensive, the on-board converters have to have high-power densities and also have to operate with high efficiencies. These requirements, along with the limitations imposed by the high slew-rate of the load and a required tight load-regulation range, usually  $\pm 5\%$ , pose very serious design challenges.

In this paper, design considerations for dc/dc, on-board module performance optimizations are discussed. A thorough study of the effect of the interconnect parasitics as a function of the on-board capacitance value, load slew-rate, and voltage regulation range is presented. In addition, the selection guidelines for the switching frequency, input voltage, and control-loop bandwidth are defined.

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## II. Transient Load Analysis

A typical structure of a microprocessor power system is shown in Fig. 1. The processor, which is represented by a current source  $i_L$ , is powered up from a power supply with regulated output voltage  $V_o$ . To reduce the effect of the interconnect inductance  $L_{interc}$  between the output of the power supply and the processor, decoupling capacitance  $C_{decoup}$  is placed right across the processor power supply pins.

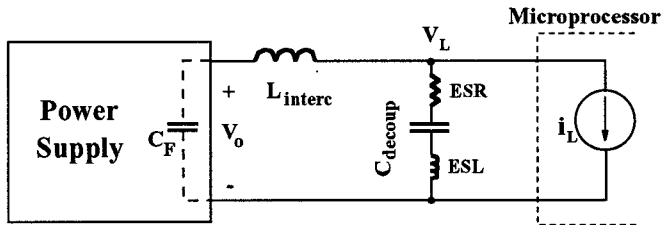


Fig. 1 Microprocessor power system structure.

The most dramatic load transients occur when the processor transition from the sleep mode to the active mode and vice versa, as illustrated in Fig. 2. In the sleep mode, the processor draws a relatively small current (typically  $\leq 1$  A), whereas it draws a substantially larger current when it operates in the active mode (typically  $\geq 10$  A). Moreover, the transition between the sleep and active modes occurs in a very short period of time, resulting in extremely high slew rates  $di_L/dt$ . According to some preliminary estimates, processor current slew rates are expected to be in the 10-A/ $\mu$ s to 100-A/ $\mu$ s range, for processors operating at around 100 MHz and above. Generally, faster current slew rates are expected in higher-speed processors that require lower supply voltages.

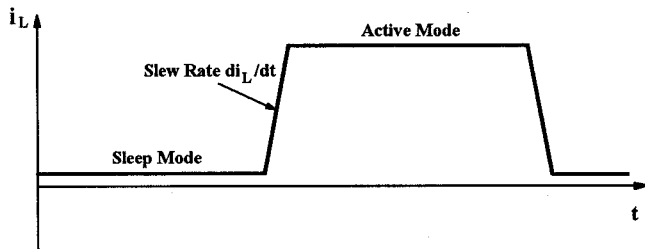


Fig. 2 Load waveform during transient.

In addition to high slew rates, the new generations of microprocessors will require a tight regulation of the output voltage, typically  $\pm 5\%$  or better. This output-voltage regulation spec will be also required to be met during the sleep-to-active mode (and vice versa) transients. Table I summarizes the output-voltage regulation ranges for different nominal output voltages and for output-voltage set accuracy of 0% (ideal) and  $\pm 1\%$ .

Table I

Calculated output-voltage regulation ranges  $\pm \Delta V_o$  for  $\pm 5\%$  regulation with 0% (ideal) and  $\pm 1\%$  output-voltage set accuracy

$V_o^{nom}$ [V]	$\pm \Delta V_o^{nom}$ [mV]	
	output-voltage set accuracy 0%	output-voltage set accuracy $\pm 1\%$
3.3	165	132
2.9	145	116
2.5	125	100
1.8	90	72
1.2	60	54

As can be seen from Table I, while the regulation band for the 3.3-V output with ideal output-voltage set accuracy, is  $\pm 165$  mV around the nominal voltage, it is only  $\pm 60$  mV for the 1.2-V output. For the output-voltage set accuracy of  $\pm 1\%$  the regulation band for 3.3-V output is reduced to 132 mV, whereas it is only  $\pm 54$  mV for the 1.2-V output.

Due to the high load-current slew rates and relatively narrow regulation ranges, the values of parasitic interconnect inductance  $L_{interc}$  and decoupling capacitance  $C_{decoup}$  have the decisive influence on the regulation performance of processor voltage  $V_L$  during transients. As illustrated in Fig. 3, for the 1.8-V output and 100-A/ $\mu$ s load-current slew rate from 1 A to 20 A, a relatively small inductance (3 nH) requires an extremely large decoupling capacitance (100  $\mu$ F) to keep the output voltage during the transients within the regulation spec. Since the decoupling capacitance needs to be as close as possible to the power-supply pins of the processor to minimize the inductance from the decoupling caps to the processor pins, the best arrangement is to place the decoupling caps in the processor-socket cavity [2]. However, the amount of capacitance that can be placed in the cavity is limited by the available cavity space. As a result, it is of the utmost importance to minimize interconnect inductance  $L_{interc}$  so that smaller decoupling capacitance can be used. The minimization of the interconnect inductance will be especially important for processor operating from lower voltages, not only because they would possess higher slew rates but also because they would generally draw more current. For example, 3.3-V processors require less than 10 A, while 1.2-V processors will very likely require more than 20 A.

To quantify the output-voltage deviation (i.e., the difference between the peak voltage during the transient and the nominal voltage as defined in Fig. 3)  $\Delta V_L$  during load transients as a function of interconnect inductance  $L_{interc}$ , decoupling capacitance  $C_{decoup}$  and its ESR and ESL, and the processor current slew rate, PSPICE simulations of the circuit in Fig. 1 were performed. In the simulations, it was assumed that the power supply output capacitance is large enough to be considered a constant voltage source. It should be noted that this approximation is valid only during a very

short period of time (i.e., several periods  $T_{res} = 2\pi\sqrt{L_{interc}C_{decoup}}$  of the  $L_{interc} - C_{decoup}$  resonant circuit), immediately after the load transition of the sleep-to-active or the active-to-sleep modes. The accuracy of this approximation and the time interval it holds are primarily dependent on the size of output-filter capacitor of the power stage  $C_F$ . Generally, for times longer than several  $T_{res}$ , the output-filter-capacitor voltage  $V_O$  cannot be considered constant because of a finite energy stored in  $C_F$ . In fact, when voltage  $V_O$  starts changing, the control loop of the power supply will respond so that the output voltage regulation is maintained with the new load current. Therefore, the transient response of  $V_O$  during the time after several  $T_{res}$  is mainly dependent on the power stage output filter ( $C_F, L_F$ ) characteristics and the control-loop dynamics. However, as will be discussed in the next section, for a properly designed power stage, voltage deviation  $\Delta V_L$  is determined by the initial voltage change immediately after the load-current transition which is governed by the  $L_{interc} - C_{decoup}$  response.

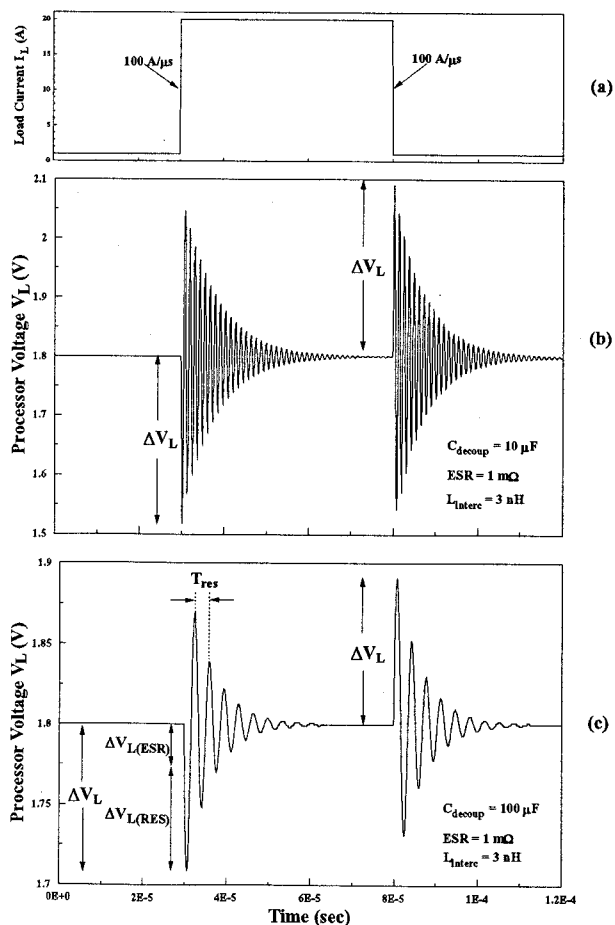


Fig. 3 Typical processor waveforms during transients:  
 (a) current transient;  
 (b) transient voltage over regulation specifications;  
 (c) transient voltage within regulation specifications.

Figure 4 shows the obtained output-voltage deviations during 20-A load transients with a load slew rate of 100 A/μs as functions of the interconnect inductance for decoupling capacitance ranging from 1 μF to 2000 μF, with ESRs of 1 mΩ (solid line) and 10 mΩ (dashed line), and with no ESL (ESL=0 nH). Figure 5 shows the similar plot for the 20-A load transient with a load slew rate of 10 A/μs. It should be noted that since the simulated circuit in Fig. 1 is linear, the output-voltage deviations for any other current steps can be also determined from plots in Figs. 4 and 5 by applying the proportionality principle. In addition, voltage deviation  $\Delta V_L$  caused by the output current change is independent of the nominal output voltage. Therefore, Figs. 4 and 5 are valid for any voltage level listed in Table I.

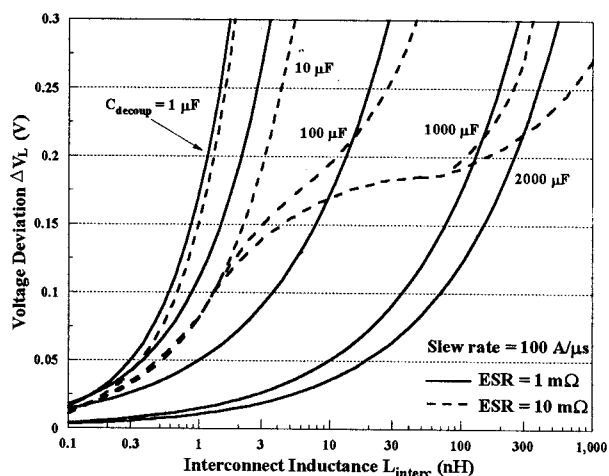


Fig. 4 Voltage deviation  $\Delta V_L$  as a function of interconnect inductance  $L_{interc}$  for slew rate = 100 A/μs,  $I_L = 20A$ , ESL = 0, ESR = 10 mΩ and 1 mΩ.

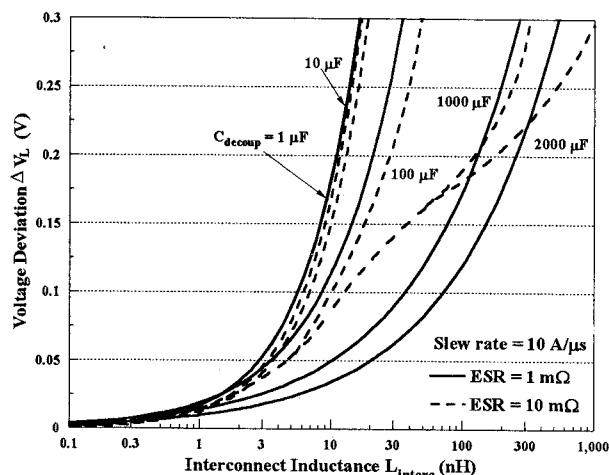


Fig. 5 Voltage deviation  $\Delta V_L$  as a function of interconnect inductance  $L_{interc}$  for slew rate = 10 A/μs,  $I_L = 20A$ , ESL = 0, ESR = 10 mΩ and 1 mΩ.

Generally, voltage deviation  $\Delta V_L$  during transients is caused by two factors. First, at the very beginning of a step

load transient, the load current step flows through decoupling capacitor  $C_{\text{decoup}}$  because a certain amount of time is needed to change the current through interconnect inductance  $L_{\text{interc}}$  to the new steady-state value. The step change in the decoupling capacitor current produces an initial voltage drop,  $\Delta V_{L(\text{ESR})}$ , on the ESR of the decoupling capacitor which is proportional to current step  $\Delta I_L$ , i.e.,

$$\Delta V_{L(\text{ESR})} = -\text{ESR} \cdot \Delta I_L \quad (1)$$

It should be noted that if  $\Delta I_L$  is positive (sleep-mode to active-mode transition),  $\Delta V_{L(\text{ESR})}$  is negative, and vice versa, as can be seen in Fig. 3.

After the initial voltage change due to the voltage drop on the ESR of the decoupling capacitor, the further change of the voltage is caused by the resonance between  $L_{\text{interc}}$  and  $C_{\text{decoup}}$ . The amplitude of this resonance is determined by the current step  $\Delta I_L$ , the values of  $L_{\text{interc}}$  and  $C_{\text{decoup}}$ , and the Q-factor of the  $L_{\text{interc}} - C_{\text{decoup}}$  circuit defined as

$$Q = \frac{1}{\text{ESR}} \sqrt{\frac{L_{\text{interc}}}{C_{\text{decoup}}}} \quad (2)$$

The total voltage deviation  $\Delta V_L$  is the sum of the initial voltage drop on the ESR,  $\Delta V_{L(\text{ESR})}$ , and the amplitude of the voltage resonance,  $\Delta V_{L(\text{RES})}$ , as indicated in Fig. 3. Since for a given decoupling capacitance (given  $C_{\text{decoup}}$  and ESR), smaller interconnect inductance  $L_{\text{interc}}$  results in lower Q-factors, the dominant component in the voltage deviation is the voltage drop on the ESR. As a result, for relatively small

$L_{\text{interc}}$ , the voltage deviations are smaller for smaller ESR of the decoupling capacitor. As can be seen from Figs. 4 and 5, for ESR=1 m $\Omega$  voltage deviations  $\Delta V_L$  are smaller than the corresponding deviations for ESR=10 m $\Omega$  (the dashed curves are above the solid curves). However, for larger values of  $L_{\text{interc}}$  (e.g., 10 nH for  $C_{\text{decoup}}=100 \mu\text{F}$  and  $>100 \text{ nH}$  for  $C_{\text{decoup}}>1000 \mu\text{F}$  in Fig. 4), the voltage deviations for ESR=10 m $\Omega$  are smaller compared to those for ESR=1 m $\Omega$  (the dashed curves are below the solid curves). Namely, for larger  $L_{\text{interc}}$ , the Q-factor increases to the point where the amplitude of the resonant component of  $\Delta V_L$  dominates the ESR-drop component.

The effect of the equivalent series inductance (ESL) of the decoupling capacitor is shown in Figs. 6 and 7. Figure 6 shows the effect of the 1-nH ESL, while Fig. 7 shows the same effect for an ESL of 5 nH. As can be seen from Figs. 6(a) and 7(a), the influence of small ESLs on the magnitude of  $\Delta V_L$  for the load-current slew rate of 10 A/ $\mu\text{s}$  is insignificant (the dashed and solid lines coincide or are close to each other). However, for the load-current slew rate of 100 A/ $\mu\text{s}$ , the effect of the ESL is much more pronounced, as can be inferred from Figs. 6(b) and 7(b). Moreover, for small decoupling capacitors ( $<10 \mu\text{F}$ ), the presence of the ESL reduces  $\Delta V_L$  (regions in Figs 6(b) and 7(b) where the dashed curves are above the solid curves). However, for  $C_{\text{decoup}} > 100 \mu\text{F}$ , the ESL significantly increases  $\Delta V_L$  (regions with the dashed curves below the solid curves).

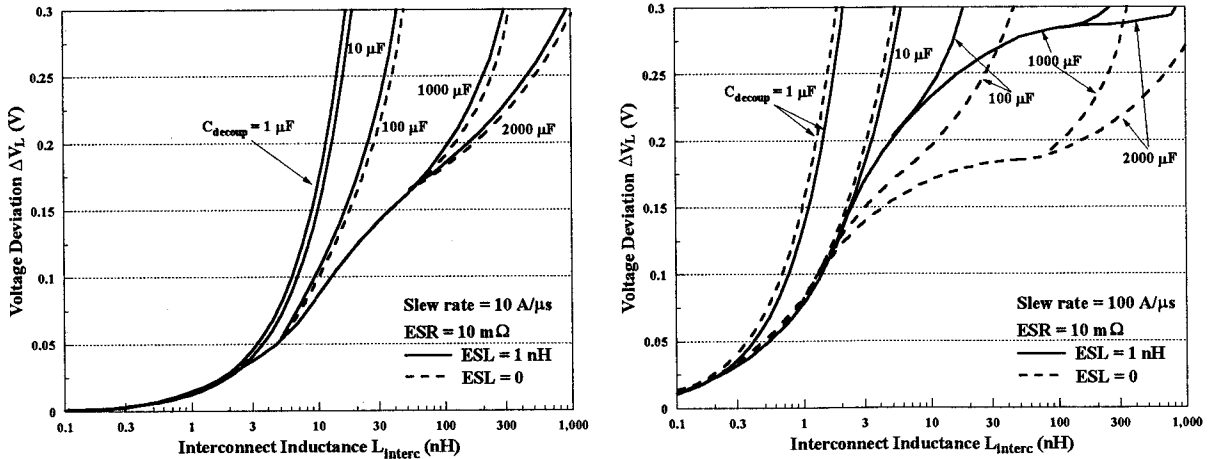


Fig. 6 Voltage deviation  $\Delta V_L$  as a function of interconnect inductance  $L_{\text{interc}}$  with ESL=0 nH (dashed lines) and ESL=1 nH (solid lines):  
 (a) slew rate = 10 A/ $\mu\text{s}$ , ESR=10 m $\Omega$ , and  $I_L=20 \text{ A}$ ;  
 (b) slew rate = 100 A/ $\mu\text{s}$ , ESR=10 m $\Omega$ , and  $I_L=20 \text{ A}$ .

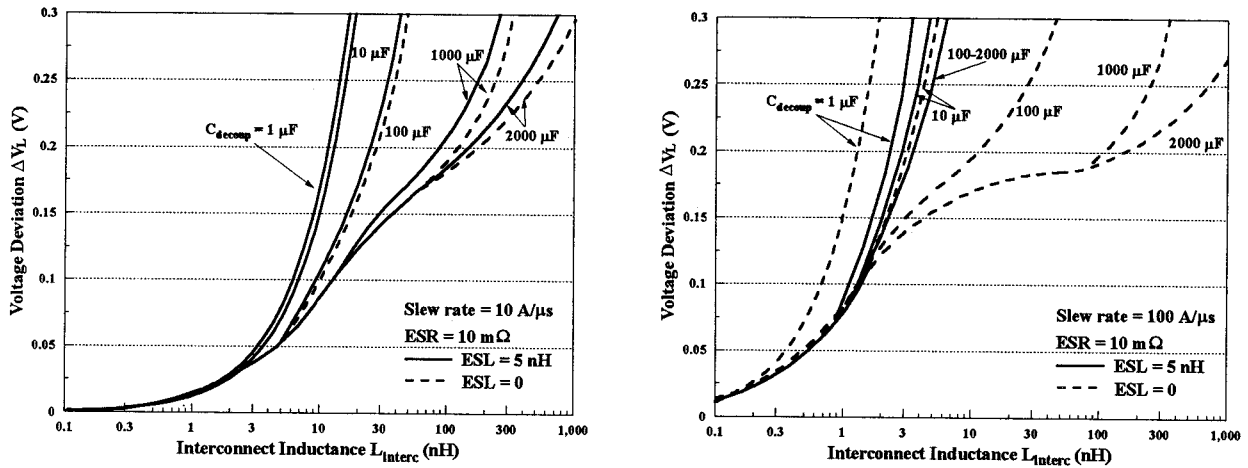


Fig. 7 Voltage deviation  $\Delta V_L$  as a function of interconnect inductance  $L_{interc}$  with  $ESL=0$  nH (dashed lines) and  $ESL=5$  nH (solid lines):  
 (a) slew rate = 10 A/ $\mu$ s,  $ESR=10$  m $\Omega$ , and  $I_L=20$  A;  
 (b) slew rate = 100 A/ $\mu$ s,  $ESR=10$  m $\Omega$ , and  $I_L=20$  A.

Table II

Estimated minimum interconnect inductance for different values of decoupling capacitance and load-current slew rates, assuming  $\pm 1\%$  output-voltage set accuracy, decoupling capacitance  $ESR=10$  m $\Omega$ , and  $ESL=1$  nH

$C_{decoup}$ [ $\mu$ H]	$L_{interc}^{max}$ [nH]									
	Slew Rate = 10 A/ $\mu$ s					Slew Rate = 100 A/ $\mu$ s				
	$V_L$ (V)					$V_L$ (V)				
	3.3	2.9	2.5	1.8	1.2	3.3	2.9	2.5	1.8	1.2
1	8.0	7.0	6.0	4.5	3.5	1.0	0.9	0.8	0.5	0.4
10	9.0	8.0	7.0	5.0	4.0	2.0	1.5	1.3	0.8	0.5
100	13	11	10	7.0	5.0	2.0	1.5	1.3	0.8	0.5
1,000	25	16	11	8.0	5.0	2.0	1.5	1.3	0.8	0.5
2,000	25	16	11	8.0	5.0	2.0	1.5	1.3	0.8	0.5

By combining the allowable regulation band from Table I with the data presented in Figs 6 and 7, the maximum interconnect inductance for given decoupling capacitance and output voltage and for given load-current transient slew rate can be determined. Table II summarizes the estimated values of  $L_{interc}^{max}$ , assuming  $\pm 1\%$  output-voltage set accuracy and decoupling capacitance with an  $ESR$  of 10 m $\Omega$ , and  $ESL$  of 1 nH.

As can be seen from Table II, for the current slew rate of 10 A/ $\mu$ s an interconnect inductance in the range of 5 nH (for 1.2-V output) to 25 nH (for 3.3-V output) is needed to keep the voltage deviations within the specifications even for a relatively large on-board capacitance of 2000  $\mu$ F. Because of the requirement for the extremely low interconnect inductance (note that 1 inch of wire typically has 10 to 20 nH of inductance, depending on the diameter), the multiple-output, centralized power supplies cannot be used to power up directly the next generations of microprocessor that possess high

current slew rates during load transients, since they usually use relatively long interconnect cables. The only viable approach is to use on-board power conversion which allows the placement of an on-board converter module next to the processor. While this approach can certainly work well with processors exhibiting current slew rates in the several tens of A/ $\mu$ s range, it may not be viable for the slew rates approaching and exceeding 100 A/ $\mu$ s. As can be seen from Table II, for the slew rate of 100 A/ $\mu$ s the maximum allowed interconnect inductance for  $C_{decoup}=2000$   $\mu$ F is below 2 nH for processors requiring 2.9 V or lower supply voltage. Because of the physical separation of the processor and the associated on-board converter, this low inductance is practically unattainable. The only solution to this problem might be the integration of the converter and the processor in the same package (in-package conversion) or even on the same silicon chip (on-chip conversion).

Generally, the interconnect inductance can be approximated as [3]

$$L_{interc} \approx \frac{2\mu_0 A}{w}, \quad (3)$$

where  $w$  is width of the connecting wire and  $A$  is the loop area formed by the connecting cable. Therefore, to minimize the parasitic interconnect inductance, it is necessary to use wide, short copper strip (foil) to connect the processor right next to the dc/dc module.

The voltage deviation  $\Delta V_L$  can be somewhat reduced by the conventional damping scheme shown in Fig. 8. The voltage waveform with damping is shown in Fig. 9. Compared with Fig. 3(b), it can be seen that the ringing of the voltage after the initial peak is significantly reduced, but the initial peak is almost unaffected. Thus, when dealing with high current slew rates, the only effective method of reducing  $\Delta V_L$  is to minimize the interconnect inductance.

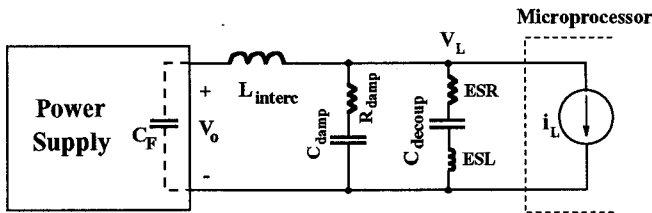


Fig. 8 Damping scheme.

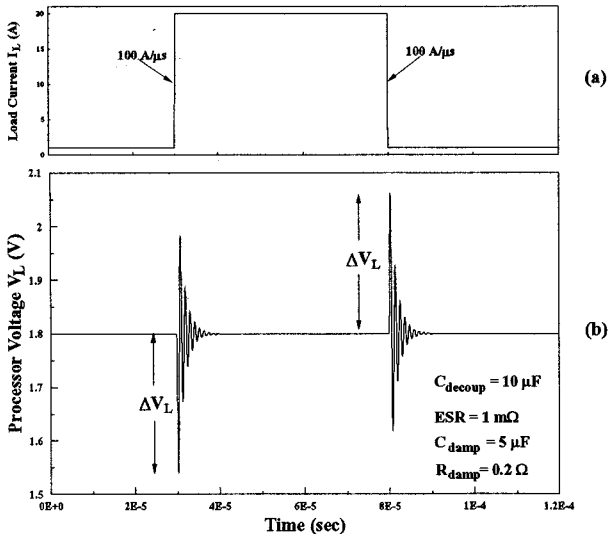


Fig. 9 Processor voltage waveform during transient with damping.  
(a) current transient;  
(b) transient voltage.

### III. Design Considerations for On-Board Modules

The block diagram of the typical complete power system for the next generations of computers is shown in Fig. 10. The dc/dc on-board module, which provides power to the

microprocessor, is supplied by one of the outputs of the off-line, multiple-output power supply that is used to provide power to disk drive(s) (12-V output) and data processing circuits that require 5-V supply. Since this power supply is connected to the motherboard by relatively long cables, its inductance  $L_{cab}$  is decoupled with capacitor  $C_{dec}$ . As explained in the previous section, interconnect inductance  $L_{interc}$  between the dc/dc modules and the microprocessor needs to be decoupled with capacitance  $C_{board}$  that is placed in the processor cavity. Note that  $C_{board}$  in Fig. 10 is the same capacitance as  $C_{decoup}$  in Fig. 1.

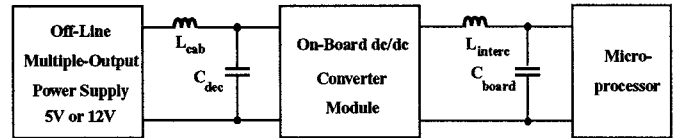


Fig. 10 Typical computer power system.

Since the galvanic isolation is provided by the transformer of the off-line power supply, the dc/dc on-board module does not need to be isolated. Consequently, the simplest, non-isolated step-down topology -- the buck converter -- can be used to implement the dc/dc on-board module. Because the motherboard real estate is relatively expensive, the area of the on-board module needs to be minimized. Generally, the required size, i.e., power density, can be achieved by increasing the switching frequency so the size of the filter components is reduced. With today's semiconductor and magnetic components, the optimum switching-frequency range is from 300 kHz to 1 MHz. At frequencies exceeding 1 MHz, the conversion efficiency may suffer due to excessive semiconductor losses (including gate-drive losses) and losses in the magnetic components (including the copper losses). If efficiency is not high enough, it may not be possible to package the converter in the desired size due to thermal problems.

It should be noted that high efficiency in the entire load range, i.e., from sleep mode to active mode, is also a requirement for the dc/dc on-board modules. While efficiency at full power (active mode) is required to achieve high power density because of reduced heat dissipation, at low power (sleep mode), high efficiency helps in meeting the EPA Energy Star requirements [4].

The circuit diagram of the buck converter power stage, along with the voltage-feedback control, is shown in Fig. 11. In addition, Fig. 12 shows the magnitude Bode plots of the power stage control-to-output small-signal transfer function, the error-amplifier (EA) transfer function, and the open loop gain. The positions of the poles and zeros of the EA compensation are determined such that the converter meets the desired stability and dynamics (bandwidth) specifications [5]. It should be noted that in practical designs the crossover frequency of the loop gain (which can be changed by the gain of the EA) is kept below approximately 1/5 of the switching frequency, although its theoretical limit is 1/2 of the switching

frequency. Also, the power stage dynamic is essentially that of the output filter.

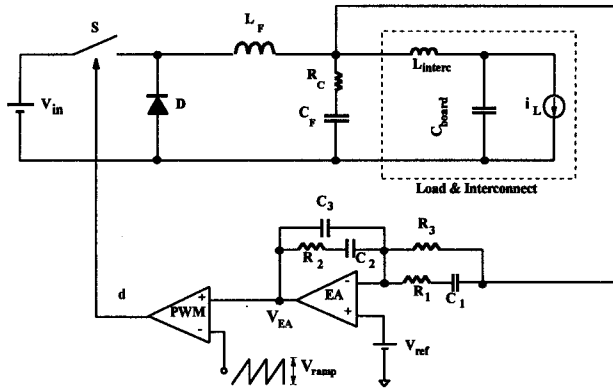


Fig. 11 Buck converter with voltage loop compensation.

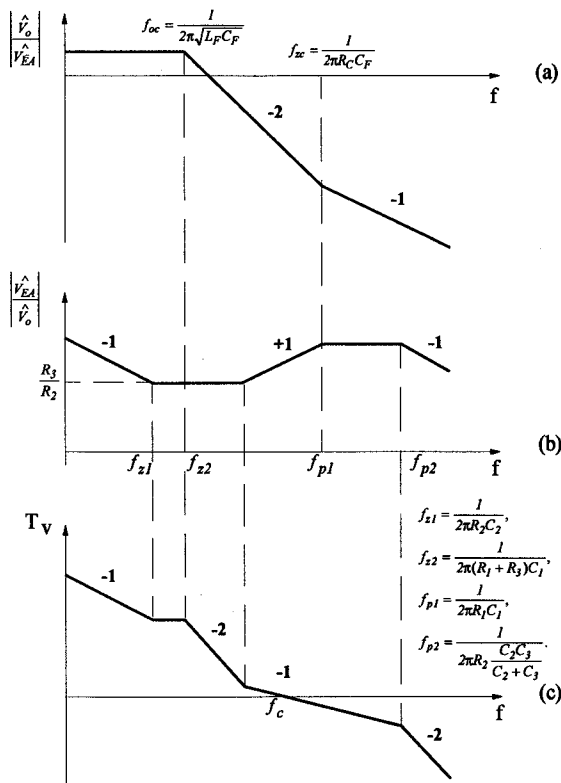


Fig. 12 Magnitude bode plots of transfer functions (a) power-stage control-to-transfer function; (b) error-amplifier transfer function; (c) loop gain.

As mentioned in the previous section, except for a very brief time interval right after the load current transition, the output voltage transient deviation is governed by the output-filter and the EA dynamics, i.e., the loop bandwidth. In addition, due to the damping in the resonant  $L_{interc} - C_{decoup}$  circuit, the influence of its parasitic oscillations on the  $V_L$  waveform diminishes after several resonant cycles, as shown in Fig. 9. As a result, it can be assumed that, except for the

initial voltage deviation  $\Delta V_L$ , for the most of the transient interval  $V_L$  behavior is determined by the converter characteristics, and not by  $L_{interc}$ .

For an ideal control with a dc high gain and the infinite loop bandwidth, the EA would respond to any change in the  $V_O$  caused by a load current change by instantaneously driving the EA output so that the duty cycle of the switch instantaneously changes to 100% (for the sleep-to-active mode transition) or to 0% (for the active-to-sleep mode transition). Therefore, if the initial voltage deviation  $\Delta V_L$  due to the  $L_{interc} - C_{decoup}$  circuit is neglected, and if an infinite bandwidth, high-gain EA is assumed, the converter during the sleep-to-active mode and the active-to-sleep mode transitions can be represented by the equivalent circuits in Figs. 13(a) and 13(b), respectively. As can be seen from Fig. 13(a), since the converter during the sleep-to-active mode transition operates with the maximum duty cycle (ideally  $D=1$ ), the input voltage is continuously applied to the output filter. Similarly, since during the active-to-sleep mode transition the switch is operating with a minimum duty cycle (ideally  $D=0$ ), the input voltage to the filter is zero (because diode D is conducting, as shown in Fig. 13(b)). Although the equivalent circuits in Fig. 13 are obtained by assuming an infinite bandwidth of the EA, they can also be used for finite-bandwidth as long as the duty cycle changes during the load-current transitions occur in a short time compared to the switching period, i.e., in one or two cycles. The criterion for estimating the minimum required bandwidth is defined in the next section.

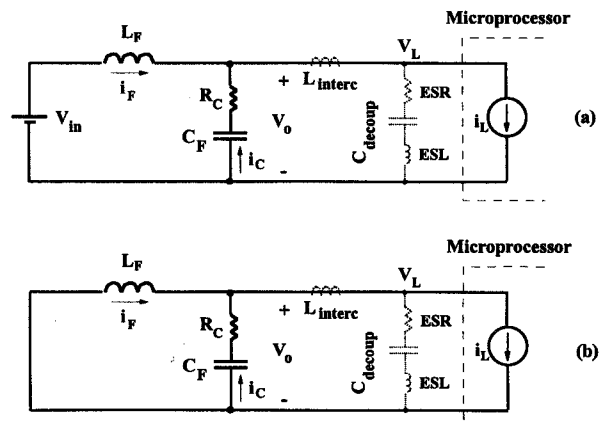


Fig. 13 Equivalent circuits of the converter with infinite bandwidth during load current transients: (a) sleep-to-active mode ( $D=1$ ); (b) active-to-sleep mode ( $D=0$ ).

Note that due to damping, resonant circuit consisting of  $L_{interc}$  and  $C_{board}$  does not affect transient response after several periods  $T_{res}$ , and therefore can be neglected (left out from the circuit).

Equivalent circuits in Fig. 13 can be used to estimate the approximate minimum capacitance which is required to keep the transient output voltage within the specified regulation limits. For example, according to Fig. 13(a), for the load step-

up transient the output current has to be initially drawn from the output capacitor  $C_F$  because the inductor current cannot be charged as fast as the load current changes, as shown in Fig. 14.

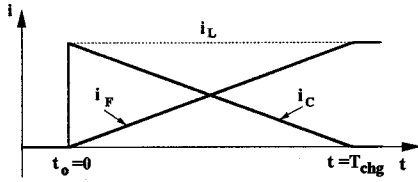


Fig. 14 Current response waveforms during step-up transient.

Since the output voltage variation is very small (<5%), the inductor current charging slope is

$$\frac{di_F}{dt} \approx \frac{V_{in} - V_L}{L_F}, \quad (4)$$

where  $L_F$  is determined by current ripple spec  $\Delta I_F$ , i.e.,

$$L_F = \frac{V_L(1-D)T_s}{\Delta I_F}. \quad (5)$$

The charging time  $T_{chg}$  required for the output-filter inductor current to ramp up from 0 to  $I_L$  is

$$T_{chg} = I_L / \left(\frac{di_F}{dt}\right). \quad (6)$$

Therefore, the capacitor voltage droop due to the discharging is given by

$$\Delta V_C = \frac{1}{C_F} \int_0^{T_{chg}} i_C dt = \frac{I_L T_{chg}}{2C_F}. \quad (7)$$

From Eqs. (4) - (7), to keep the voltage droop within regulation spec  $\Delta V_{L(spec)}$ , the minimum required output-filter capacitance is

$$C_F > \frac{I_L^2}{2\Delta I_F \Delta V_L f_s} D. \quad (8)$$

Similar derivation can be used to estimate the minimum required output-filter capacitance to keep the voltage change during the step-down transient within the regulation band. Considering both situations, the required minimum output-filter capacitance is

$$C_F > \frac{I_L^2}{2\Delta I_F \Delta V_L f_s} \max(D, 1-D). \quad (9)$$

Therefore, 50% duty-cycle gives the smallest possible capacitance for given specifications. Figure 15, generated from Eq. (9), clearly shows that 5 V input requires less capacitance because its duty-cycle is closer to 50%. In fact, for a given output voltage  $V_O$  and a given output-filter-inductor current ripple  $\Delta I_F$ , a smaller inductance  $L_F$  is needed

for a lower input voltage  $V_{in}$ . Since the current change in a smaller inductance is faster, the charging and discharging times of the inductor are faster, requiring a smaller output-filter capacitance to keep the output voltage within the regulation spec.

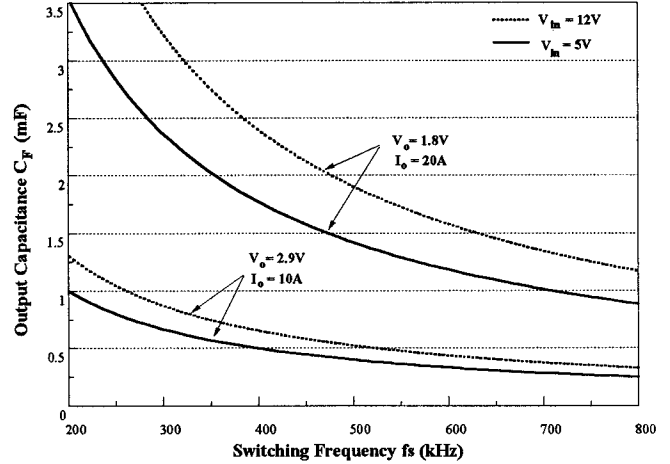


Fig. 15 Calculated minimum required output-filter capacitance as function of switching frequency for  $\Delta I_F = 10\% I_L$  and  $\Delta V_L = 5\% V_L$ .

#### IV. Simulation Verification

To verify the design curves given in Figs. 4, 5, 6, 7, and 15, and to establish a criterion for the control-loop bandwidth selection, a number of PSPICE simulations were performed. The simulation results for a 1.8 V/20 A on-board converter supplying a processor with the 25 A/ $\mu$ s current slew rate are presented in Figs. 16 through 18, while the circuit parameters and component values used in the simulations are listed in Table III. These closed-loop simulations were performed at two switching frequencies, i.e., 300 kHz and 750 kHz, and for various bandwidths of the voltage control loop, assuming a 10% output-filter-inductor current ripple and the minimum output-filter capacitance calculated from Eq. (9).

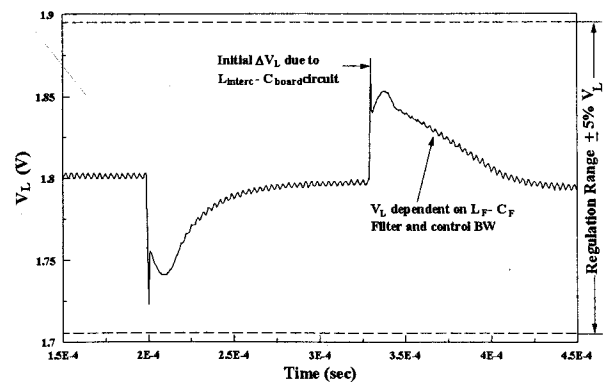


Fig. 16 Typical transient-voltage waveform of processor during load-current transitions shown in Fig. 2.

Figure 16 shows the typical processor voltage waveform during transients similar to that of Fig. 2. As indicated in the figure, the initial voltage deviation  $\Delta V_L$ , that also determines the maximum voltage deviation, is caused by the interaction of parasitic interconnect inductance  $L_{\text{interc}}$  and board capacitance  $C_{\text{board}}$ . After this initial deviation, the transient response is governed by the power stage parameters ( $L_F$  and  $C_F$ ) and the bandwidth of the control loop. Also indicated in Fig. 16 is the  $\pm 5\%$   $V_L$  ( $\pm 90$  mV) voltage-regulation band which assumes the ideal voltage-set accuracy (Table I).

Table III  
Circuit parameters and component values used in PSPICE simulations

	$f_s=300$ kHz			$f_s=750$ kHz	
	$0.1f_s$	$0.3f_s$	$0.05f_s$	$0.1f_s$	$0.1f_s$
$f_c$	5	5	5	5	5
$V_{\text{in}}$ [V]	5	5	5	5	5
$V_o$ [V]	1.8	1.8	1.8	1.8	1.8
$I_L$ [A]	20	20	20	20	20
$\Delta I_F$ [A]	2	2	2	2	2
$di_L/dt$ [A/ $\mu$ s]	25	25	25	25	25
$L_F$ [ $\mu$ H]	1.92	1.92	1.92	0.786	0.786
$C_F$ [mF]	2.5	2.5	2.5	1	1
$R_C$ [m $\Omega$ ]	2	2	2	2	2
$L_{\text{interc}}$ [nH]	2	2	2	2	2
$C_{\text{board}}$ [ $\mu$ F]	100	100	100	100	100
ESR [m $\Omega$ ]	10	10	10	10	10
ESL [nH]	1	1	1	1	1
$C_1$ [nF]	1.9	1.9	1.9	0.76	0.76
$R_1$ [k $\Omega$ ]	2.6	2.6	2.6	2.5	2.5
$C_2$ [nF]	0.94	0.31	4.7	1.2	1.2
$R_2$ [k $\Omega$ ]	170	510	34	65	65
$C_3$ [pF]	6.2	2.1	31	6.5	6.5
$R_3$ [k $\Omega$ ]	10	10	10	10	10
$V_{\text{ramp}}$ [V]	1.8	1.8	1.8	1.8	1.8
EA $SR_{\text{max}}$ [A/ $\mu$ s]	0.25	0.25	0.25	0.25	1.2

Figure 17 shows the simulated transient voltage waveforms of a processor supplied by an on-board converter operating at 300 kHz with different crossover frequencies of the control loop. As can be seen from Figs. 17(a) and 17(b), there is no noticeable difference between the transient responses for the control-loop bandwidths of  $f_c=0.1f_s=30$  kHz (Fig. 17(a)) and  $f_c=0.3f_s=90$  kHz (Fig. 17(b)). Both loop bandwidths are sufficient to keep the transient voltage within the regulation band with the minimum output-filter capacitance of 2.5  $\mu$ F. The transient voltage waveforms are not affected by the loop bandwidth because for both bandwidths the change of the EA output voltage is slew-rate limited due to the relatively large EA gains necessary to achieve these control-loop bandwidths. Namely, because minimum  $C_F$  is determined from the transient voltage considerations (Eq. (9)) and not from the output-voltage ripple considerations, the value of  $C_F$  is much larger than in conventional designs. As a result, the power stage filter

frequency ( $f_{oc}$  in Fig. 12(a)) is very low. Therefore, to obtain a relatively modest crossover frequency, e.g.,  $f_c=0.1f_s$ , the gain of the EA has to be high to make up for the power stage attenuation. Due to a high gain, the EA output is slew-rate limited even for relatively small voltage differences (errors) at the EA inputs [6].

However, as shown in Fig. 17(c), if the bandwidth of the loop is reduced too much, e.g.,  $f_c=0.05f_s=6$  kHz, the transient voltage response is too slow to keep the voltage within the specified range. In this case, the reduction of the control-loop bandwidth requires that the EA gain and, therefore the EA bandwidth, be reduced to the point where the rate of change of the EA output voltage is not limited by the EA slew-rate, but rather by its low bandwidth. As a result, the output of the EA, and consequently the duty cycle of the switch requires too many cycles to change to the extreme ( $D=1$ ) causing the output-filter capacitor voltage to fall below the regulation range limits.

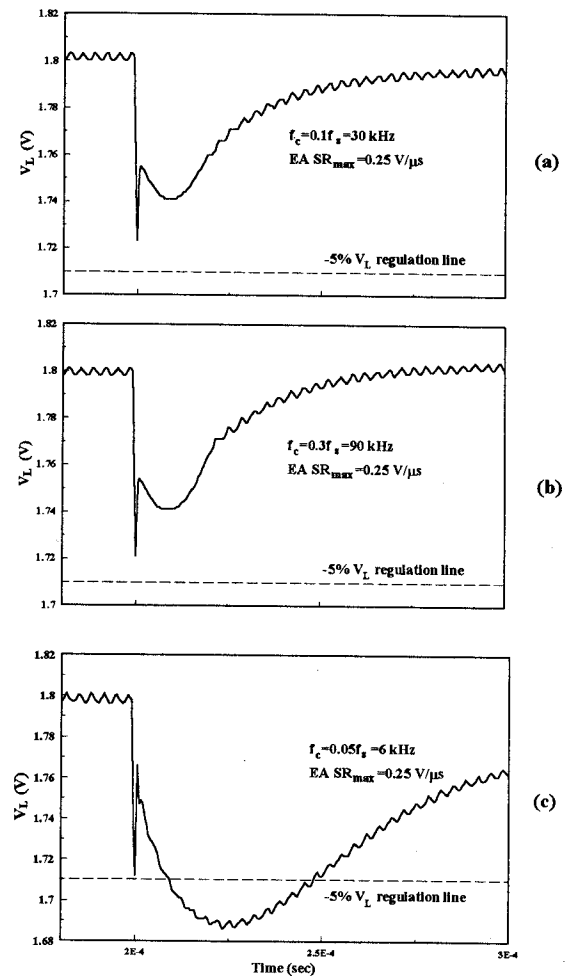


Fig. 17 Transient voltage waveforms of processor supplied by on-board converter operating at  $f_s=750$  kHz with different crossover frequencies  $f_c$ :  
(a)  $f_c=0.1f_s=30$  kHz;  
(b)  $f_c=0.3f_s=90$  kHz;  
(c)  $f_c=0.05f_s=6$  kHz.

From the above explanations, it can be concluded that the on-board converters do not need very high control-loop bandwidths to minimize the output-filter capacitor size. In fact, modest bandwidths of  $0.1f_s$  to  $0.2f_s$  were found to give satisfactory performance. However, since the response of the EA is slew-rate limited, the selection of the EA with a proper slew rate is of the utmost importance. As illustrated in Fig. 18(a), if the same EA ( $SR_{\max}=0.25$  V/ $\mu$ s) is used in an on-board converter operating at  $f_s=750$  kHz and with  $f_c=0.1f_s=75$  kHz, the transient response of the processor voltage cannot meet the specifications. Namely, for the switching frequency of 750 kHz the slew rate of 0.25 V/ $\mu$ s is not fast enough to change the duty cycle of the switch to the extreme ( $D=1$ ) in a couple of cycles because the switching period is very much reduced. However, if the EA is implemented with an operational amplifier that has a higher slew rate, as for example,  $SR_{\max}=1.2$  V/ $\mu$ s, the voltage transient can meet the spec for the same (minimum) output-filter capacitance and crossover frequency, as illustrated in Fig. 18(b).

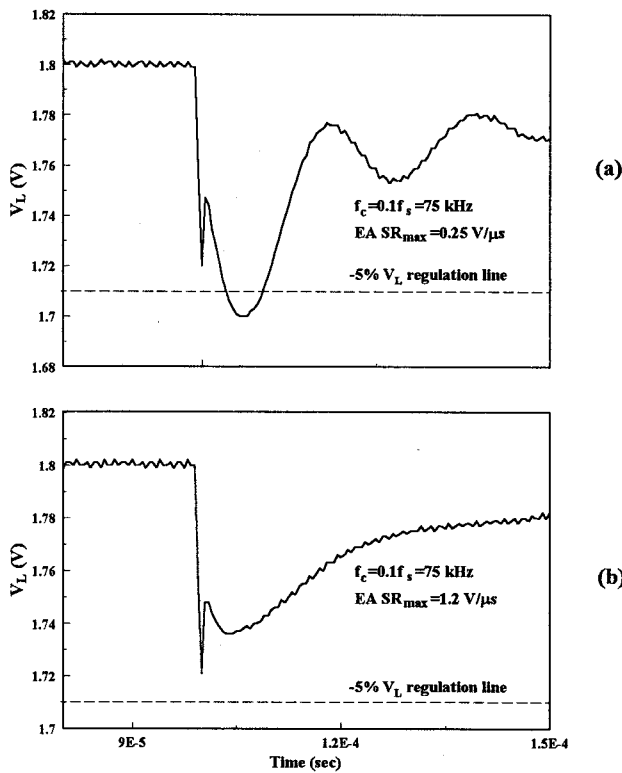


Fig. 18 Transient voltage waveforms of processor supplied by on-board converter operating at  $f_s=750$  kHz with crossover frequency of  $f_c=0.1f_s=75$  kHz for different slew rates of EA:

- (a)  $SR_{\max}=0.25$  V/ $\mu$ s;  
 (b)  $SR_{\max}=1.2$  V/ $\mu$ s.

According to the above discussion, the required slew rate of the EA amplifier, necessary to ensure that the extreme duty-cycle change will occur in less than two switching periods, can be calculated from

$$SR_1 > \frac{DV_{ramp}}{2(1/f_s)} = \frac{V_o V_{ramp}}{2V_{in}} f_s, \quad (10)$$

for active-to-sleep mode transition, i.e., duty cycle change from  $D=V_o/V_{in}$  (steady-state duty cycle) to  $D=0$ , and

$$SR_2 > \frac{V_{ramp} - DV_{ramp}}{2(1/f_s)} = \frac{V_{ramp}}{2} \left(1 - \frac{V_o}{V_{in}}\right) f_s, \quad (11)$$

for sleep-to-active mode transition, i.e., duty cycle change from  $D=V_o/V_{in}$  (steady-state duty cycle) to  $D=1$ .

In Eqs. (10) and (11),  $V_{ramp}$  is the oscillator ramp height, as shown in Fig. 11, and the term  $DV_{ramp}$  represents the EA output voltage steady-state value (when transients are settled). From Eqs. (10) and (11), the minimum required EA slew rate is

$$SR \geq \max(SR_1, SR_2). \quad (12)$$

Selecting the EA slew rate according to Eq. (12) ensures that the transient voltage specifications are met with the minimum output filter inductance calculated from Eq. (9) (i.e., Fig. 15). In the example given in Fig. 17, the required calculated minimum slew rate of the EA is 0.17 A/ $\mu$ s, while the corresponding slew rate for the circuit in Fig. 18 is 0.43 A/ $\mu$ s.

## V. Summary

The design guidelines of the on-board dc/dc module for low voltage, fast slew rate microprocessors have been presented. The effects of slew rate, interconnect inductance, on-board capacitance and its ESR and ESL have been analyzed. Selection criteria for input voltage, output capacitor, switching frequency, and control-loop bandwidth are given.

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