Study and Analysis on a High-Frequency Current-Source Single-Stage PFC Converter*

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ABSTRACT

The study and analysis of a high-frequency current-source (CS) single-stage power-factor-correction (S^2PFC) converter is presented in this paper. The general principles of the S^2PFC techniques are introduced first. Based on the general principles, this paper focuses on the CS S^2PFC technique and explores the effects of different circuit parameters on the input current THD and current ripple, the switch current stress, the energy-storage capacitor voltage stress and the overall efficiency. Simulation and experimental data are given to support the study and analysis.

I. INTRODUCTION

In recent years, many single-stage power factor correction (S^2PFC) techniques have been proposed to comply with IEC 1000-3-2 input current harmonics limits with low-cost and good performance. The input boost inductor in a S^2PFC converter can be operated in either discontinuous-conduction-mode (DCM) or continuous-conduction-mode (CCM). Generally, CCM S^2PFC converters are more desirable because of their small EMI filter, low current stress and good efficiency.

Figure 1 shows two CCM S^2PFC circuits with an additional high-frequency inductor L_1 [1][2]. Though these two circuits have different circuit topologies, they are functionally equivalent circuits. As a simple case, these two converters can be operated while N_1=N_p in Fig. 1(a) or no tapping on N_p in Fig. 1(b). In this case, the ideal waveforms of input voltage and boost inductor current are shown in Fig. 2. Because the high-frequency inductor L_1 can be regarded as a high-frequency current source, in this paper, the circuits in Fig. 1 are called current-source (CS) CCM S^2PFC circuits.

Above CS S^2PFC converters have good performance and low cost. Therefore, they have been proposed and studied in [1-4]. However, further study is still necessary to provide a comprehensive understanding and detailed design considerations of this converter. This paper focuses on the CS S^2PFC converter and explores the effects of different circuit parameters on the input current THD and current ripple, the switch current stress, the energy-storage capacitor voltage stress, and overall efficiency. Simulation and experimental data are given to support the study and analysis.

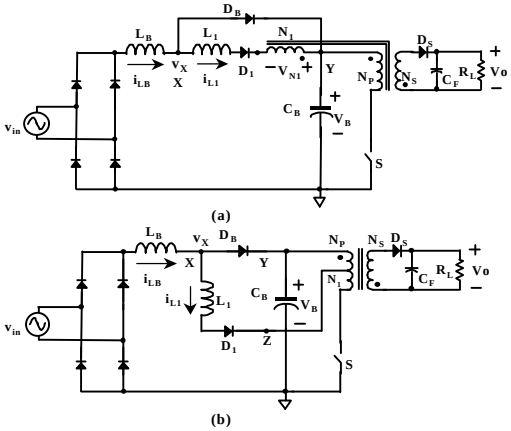
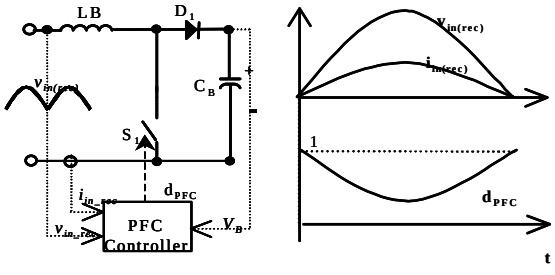


Fig. 1 CCM current-source S2PFC circuits with:
(a) two-terminal cell [2]; (b) three terminal cell [1]

II. BRIEF EXPLANATION OF THE PFC FUNCTION OF THE CS S^2PFC CONVERTER

As shown in Fig. 2, in order to achieve perfect input current shaping in the conventional CCM boost PFC converter, the switch duty cycle d_{PFC} has to decrease with the instantaneous line voltage increase in each half line cycle. Equation (1) shows the required duty-cycle of the CCM boost PFC converter during a half-line cycle[4]:

$$d_{PFC}(t) = 1 - \frac{V_{in(peak)} \cdot |\sin \nu t|}{V_B} \qquad (1)$$



(a) (b)

Fig. 2 Ideal CCM boost PFC circuit and its waveforms:
(a) Circuit diagram, and, (b) ideal voltage, current and duty-cycle waveform during a half line cycle

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However, in an integrated S^2PFC converter, the switch duty cycle is almost constant during a line cycle if the DC/DC stage is already in the steady state. To achieve input-current-shaping on a CCM S^2PFC boost inductor, the effective duty-cycle on the S^2PFC boost inductor should be modulated in the way similar to the ideal PFC duty-cycle shown in Fig. 2(b). In the CS S^2PFC converter, the effective duty-cycle is achieved by the additional current-source inductor L_1. Figure 3 shows the input current waveforms of the CS S^2PFC converter and Fig. 4 shows the principle switching waveforms of the CS S^2PFC converters at different time instances A and B in Fig.3. Because the current commutation between the boost diode D_B and the CS inductor L_1 after switch S is turned on in each switching cycle [3], the effective duty-cycle on the boost inductor is actually less than the switch duty-cycle D, as shown in Fig. 4. Fig. 4 also shows that the instantaneous effective duty-cycle D_{eff} decreases with the line voltage increases, which follows the shape of the ideal PFC duty cycle in Fig. 2(b). Equation (2) represents the effective duty cycle D_{eff}. When the input voltage rises, the boost inductor current i_{LB} also rises. As the result, the effective duty cycle will decrease. Therefore, the input current can be shaped.

Above is just a brief explanation of the principle of the CCM CS S^2PFC circuits. In following sections, the detailed discussions on the effects of several key parameters will be given and a design guideline will be provided.

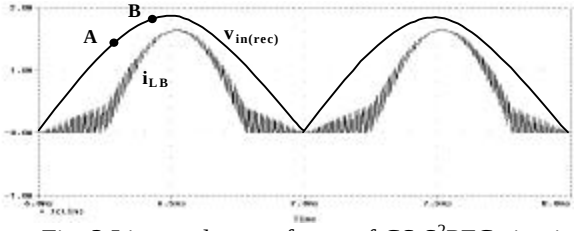

Fig. 3 Line cycle waveforms of CS S^2PFC circuit

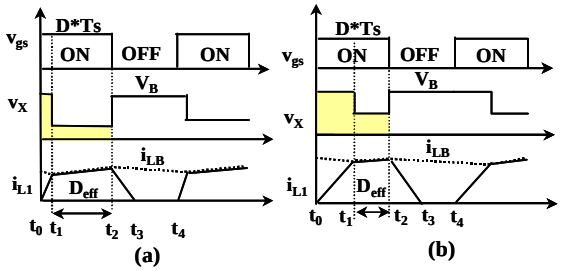

Fig. 4 Switching waveforms of the CS S^2PFC circuit

$$D_{eff} = \frac{DV_B - L_1 f_s i_{LB}}{V_B - \frac{v_{in(rec)} \cdot L_1}{L_1 + L_B}} \approx D - \frac{L_1 \cdot f_s \cdot i_{LB}}{V_B} \qquad (2)$$

(Only apply to L_B in CCM mode)

III. STUDY AND DISCUSSIONS OF THE CS S^2PFC CONVERTERS

In order to provide design guidelines to help further understand and optimize the CS S^2PFC circuit, further study is necessary. In this section, the analysis and design guidelines will be discussed on different circuit parameters and different issues.

3.1 INPUT CURRENT HARMONICS

According to the input-current-shaping (ICS) mechanism of the CS S^2PFC converter, theoretically, L_1 is the key design parameter for input current harmonics. To get adequate input current harmonics margin to meet the IEC61000 harmonics standard, L_1 need be operated in DCM mode. Therefore, each switching cycle when the switch is turn on, the current in L_1 can start from zero to get a strong modulation effect. Similarly, from the modulation effect point of view, a large L_1 is preferred. However, L_1 cannot be too large, otherwise L_1 will enter CCM mode at low line, full load. If so, as can been seen in Fig. 5, the time interval t_0-t_1 for L_1 current to reach i_{LB} will be reduced because the initial value of i_{L1} is larger than zero. Figure 5(a) shows L_1 in DCM with strong effect on duty-cycle while fig. 5(b) shows L_1 in CCM with reduced effect on duty cycle. Consequently, the PFC modulation effect will be hurt if L_1 enters CCM mode.

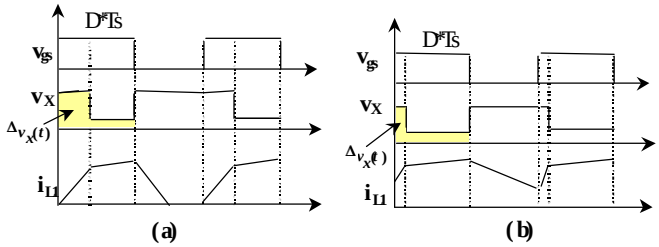

Fig. 5 Over-designed L_1 will enter CCM current mode
(a) Switching waveform with properly designed DCM L_1
(b) Switching waveform with over-designed L_1

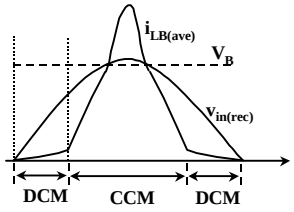

Fig. 6 Conceptual waveform of high current distortion caused by over-designed L_1 while V_B is already lower than $v_{in(peak)}$

Besides, it is necessary to point out that there is another big impact if L_1 is over-designed. Because L_1 can reduce the effective duty-cycle on the boost inductor, it also reduces the bulk-capacitor voltage V_B. If L_1 is too large, V_B will be too low so that it can be even lower than the peak input voltage.

As the result, L_B cannot have adequate reset during the time interval while $v_{in(rec)}$ is higher than V_B. L_B will be saturated and have a highly distorted current peak, as shown in Fig. 6.

As a summary, to satisfy the PFC condition a large L_1 is preferred but L_1 cannot be too large. In section 4, a design curve of L_1 will be given.

3.2 BULK CAPACITOR VOLTAGE STRESS

The bulk energy-storage capacitor voltage V_B stress in a S^2PFC converter is also a key design consideration. In the ideal CCM boost PFC converter, the boost output voltage is given in Equation 3, which shows the relationship between half-line-average duty-cycle D_{AVE} and boost output voltage V_B. The CS CCM S^2PFC converter has much lower voltage stress than the DCM S^2PFC converter without capacitor voltage-feedback windings. This can be explained with two reasons. First, the CS S^2PFC converter is designed to have CCM boost inductor current. This means that L_B in the CS S^2PFC converter has much larger inductance than it does in a DCM S^2PFC converter. Normally, in S^2PFC converter, a large boost inductor L_B helps to reduce V_B stress [6]. However, the more important reason is that the additional inductor L_1 introduces effective boost duty-cycle D_{eff} on L_B and D_{eff} is smaller than the switch duty-cycle. With the reduced duty-cycle, capacitor voltage V_B is reduced. In the CS S^2PFC, theoretically, the boost capacitor voltage V_B should be able to be calculated in a similar way as in Equation 3 while the D_{AVE} is actually the average of the effective duty-cycle D_{eff}. However, because the switch duty-cycle is determined by the dc/dc output stage and V_B changes with load and line changes, an numerical integration has to be used based on the input/output power balance, in order to calculate the actual V_B in stead of a simple equation like Equation 3.

$$V_B = \frac{V_{in(AVE)}}{1 - D_{AVE}} \qquad (3)$$

--- (Use $D_{eff(AVE)}$ if in CCM S^2PFC circuit)

Nevertheless, Equation 2 and 3 can conceptually show how the V_B changes with the load current or L_1. If output load current decreases, the input inductor current i_{LB} will also decrease to maintain the input/output power balance. According to Equation 2, the effective duty-cycle will increases. Therefore, the capacitor voltage V_B will increase at light load. On the other hand, large L_1 will always give smaller effective duty-cycle, resulting in lower V_B. To provide adequate voltage margin for the 450 V electrolytic capacitor at high line, light load, a large L_1 is always preferred to further reduce $V_{B(max)}$, as long as V_B is higher than the minimum $V_{in(peak)}$ at low line, full load.

Other than using a large L_1, there is a more effective way to reduce V_B stress [1][3]. It is to use a tapped dc/dc converter transformer as shown in Fig. 1(b) or design the winding N_1 to be less than N_p as in Fig.1 (a). The principle of the tapped transformer is similar as the DCM S^2PFC converter with feedback winding N_1 [6]. Generally, with the feedback winding or transformer tapping, V_B stress can be reduced significantly and the efficiency can be improved. Besides, in the CS S^2PFC converter, the feedback winding can reduce the voltage-second on L_B and L_1, therefore, smaller cores may be used to reduce the size and cost. The effect of feedback winding can be quantified by the feedback ratio K_{FB}, which is defined as in Equation 4 or 5 for the S^2PFC circuits in Fig. 2(a) or 2(b), respectively. Once these two circuits have same feedback ratio K_{FB}, they have identical functionality and performance.

In two-terminal S^2PFC: $$K_{FB} = \frac{N_p - N_1}{N_p} \qquad (4)$$

In three-terminal S^2PFC: $$K_{FB} = \frac{N_1}{N_p} \qquad (5)$$

The drawback of using a feedback winding or transformer tapping is the dead conduction angle on the input current introduced by the winding N_1 [3][6]. With the induced voltage on winding N_1 in Fig. 2(b), the front-end diode-bridge can not have input current near the line-voltage-crossover time interval. The dead conduction angle will cause additional input current distortion. Nevertheless, it is necessary to point out that for low power application (P_{in} < 600W) in IEC61000 class D range, it is fine for the input current have certain distortion. In fact, minimum current distortion is not a design goal as long as the current harmonics can meet IEC limits [6]. An optimized circuit should have the input current harmonics just lower than the IEC limits with certain margin, and, have optimized efficiency, low voltage stress and low cost.

As a summary, from reducing V_B stress point of view, an optimal design needs L_1 and N_1/N_p to be as large as possible while the input current can still meet IEC harmonics limits. A design approach will be presented in section 4 with experimental data.

3.3 CURRENT STRESS AND EFFICIENCY

The converter efficiency is also an important consideration of the S^2PFC converters. To get good efficiency, there are two major design parameters to be considered. As discussed in previous section, the current-source inductor L_1 and transformer tapping N_1/Np (Fig. 2(b)) can reduce the bulk capacitor voltage stress. A lower V_B means lower rating semiconductor component and lower semiconductor loss. Furthermore, as can been seen on Fig. 7,

a large L_1 or a higher N_1/N_p ratio can reduce the charging rate of the inductor current i_{L1} after switch S is turned on at t_0. In Fig. 7, the dashed line shows the v_X and i_{L1} waveforms with a smaller L_1 or N_1/N_p and the solid line shows the v_X and i_{L1} waveforms with a larger L_1 or N_1/N_p. As can be seen, the RMS current through L_1 to switch S can be reduced with large L_1 value or high N_1/N_p ratio. Therefore, the switch conduction loss can be reduced. As a result, large L_1 or high N_1/N_p ratio can improve the converter efficiency. This is proved experimentally in section 4. Again, as discussed in previous sections, the value of L_1 or N_1 cannot be too high because of the constraint from the input current harmonics limits.

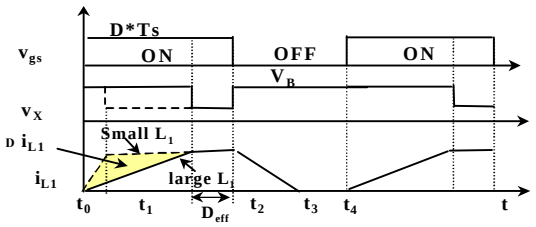

Fig. 7 Reduced switch current with L_1 or N_1/N_p (Fig.2(b))

IV. SIMULATION AND EXPERIMENTAL DESIGN STUDY OF THE CS S²PFC CONVERTER

Different L_B and L_1 values have been studied with simulation and experiment for the design optimizations. The simulation/experimental circuit is designed to have a universal-line input (90-265Vac) and 5V/40A output, which is similar to the specifications of a typical low-end computer power supply. One fundamental problem for the circuits in Fig. 2 are their wide capacitor voltage V_B range with universal line input [7]. To optimize the performance in universal-line range, the voltage-doubler version of CS S²PFC circuit [8] has to be used as shown in Fig. 8. The voltage-doubler CS S²PFC circuit has same operation principle as the circuit in Fig. 2 except there is a range-selection switch SW, which is always closed in the American line range (90-135V_{ac}) and opened in the European line range (180-265V_{ac}).

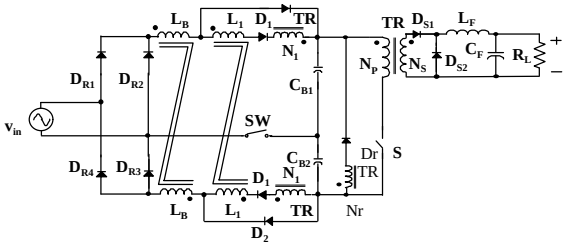

Fig. 8 Circuit diagram for simulation and experiment

The key experimental circuit components have been chosen as follows: L_B: 45 - 190 μH (each winding), L_1: 30 - 100 μH (each winding), N_1 = 14 T, N_p = 52 T, N_r = 52 T and N_s = 3 T, $C_{B1,2}$: 470 uF/250V, switch S: IXYS 12N100 and Schottky diode $D_{S1\text{-}2}$: IR81CND45, switching frequency fs=70kHz. It is necessary to point out that the feedback ratio K_{FB} for this voltage-doubler S²PFC should be defined in Equation 7 to have same effect as K_{FB} in the CS S²PFC circuit in Fig. 2(a).

$$K_{FB} = \frac{0.5 \cdot N_P - N_1}{0.5 \cdot N_p} \tag{7}$$

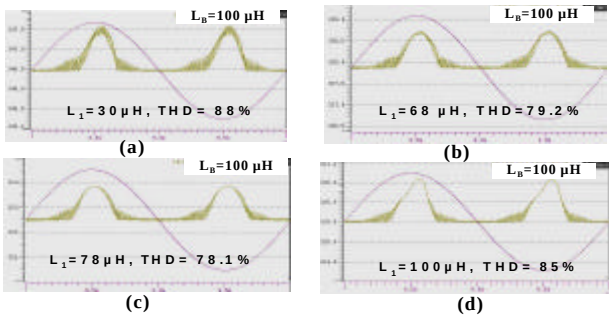

Fig. 9 Different boost inductor current with different L_1

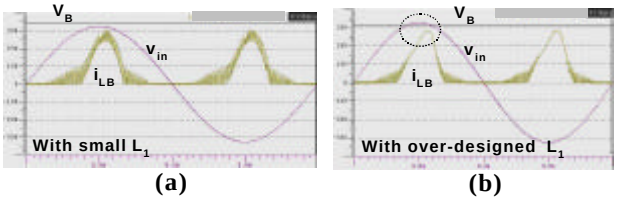

Fig.10 Simulation waveforms show low V_B cause i_{LB} distortion with over-designed L_1

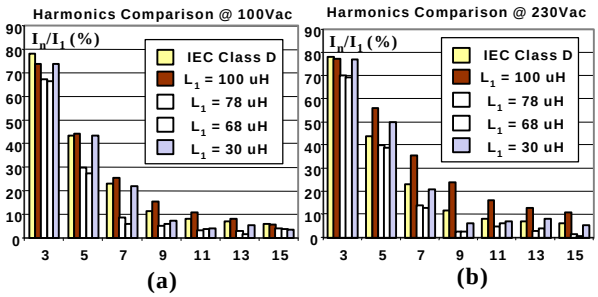

Fig. 11 Line input current harmonics with different L_1

First, to study the L_1 effect on the input current, L_B was fixed at 100 μH and several different L_1 have been used in the circuit in Fig. 8. Figure 9 shows different input current waveforms in simulations with different L_1 inductance at 230 V_{ac}, full load. This figure was obtained with a closed voltage-loop simulation with Simplis® software. As shown in Figure 9(d), if L_1 is over designed, there is high distortion on the input current because V_B is lower than $V_{in(peak)}$. The input current THD is about 85%. After L_1 was decreased to 78 μH,

V_B was already higher than $v_{in(peak)}$. Therefore, the input current has much less distortion and input current THD was reduced to 78.1%, as shown in Fig. 9(c). After that, if L_1 was too small, the converter did not have enough PFC modulation and the distortion increased again. For example, as shown in Fig. 9(a), input current has high distortion again and THD = 88%. Figure 10 shows the simulation waveforms with proper-designed L_1 and over-designed L_1. It confirms that with over-designed L_1, V_B will be lower than $V_{in(peak)}$, resulting in high current distortion. Figure 11 shows the current harmonics comparison with different L_1. As can been seen, for L_1 around 68 and 78 μH, the CS S^2PFC circuit can meet the IEC standard with plenty margin.

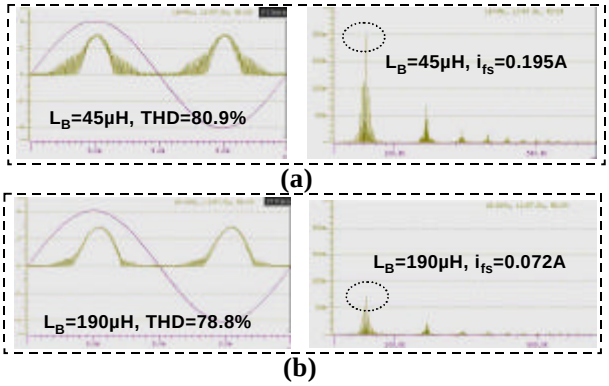

Fig. 11 Boost inductor current waveforms with different L_B

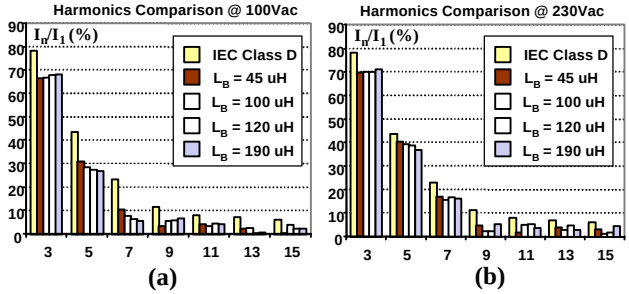

Fig. 12 Line input current harmonics with different L_B

To show L_B's effect on the input current, L_1 is fixed as L_1=68 μH and several different L_B values were used in the experimental circuit. Figure 11 shows the different boost inductor current waveforms in simulations and the input current THD. As can been seen, the input current THD just changed a little while L_B had significantly different values, from 45 μH to 190 μH. It shows that L_B has relatively weak effect on the low frequency input current harmonics. This fact is also proved by Fig. 12, which shows the low frequency input current harmonics with different L_B. However, as shown in Fig. 11, the effect of different L_B is the difference on the boost inductor current ripple at switching frequency. A large L_B means small current ripple on L_B. Theoretically, the current ripple should be determined by the total inductance L_B + L_1. This is because during the time interval of boost inductor charging, these two inductors have the total input voltage on them. Figure 13 shows the curve of total inductance vs. the boost current ripple. The switching frequency current ripple is going to determine the differential mode EMI filter size.

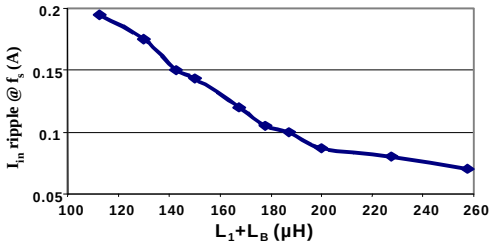

Fig. 13 Switching-frequency current ripple on boost inductor is determined by the total inductance of L_B and L_1

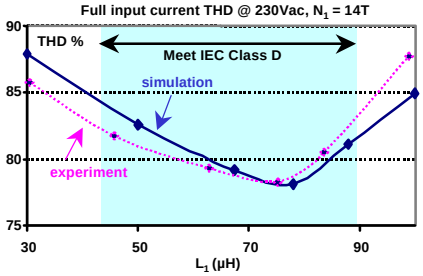

Fig. 14 Simulated and experimental L_1 vs. THD curve

$$\text{Normalized } L_1: \quad L_1^* = L_1 \cdot f_s \cdot P_o / h \qquad (8)$$

Figure 14 provides the simulation and experiment curves of the input current THD vs. L_1. It shows the simulation result is quite close to the experimental result. This curve can be used for design reference of the CS S^2PFC with fixed feedback ratio K_{FB} = 0.4~0.5. It is necessary to point out that this K_{FB} is already close to optimized value for universal line input, based on our experience. In a design, L_1 should be chosen inside the shaded area to guarantee the input current harmonics meet IEC class D limits. Generally, within this shaded area in Fig. 14, L_1 should be chosen as large as possible to get the low V_B stress and the good efficiency. For the circuit with different output power P_o, efficiency η and switching frequency f_s, the curve shown in Fig. 14 can be normalized with Equation 8. The principle of normalization is based on the effective duty-cycle d_{eff} by Equation 2.

Figure 15 shows L_B's and L_1's effects on the bulk capacitor voltage V_B stress in the experiment. As can been seen, a larger L_B or L_1 will result in a lower V_B. Figure 16 shows different measured efficiencies with different L_B and L_1. As can been seen in Fig. 16(a), a large L_B can increase efficiency a little (less than 0.4%) because of smaller current ripple. On the other hand, L_1 has stronger effect on the

efficiency (about 2.6% difference). By increasing L_1 value, as discussed in Section 3, the switch current stress can be reduced and a better efficiency can be achieved. However, after L_1 reaches a certain value, because V_B starts to be lower than $v_{in(peak)}$, a high current peak occurs which increase the current stress. The efficiency does not increase any longer. With the voltage-doubler front-end, the full-load (5V/40A) efficiency of this converter is higher than 80% in full line range (90-265Vac) which is better, or, at least comparable to two-stage PFC approach.

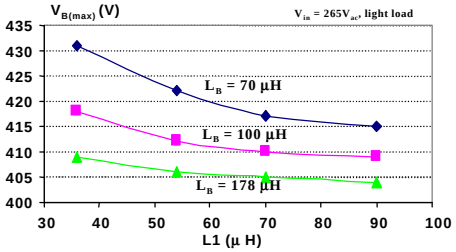

Fig. 15 Capacitor voltage $V_{B(max)}$ changes with L_1 and L_B

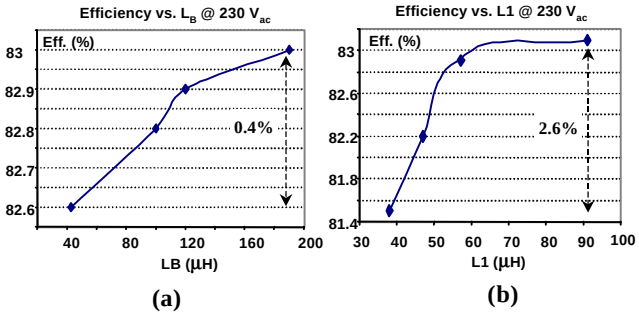

Fig. 16 Full load efficiency with different L_1 and L_B

In summary, many different issues need to be considered during the design of this converter. The feedback winding ratio K_{FB} with N_1, inductor L_B and L_1 are important design parameters of the CS S^2PFC converter. Generally, as to N_1, the feedback ratio K_{FB} should be chosen as high as possible to achieve high efficiency and low V_B stress, until it is hard for the converter to meet IEC61000 Class D harmonics limits. The optimized K_{FB} is in 0.4~0.5 range. L_1 and L_B should be selected by considering Figs. 14 – 16. The design objective is to get the lowest V_B stress and highest efficiency while the converter can still meet IEC harmonics limits. Within the IEC limits, L_1 should be chosen a large value based on Fig. 14. To provide a straightforward design approach, Fig. 17 summarizes the design steps and provides clear design guidelines of the voltage-doubler CCM CS S^2PFC for universal line applications. It is necessary to point out that a few straightforward steps are not enough for the design optimization of this converter. Numerical analysis, simulations, and experiments are all necessary to get the optimal design. In addition, the dc/dc output stage design should be quite similar as the conventional dc/dc converter design.

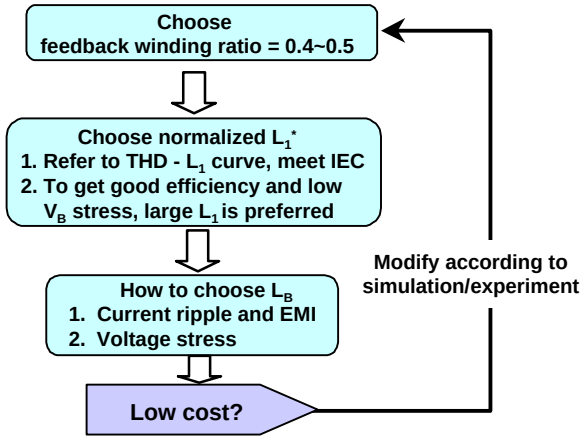

Fig. 17 Design guideline of CS S^2PFC converter
(with voltage-doubler front-end for universal line input)

V. SUMMARY

In this paper, the detailed analysis and experimental data have been provided to explore the issues in the CCM CS S^2PFC converter. Different circuit parameters' effect on input current, switch current stress, circuit voltage stress and overall efficiency have been presented. Design considerations and guidelines have been discussed with the simulation and experimental data.

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