Design Optimization of Single-Stage, Single-Switch Input-Current Shapers

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Abstract - Design considerations for a recently introduced single-stage, single-switch, input-current-shaper (S^4ICS) which combines the boost-like front end with a continuous-conduction-mode dc/dc output stage are provided. A complete design-oriented mathematical model is derived for both the discontinuous and continuous conduction modes of operation of the boost inductor. The design procedure is illustrated on the example of a 5 V/20 A, universal line-voltage range S^4ICS forward converter.

I. Introduction

A number of single-stage, single-switch input-current shapers (S^4ICSs) with fast output-voltage regulation were introduced in [1]-[9]. Most of the reported S^4ICS circuits employ discontinuous conduction mode (DCM) of operation in the ICS stage, usually with boost topology. In these circuits, low input-current harmonic distortions are achieved by the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle during a line period is held relatively constant.

The implementation of the continuous conduction mode (CCM) of operation in the ICS stage is more challenging because a single switch has to control two different duty cycles; i.e., a constant duty cycle of the dc/dc converter (in steady state) and a variable duty cycle of the ICS inductor. Up to date, the CCM operation of the ICS stage has been reported in [4], [6], and [9]. The variable duty cycle for the CCM operation of the ICS inductor can be achieved by using an additional capacitance [4], additional inductance (leakage inductance of the transformer and/or external inductance) [6], or by employing the charge pump concept [9]. The S^4ICS circuits presented in [6] and [9] are particularly attractive as they are suitable for universal line-voltage operation.

In this paper, design considerations for the S^4ICSs introduced recently in [6] are provided. The forward converter implementation of the S^4ICSs is shown in Fig. 1.

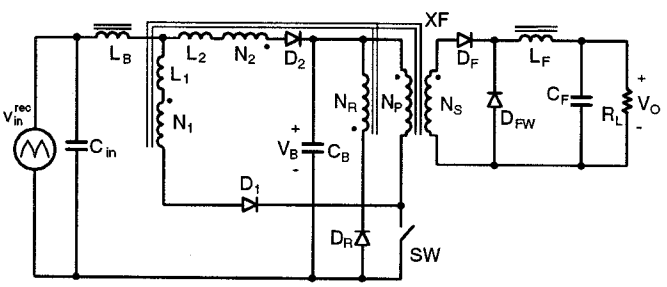

Fig. 1 S^4ICS forward converter introduced in [6]

The variable duty cycle for the CCM operation of the boost inductor, L_B, is achieved by inductance L_1 and/or inductance L_2, which can be leakage inductance(s) of the transformer *XF* and/or external inductance(s). Principles of operation are given in [6].

In this paper a complete design-oriented analysis is provided for both DCM and CCM operations of the boost inductor. Design equations, and design curves for design optimization are given. The design procedure is illustrated on the example of a 5 V/20 A, universal line-voltage range (90-265 V_{rms}) S^4ICS forward converter.

II. DCM Operation of Boost Inductor

A. *Analysis*

To simplify the analysis, the following assumptions were made:

- input voltage is a full-wave rectified sine wave,

$$v_{in}^{rec} = V_{im}\left|\sin(\omega_L t)\right| \; ; \tag{1}$$

- input voltage is constant during a switching cycle because the switching frequency, f_S, is much higher than the line frequency, $f_L = \omega_L/2\pi$;
- energy-storage capacitor voltage, V_B, is constant during each half of a line cycle;
- all semiconductor components are ideal, only the forward voltage drop of the secondary-side diodes is not neglected;
- power transformer *XF* does not have leakage inductances, but possesses a finite magnetizing inductance.

During a half of a line cycle, two DCM operations of the boost inductor can happen, as shown in Fig. 2. In DCM**a**, the reset of L_B is completed before the reset of the transformer, i.e., $D_{rLB} < D_{rXF}$, which results in a triangular waveform of i_{LB}, as shown in Fig. 2(a). In DCM**b**, the transformer resets before the boost inductor, which yields a more complex waveform of i_{LB}, as shown in Fig. 2(b).

In DCM**a**, the average boost inductor current, which is also the line current, is determined as

$$i_{LBav}^{DCMa} = \frac{D + D_{rLB}}{2} \cdot i_{LBpk} \; , \tag{2}$$

where the peak inductor current is

$$i_{LBpk} = \frac{v_{in}^{rec} - \dfrac{N_1}{N_P} V_B}{L_B f_S} \cdot D \; . \tag{3}$$

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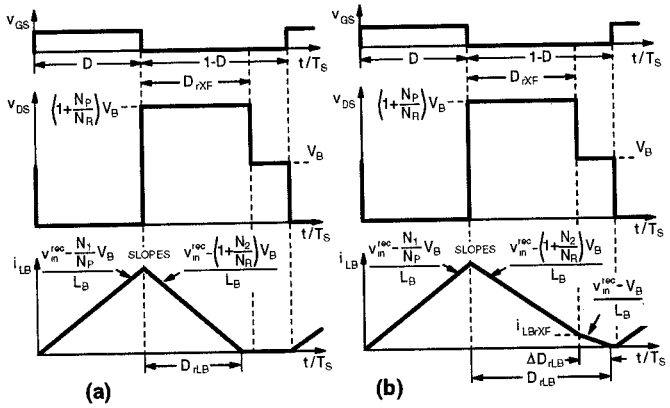


Fig. 2 Key waveforms in (a) DCM**a**, (b) DCM**b** operation of boost inductor

From the flux balance of the boost inductor,

$$\left(v_{in}^{rec}-\frac{N_1}{N_P}\cdot V_B\right)\cdot D=\left[\left(1+\frac{N_2}{N_R}\right)\cdot V_B-v_{in}^{rec}\right]\cdot D_{rLB}\ , \quad (4)$$

it follows that

$$D+D_{rLB}=\frac{1-\frac{N_1}{N_P}+\frac{N_2}{N_R}}{1+\frac{N_2}{N_R}-\frac{v_{in}^{rec}}{V_B}}\cdot D\ . \quad (5)$$

Substituting (3) and (5) into (2), the average boost inductor current in DCM**a** is obtained as

$$i_{LBav}^{DCMa}=\frac{V_B D^2}{2L_B f_S}\cdot\frac{A_1+A_2\frac{v_{in}^{rec}}{V_B}}{1+\frac{N_2}{N_R}-\frac{v_{in}^{rec}}{V_B}}\ , \quad (6)$$

where

$$A_2=1-\frac{N_1}{N_P}+\frac{N_2}{N_R}\ \text{ and }\ A_1=-\frac{N_1}{N_P}A_2\ . \quad (7)$$

In DCM**b**, the average boost inductor current is determined as

$$i_{LBav}^{DCMb}=\frac{D+D_{rXF}}{2}\cdot i_{LBpk}+\frac{D_{rXF}+\Delta D_{rLB}}{2}\cdot i_{LBrXF}\ , \quad (8)$$

where

$$D_{rXF}=\frac{N_R}{N_P}\cdot D \quad (9)$$

is the transformer reset cycle, i_{LBpk} is the peak inductor current defined in (3), i_{LBrXF} is the boost inductor current at the moment the transformer core reset is completed, i.e.,

$$i_{LBrXF}=\frac{V_B-v_{in}^{rec}}{L_B f_S}\cdot\Delta D_{rLB}\ , \quad (10)$$

and ΔD_{rLB} represents the additional reset interval of L_B after the reset of the transformer is completed. ΔD_{rLB} can be obtained from the flux balance of L_B,

$$\left(v_{in}^{rec}-\frac{N_1}{N_P}\cdot V_B\right)\cdot D=\left[\left(1+\frac{N_2}{N_R}\right)\cdot V_B-v_{in}^{rec}\right]\cdot\frac{N_R}{N_P}\cdot D+\left(V_B-v_{in}^{rec}\right)\cdot\Delta D_{rLB}\ . \quad (11)$$

From (11), it follows that

$$\Delta D_{rLB}=\frac{\left(1+\frac{N_R}{N_P}\right)\cdot\frac{v_{in}^{rec}}{V_B}-\frac{N_R+N_1+N_2}{N_P}}{1-\frac{v_{in}^{rec}}{V_B}}\cdot D\ . \quad (12)$$

Substituting (3), (9), (10), and (12) into (8), the average boost inductor current in DCM**b** is obtained as

$$i_{LBav}^{DCMb}=\frac{V_B D^2}{2L_B f_S}\cdot\frac{B_1+B_2\frac{v_{in}^{rec}}{V_B}}{1-\frac{v_{in}^{rec}}{V_B}}\ , \quad (13)$$

where

$$B_1=\left(\frac{N_1+N_2}{N_P}\right)^2-\frac{N_1}{N_P}+\frac{N_2N_R}{N_P^2}\ , \quad (14)$$

and

$$B_2=1-\frac{N_1}{N_P}-\frac{N_2}{N_P}\cdot\left(2+\frac{N_R}{N_P}\right)\ . \quad (15)$$

The boundary condition between DCM**a** and DCM**b** operations can be found from (12). The condition for operation of L_B in DCM**b** is $\Delta D_{rLB}>0$, i.e.,

$$v_{in}^{rec}>\frac{N_R+N_1+N_2}{N_R+N_P}\cdot V_B\ , \quad (16)$$

whereas, the boundary angle between DCM**a** and DCM**b** is defined as

$$\theta_{ab}=a\sin\left(\frac{N_R+N_1+N_2}{N_R+N_P}\cdot\frac{V_B}{V_{im}}\right)\ . \quad (17)$$

The operation modes of the DCM boost inductor are summarized in Fig. 3. A typical line current waveform is also

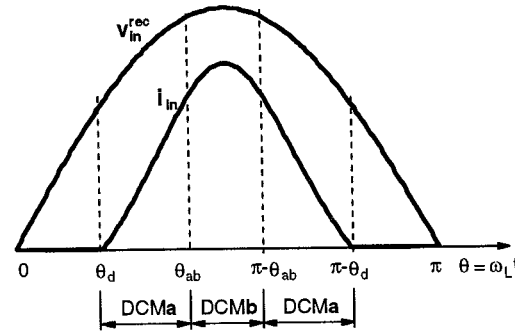


Fig. 3 Operation modes of DCM boost inductor

shown in Fig. 3. The zero-crossing angle (dead angle), θ_d, is defined as

$$\theta_d = a\sin\left(\frac{N_1}{N_P}\cdot\frac{V_B}{V_{im}}\right). \quad (18)$$

B. Design

Since the energy-storage capacitor voltage, V_B, in a S^{4}ICS is not regulated, it varies with the input line. To minimize the cost, it is desirable to keep V_B below 400 V so that a capacitor with a rated voltage of 450 V can be safely used. Therefore, the design goal is to keep energy-storage-capacitor voltage V_B between a maximum value, $V_{B\max}$ (e.g., $V_{B\max} = 400$ V), and a minimum value, $V_{B\min}$, which is determined either by the maximum achievable duty cycle set by the PWM circuit (e.g., $D_{\max} = 0.49$) or by the condition to keep L_B in DCM (see (26)), whichever yields a larger value of $V_{B\min}$. The design parameters are L_B, L_F, N_P, N_R, N_S, N_1, and N_2.

Voltage V_B can be obtained from the input-output power balance,

$$\frac{2}{\pi}\int_{\theta_d}^{\theta_{ab}} i_{LBav}^{DCMa}\, v_{in}^{rec}\, d\theta + \frac{2}{\pi}\int_{\theta_{ab}}^{\pi/2} i_{LBav}^{DCMb}\, v_{in}^{rec}\, d\theta = \frac{V_o I_o}{\eta}, \quad (19)$$

where η is the assumed efficiency of the converter.

Voltage V_B reaches $V_{B\max}$ at high line, when forward inductor L_F operates at its DCM-CCM boundary, which occurs at some output current $I_o \le I_{o\max}$. In fact, when L_F operates in CCM, with decreasing output current the bulk-capacitor voltage increases; when L_F enters DCM, voltage V_B does not depend on the output current any more, as shown in [3]. To achieve a higher efficiency, it is desirable the DCM-CCM boundary of L_F to occur at a lower output current.

At the DCM-CCM boundary of L_F, the output current is determined as

$$I_{oDCH} = \frac{(V_o + V_F)\cdot(1 - D_{\min})}{2 L_F f_S}, \quad (20)$$

and duty cycle $D_{\min}$ is obtained from the flux balance of L_F as

$$D_{\min} = \frac{N_P}{N_S}\cdot\frac{V_o + V_F}{V_{B\max}}. \quad (21)$$

Substituting (1), (6), (7), (13)-(15), (20), and (21) into (19) at high line, the ratio of the boost and forward inductances can be obtained as

$$\frac{L_B}{L_F} = \frac{2\eta_H}{\pi}\cdot\frac{\frac{V_{imH}}{V_{B\max}}\cdot\left(\frac{N_P}{N_S}\right)^2}{1 - \frac{N_P}{N_S}\cdot\frac{V_o + V_F}{V_{B\max}}}\cdot\left(1 + \frac{V_o}{V_F}\right)\cdot K_H, \quad (22)$$

where V_{imH} is the amplitude of the high line voltage, η_H is the assumed efficiency of the converter at high line, and

$$K_H = A_2\int_{\theta_{dH}}^{\theta_{abH}} \frac{\frac{V_{imH}}{V_{B\max}}\sin(\theta) - \frac{N_1}{N_P}}{1 + \frac{N_2}{N_R} - \frac{V_{imH}}{V_{B\max}}\sin(\theta)}\cdot\sin(\theta)\, d\theta$$

$$+ B_1\int_{\theta_{abH}}^{\pi/2} \frac{\sin(\theta)}{1 - \frac{V_{imH}}{V_{B\max}}\sin(\theta)}\, d\theta + B_2\int_{\theta_{abH}}^{\pi/2} \frac{\frac{V_{imH}}{V_{B\max}}\sin^2(\theta)}{1 - \frac{V_{imH}}{V_{B\max}}\sin(\theta)}\, d\theta. \quad (23)$$

In (23), θ_{dH} is the zero-crossing angle, defined in (18), at high line, and θ_{abH} is the DCM**a**-DCM**b** boundary angle, defined in (17), at high line.

Voltage $V_B = V_{B\min}$ at low line and full load, when forward inductor L_F operates in CCM. $V_{B\min}$ is determined either by the maximum achievable duty cycle or by the condition to keep L_B in DCM (see (26)), whichever yields a larger value of $V_{B\min}$.

Writing $I_o = I_{o\max}$ in (19) and substituting (1), (6), (7) and (13)-(15) into (19) at low line, the product of the boost inductance and switching frequency can be obtained as

$$L_B f_S = \frac{\eta_L}{\pi}\cdot\frac{\frac{V_{imL}}{V_{B\min}}\cdot\left(\frac{N_P}{N_S}\right)^2}{I_{o\max}}\cdot\frac{(V_o + V_F)^2}{V_o}\cdot K_L, \quad (24)$$

where V_{imL} is the amplitude of the low line voltage, η_L is the assumed efficiency of the converter at low line, and K_L is determined by the same expression as (23), by replacing V_{imH}, $V_{B\max}$, θ_{dH}, and θ_{abH} with V_{imL}, $V_{B\min}$, θ_{dL}, and θ_{abL}, respectively.

Using (22) and (24), for selected values of N_P, N_R, N_S, N_1, and N_2, and selected switching frequency f_S, the inductances L_B, L_F will be determined. The values of N_P, N_R, and N_S should be selected as for the conventional dc-dc forward converter. Finally, N_1 and N_2 should be selected according to the following considerations.

To keep the operation of L_B in DCM, the condition

$$D + D_{rXF} + \Delta D_{rLB} \le 1 \quad (25)$$

should be satisfied. Substituting (9) and (12) into (25), and using the flux balance of L_F, it follows that

$$V_B \ge V_{im} + \left(\frac{N_P}{N_S} - \frac{N_1 + N_2}{N_S}\right)\cdot(V_o + V_F). \quad (26)$$

Applying (26) at high line, the minimum value of $N_1 + N_2$ can be obtained as

$$\frac{N_1 + N_2}{N_P} \ge 1 - \frac{V_{B\max} - V_{imH}}{\left(\frac{N_P}{N_S}\right)\cdot(V_o + V_F)}. \quad (27)$$

The maximum value of $N_1 + N_2$ is determined by the requirement for a proper operation of the circuit during on-time of the switch [6],

$$\frac{N_1+N_2}{N_P}<1\ . \qquad (28)$$

Applying (26) at low line, the minimum value of voltage V_B can be calculated as

$$V_{B\min}\geq V_{imL}+\left(\frac{N_P}{N_S}-\frac{N_1+N_2}{N_S}\right)\cdot\left(V_o+V_F\right)\ . \qquad (29)$$

To optimize the performance, $V_{B\min}$ should be as small as possible. It follows from (29) that smaller $V_{B\min}$ will be achieved with larger N_1+N_2. Therefore, N_1+N_2 should be selected close to its maximum possible value, i.e., N_1+N_2 should be equal to the number of primary turns reduced by one or two turns.

It should be noted that the voltage $V_{B\min}$ determined by (29) presents the minimum value of the bulk-capacitor voltage only if it yields a maximum duty cycle

$$D_{\max}=\frac{N_P}{N_S}\cdot\frac{V_o+V_F}{V_{B\min}}<\frac{1}{1+\dfrac{N_R}{N_P}}\approx 0.5\ . \qquad (30)$$

Otherwise, the minimum value of the bulk-capacitor voltage is determined by the maximum achievable duty cycle.

It is interesting to find the condition for L_B operating only in DCMa, i.e., the condition for $D_{rLB}\leq D_{rXF}$. From (16), applied at high line, it follows that

$$\frac{N_1+N_2}{N_P}\geq\left(1+\frac{N_R}{N_P}\right)\cdot\frac{V_{imH}}{V_{B\max}}-\frac{N_R}{N_P}\ . \qquad (31)$$

For example, at $V_{imH}=375$ V, $V_{B\max}=400$ V, and $N_R=N_P$, it follows from (31) that $N_1+N_2\geq 0.9\cdot N_P$.

After selecting the sum N_1+N_2, the value of N_1 should be determined from the trade-off between direct energy transfer and, therefore, higher efficiency (larger N_1), and zero-crossing distortion of the line current, associated with lower power factor and higher total harmonic distortion (smaller N_1). In fact, N_1 should be selected as large as possible to achieve higher efficiency and still to satisfy the line-current harmonic standards such as, for example, IEC 1000-3-2 [10].

C. *Design Example*

The design procedure is illustrated on the example of a 5 V/20 A, universal line-voltage range (90-265 V_{rms}) S^{4}ICS forward converter. Maximum bulk-capacitor voltage $V_{B\max}=400$ V was specified.

First, $N_S=3$, is selected, which is the typical number of secondary turns in computer power supplies with multi outputs. Number of primary turns, N_P, should be as large as possible, to maximize efficiency. However, the maximum N_P is determined from the requirement that $D_{\max}<0.5$ at low line. To minimize the voltage stress on the switch, $N_R=N_P$ is selected since $D_{\max}\approx 0.5$. According to the considerations in the previous section, $N_1+N_2=N_P-2$ is selected, which,

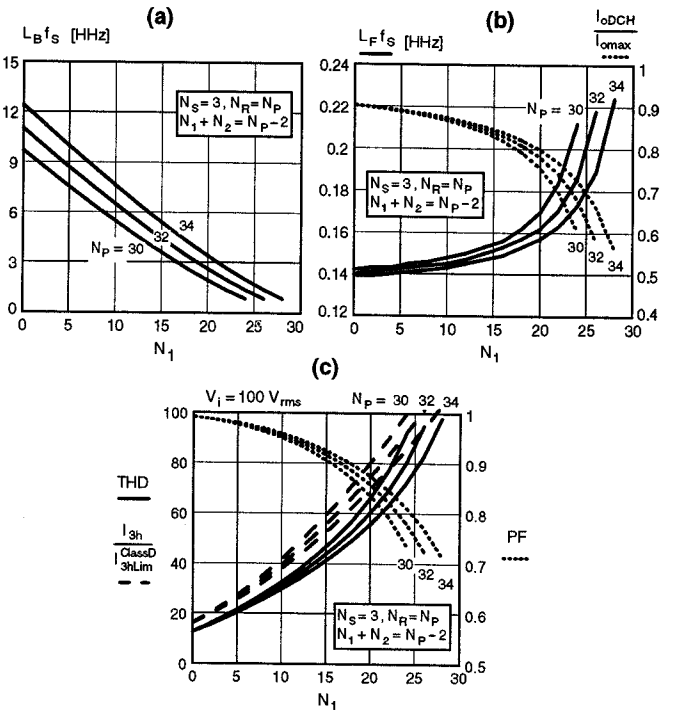


Fig. 4 Design curves for DCM operation of boost inductor ($V_o=5$ V, $I_{omax}=20$ A)

from (29), yields $V_{B\min}=131$ V ($V_F=0.55$ V). Therefore, a possible range of N_P is $N_P=30$–34, which results in $D_{\max}=0.42$–0.48. For the selected values, design curves are presented in Fig. 4. As can be seen from Figs. 4(a) and (b), with increasing N_1, the product L_Bf_S is decreasing and product L_Ff_S is increasing. (Equivalently, with increasing L_Ff_S, the ratio I_{oDCH}/I_{omax}, which represents the DCM-CCM boundary of L_F at high line, is decreasing, i.e., L_F operates in CCM in a wider range of the output current.) Also, with increasing N_1, the total harmonic distortion, *THD*, of the line current is increasing and the power factor, *PF*, is decreasing. Figure 4(c) also shows the third harmonic of the line current (which is the most critical harmonic) relative to the IEC 1000-3-2, Class-D limit [10]. The curves in Fig. 4(c) are obtained for $V_{i,rms}=100$ V, at full load. (The limits for $V_{i,rms}=100$ V are calculated by multiplying the $V_{i,rms}=230$ V limits with 230/100=2.3.) The corresponding curves for $V_{i,rms}=230$ V are almost identical to the curves in Fig. 4(c). Line current waveforms for four different values of N_1 and $N_P=34$ (as example), at $V_{i,rms}=100$ V and 230 V are given in Fig. 5. As can be seen, the line current has almost identical waveforms at low line and high line. In Fig. 5, the IEC 1000-3-2, Class-D envelopes as well as the ideal, sinusoidal line current waveform are also shown. To keep the third harmonic below, e.g., 80% of the IEC 1000-3-2, Class-D limit, it follows from Fig. 4(c) that N_1 should be smaller than 22, 21, and 20 for $N_P=34$, 32, and 30, respectively. A good design compromise is to select $N_P=34$ (for higher efficiency), $N_1=20$ and $N_2=12$. Then, from Figs. 4(a) and (b), $L_Bf_S=3.4$

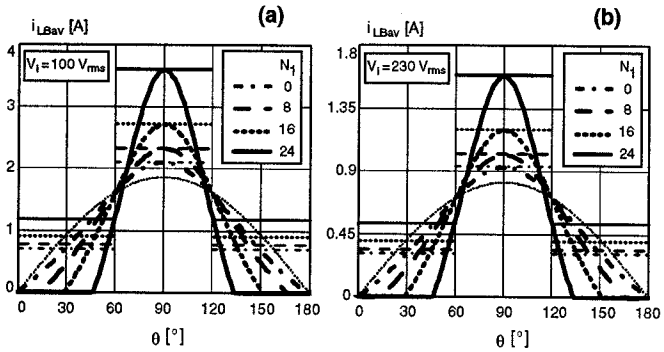


Fig. 5 Line current waveforms in DCM operation of boost inductor (V_o = 5 V, I_{omax} = 20 A, N_S=3, N_P=N_R=34, N_1+N_2=32)

HHz and $L_F f_S$ = 0.157 HHz (e.g., selecting f_S = 75 kHz yields L_B = 45 μH and L_F = 2.1 μH); which results in THD = 55.5%, $I_{3h}/I_{3h\text{Lim}} \approx 70\%$, and PF = 0.875.

III. CCM Operation of Boost Inductor

A. Analysis

For CCM operation of the boost inductance, it is necessary to have a substantial inductance connected in series with winding N_1 or winding N_2. The additional inductance can be either the leakage inductance of the winding (achieved with an appropriate transformer structure) or an external inductance. This inductance provides the variable duty cycle for L_B to operate in CCM. Key waveforms which illustrate principle of operation are given in Fig. 6 for the case of $L_1 >> L_2$. After switch SW is turned on at the beginning of a switching cycle, the boost inductor current, i_{LB}, starts to commutate from winding N_2 (current i_2) to winding N_1 (current i_1). Because of inductance L_1, the slope of current i_1 is limited,

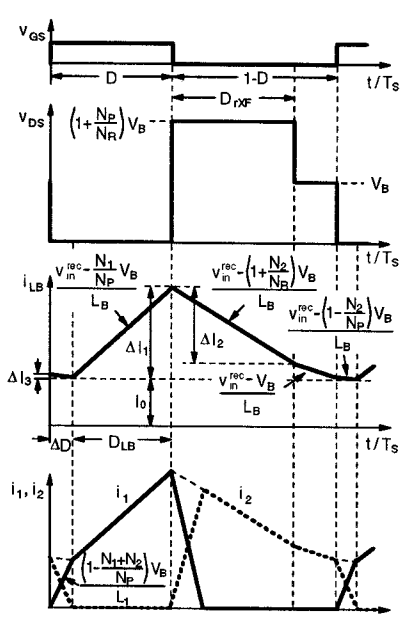


Fig. 6 Key waveforms in CCM operation of boost inductor

$$\frac{di_1}{dt} = \frac{\left(1-\frac{N_1+N_2}{N_P}\right)V_B}{L_1}, \tag{32}$$

and the commutation cycle, ΔD, is not negligible compared to duty cycle D. As can be seen from Fig. 6, because of ΔD, the effective duty cycle "seen" by the boost inductor is reduced,

$$D_{LB} = D - \Delta D . \tag{33}$$

Commutation cycle ΔD can be obtained from the flux balance of L_B, i.e.,

$$\frac{v_{in}^{rec} - \frac{N_1}{N_P}\cdot V_B}{1+\frac{L_1}{L_B}}\cdot(D-\Delta D) = \left[\left(1+\frac{N_2}{N_R}\right)\cdot V_B - v_{in}^{rec}\right]\cdot\frac{N_R}{N_P}\cdot D$$
$$+\left(V_B - v_{in}^{rec}\right)\cdot\left(1-D-\frac{N_R}{N_P}D\right)+\left(V_B\left(1-\frac{N_2}{N_P}\right)-v_{in}^{rec}\right)\cdot\Delta D . \tag{34}$$

After a few simple algebraic operations, ΔD is obtained as

$$\Delta D = D - \frac{\left(1+\frac{L_1}{L_B}\right)\cdot\left(1-\frac{v_{in}^{rec}}{V_B}\right)}{1-\frac{N_1+N_2}{N_P}+\frac{L_1}{L_B}\cdot\left(1-\frac{N_2}{N_P}-\frac{v_{in}^{rec}}{V_B}\right)} . \tag{35}$$

As can be seen from (35), the effective duty cycle "seen" by the boost inductor is

$$D_{LB} = D - \Delta D \sim 1-\frac{v_{in}^{rec}}{V_B}, \tag{36}$$

which corresponds to the conventional CCM boost ICS. Note that D_{LB} is approximately equal to $\left(1-v_{in}^{rec}/V_B\right)$ at $L_1 << L_B$ and $N_1 = 0, N_2 = 0$.

To achieve CCM operation of L_B, ΔD must be greater than zero or equal to zero. From (35), it follows that

$$v_{in}^{rec} \geq \left(1-\frac{1-\frac{N_1}{N_P}-\left(1+\frac{L_1}{L_B}\right)\cdot\frac{N_2}{N_P}}{1+\frac{L_1}{L_B}\cdot(1-D)}\cdot D\right)\cdot V_B . \tag{37}$$

Therefore, the boundary angle between DCM and CCM operations of L_B is defined as

$$\theta_{bc} = a\sin\left[\left(1-\frac{1-\frac{N_1}{N_P}-\left(1+\frac{L_1}{L_B}\right)\cdot\frac{N_2}{N_P}}{1+\frac{L_1}{L_B}\cdot(1-D)}\cdot D\right)\cdot\frac{V_B}{V_{im}}\right] . \tag{38}$$

In CCM, the average boost inductor current is determined as (see Fig. 6)

$$i_{LBav}^{CCM} = I_0 + \frac{D + D_{rXF} - \Delta D}{2} \cdot \Delta I_1 + \frac{1-D}{2} \cdot (\Delta I_1 - \Delta I_2)$$

$$+ \frac{1 - D - D_{rXF} + \Delta D}{2} \cdot \Delta I_3 \ , \qquad (39)$$

where

$$I_0 = \frac{\left(1 - \frac{N_1 + N_2}{N_P}\right) \cdot V_B}{L_1 f_S} \cdot \Delta D \ , \qquad (40)$$

$$\Delta I_1 = \frac{v_{in}^{rec} - \frac{N_1}{N_P} \cdot V_B}{(L_B + L_1) f_S} \cdot (D - \Delta D) \ , \qquad (41)$$

$$\Delta I_2 = \frac{\left(1 + \frac{N_2}{N_R}\right) \cdot V_B - v_{in}^{rec}}{L_B f_S} \cdot D_{XF} \ , \qquad (42)$$

$$\Delta I_3 = \frac{\left(1 - \frac{N_2}{N_P}\right) \cdot V_B - v_{in}^{rec}}{L_B f_S} \cdot \Delta D \ . \qquad (43)$$

Substituting (9), (35), and (40)-(43) into (39), after a number of simple algebraic operations, the average boost inductor current in CCM is obtained as

$$i_{LBav}^{CCM} = \frac{V_B}{L_1 f_S}\left(1 - \frac{N_1 + N_2}{N_P}\right)\left[D - \frac{\left(1 + \frac{L_1}{L_B}\right)\cdot\left(1 - \frac{v_{in}^{rec}}{V_B}\right)}{C_2 - \frac{L_1}{L_B}\frac{v_{in}^{rec}}{V_B}}\right]$$

$$+ \frac{V_B}{2 L_B f_S}\left[C_0 + \frac{\left(1 - \frac{v_{in}^{rec}}{V_B}\right)\cdot\left(\frac{v_{in}^{rec}}{V_B} + C_1\right)}{C_2 - \frac{L_1}{L_B}\frac{v_{in}^{rec}}{V_B}}\right] , \qquad (44)$$

where

$$C_0 = -2D\left(1 - \frac{N_R + N_P}{2N_P} D\right) \cdot \frac{N_2}{N_P} \ , \qquad (45)$$

$$C_1 = -\frac{N_1}{N_P} + \frac{N_2}{N_P}\left(1 + \frac{L_1}{L_B}\right) , \qquad (46)$$

and

$$C_2 = 1 - \frac{N_1 + N_2}{N_P} + \frac{L_1}{L_B}\left(1 - \frac{N_2}{N_P}\right) . \qquad (47)$$

For further calculations, it is convenient to rewrite (44) in the following form:

$$i_{LBav}^{CCM} = \frac{K_{L1}^{CCM}}{L_1 f_S} + \frac{K_{LB}^{CCM}}{L_B f_S} \ . \qquad (48)$$

During a half of a line cycle, before entering CCM, the boost inductor operates in two DCMs, as described in Section II. Following the same derivation procedure as in Section II, the average boost inductor current in the two DCMs is obtained as

$$i_{LBav}^{DCMa} = \frac{V_B D^2}{2 L_B f_S} \cdot \frac{A_1 + A_2 \frac{v_{in}^{rec}}{V_B} + \frac{L_1}{L_B}\left(A_3 + A_4 \frac{v_{in}^{rec}}{V_B} - \left(\frac{v_{in}^{rec}}{V_B}\right)^2\right)}{\left(1 + \frac{L_1}{L_B}\right)^2 \left(1 + \frac{N_2}{N_R} - \frac{v_{in}^{rec}}{V_B}\right)} \qquad (49)$$

where A_1 and A_2 are defined in (7), and

$$A_3 = -\left(1 + \frac{N_2}{N_R}\right)\frac{N_1}{N_P} \ , \quad A_4 = 1 + \frac{N_1}{N_P} + \frac{N_2}{N_R} \ , \qquad (50)$$

whereas

$$i_{LBav}^{DCMb} = \frac{V_B D^2}{2 L_B f_S} \cdot \frac{B_1 + B_2 \frac{v_{in}^{rec}}{V_B} + \frac{L_1}{L_B}\left(B_3 + B_4 \frac{v_{in}^{rec}}{V_B}\right)}{\left(1 + \frac{L_1}{L_B}\right)^2 \left(1 - \frac{v_{in}^{rec}}{V_B}\right)} \ , \qquad (51)$$

where B_1 and B_2 are defined in (14) and (15), respectively, and

$$B_3 = \frac{N_1}{N_P}\left(\frac{2N_2}{N_P} - 1\right) + \frac{(N_2 + N_R) N_2}{N_P^2}\left(2 + \frac{L_1}{L_B}\right) , \qquad (52)$$

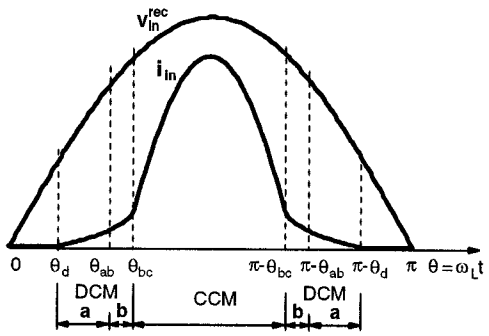
$$B_4 = 1 - \frac{3N_2}{N_P} - \frac{N_2 N_R}{N_P^2}\left(2 + \frac{L_1}{L_B}\right) + \frac{N_1 - N_2}{N_P}\frac{L_1}{L_B} \ . \qquad (53)$$

For further calculations, it is convenient to rewrite (49) and (51) as

$$i_{LBav}^{DCMa} = \frac{K_{LB}^{DCMa}}{L_B f_S} \quad \text{and} \quad i_{LBav}^{DCMa} = \frac{K_{LB}^{DCMb}}{L_B f_S} \ . \qquad (54)$$

Finally, the boundary angle between **DCMa** and **DCMb** is defined as

$$\theta_{ab} = a\sin\left(\frac{N_1 + (N_2 + N_R)\left(1 + \frac{L_1}{L_B}\right)}{N_P + N_R\left(1 + \frac{L_1}{L_B}\right)} \cdot \frac{V_B}{V_{im}}\right) . \qquad (55)$$



The operation modes of the CCM boost inductor are summarized in Fig. 7. A typical line current waveform is also shown in Fig. 7. The zero-crossing angle (dead angle), θ_d, is defined in (18).

B. Design

The design goal is, as already described in Section II, to keep energy-storage-capacitor voltage V_B between a maximum value, $V_{B\max}$, and a minimum value, $V_{B\min}$. The design parameters are L_B, L_1, L_F, N_P, N_R, N_S, N_1, and N_2.

Voltage V_B can be obtained from the input-output power balance. Using (48) and (54), the input-output power balance can be written as

$$\frac{1}{L_B f_S}\cdot\left(\frac{2}{\pi}\int_{\theta_d}^{\theta_{ab}} K_{LB}^{DCMa}\, v_{in}^{rec}\, d\theta+\frac{2}{\pi}\int_{\theta_{ab}}^{\theta_{bc}} K_{LB}^{DCMb}\, v_{in}^{rec}\, d\theta\right.$$
$$\left.+\frac{2}{\pi}\int_{\theta_{bc}}^{\pi/2} K_{LB}^{CCM}\, v_{in}^{rec}\, d\theta\right)+\frac{1}{L_1 f_S}\cdot\left(\frac{2}{\pi}\int_{\theta_{bc}}^{\pi/2} K_{L1}^{CCM}\, v_{in}^{rec}\, d\theta\right)$$
$$=\frac{V_o I_o}{\eta}\,. \qquad (56)$$

Voltage $V_B = V_{B\max}$ at high line, when L_F operates at the DCM-CCM boundary at output current $I_{oDCH} \le I_{o\max}$. Substituting (1), (49), (7), (50), (51), (14), (15), (52), (53), and (44)-(47) into (56) at high line, the input-output power balance yields

$$\frac{K_{LBH}}{L_B f_S}+\frac{K_{L1H}}{L_1 f_S}=\frac{V_o I_{oDCH}}{\eta_H}\,, \qquad (57)$$

where K_{LBH} and K_{L1H} represent the expressions in the first and second parenthesis on the left side of Eq. (56); I_{oDCH} is defined with (20) and (21).

Voltage $V_B = V_{B\min}$ at low line and full load, when L_F operates in CCM. $V_{B\min}$ should be defined to be slightly higher than V_{imL} (e.g., $V_{B\min} = V_{imL} + 1$), if it is not limited by the maximum duty cycle. Also, $V_{B\min}$ has to satisfy (37). It can be easily shown that after substituting (20) into (37), a quadratic equation is obtained, which shows the range of possible values of $V_{B\min}$.

Writing $I_o = I_{o\max}$ in (56) and substituting (1), (49), (7), (50), (51), (14), (15), (52), (53), and (44)-(47) into (56) at low line, the input-output power balance yields

$$\frac{K_{LBL}}{L_B f_S}+\frac{K_{L1L}}{L_1 f_S}=\frac{V_o I_{o\max}}{\eta_L}\,, \qquad (58)$$

Using (58), for a selected ratio of inductances, L_1/L_B, the product of inductance L_1 and switching frequency f_S is obtained as

$$L_1 f_S = \eta_L \frac{K_{L1L}+\frac{L_1}{L_B}K_{LBL}}{V_o I_{o\max}}\,. \qquad (59)$$

Further, substituting (20), (21), and (59) into (57), the product of forward inductance L_F and switching frequency f_S is obtained as

$$L_F f_S = \frac{\eta_L}{2\eta_H}\frac{K_{L1L}+\frac{L_1}{L_B}K_{LBL}}{K_{L1H}+\frac{L_1}{L_B}K_{LBH}}(V_o+V_F)\left(1-\frac{N_P}{N_S}\frac{V_o+V_F}{V_{B\max}}\right) \qquad (60)$$

From (59) and (60), for selected values of N_P, N_R, N_S, N_1, and N_2, and for selected switching frequency f_S, the inductances L_1, L_B, and L_F will be determined. The values of N_P, N_R, and N_S should be selected as for the conventional dc-dc forward converter. Finally, N_1 and N_2, should be selected according to the following considerations.

Applying the condition for CCM operation of L_B at high line, from (37) the maximum value of $N_1 + N_2$ can be obtained as

$$\frac{N_1+N_2}{N_P}+\frac{L_1}{L_B}\frac{N_2}{N_P} < 1-\frac{1+\frac{L_1}{L_B}(1-D_{\min})}{D_{\min}}\left(1-\frac{V_{imH}}{V_{B\max}}\right) \qquad (61)$$

Note that for $L_1 << L_B$, (61) has the same form as (27) with the opposite unequal sign. The minimum value of $N_1 + N_2$ is zero. In fact, it follows from (35) and (36) that the CCM operation of L_B best corresponds to the conventional boost ICS at $N_1 = 0$ and $N_2 = 0$. Therefore, N_1 and N_2 should be finally selected from the trade-off between circuit efficiency and line current distortion.

C. Design Example

As in Section II, $N_S = 3$, $N_P = N_R = 34$ are selected. Further, $V_{B\min} = 130$ V is chosen, which yields $D_{\max} = 0.485$. According to (61), $N_1+N_2 \le 20$ at $L_1 << L_B$, and $N_1+2N_2 \le 9$ at the other extreme case, $L_1 = L_B$. For the selected values of N_S, N_P, and N_R, design curves are shown in Fig. 8. As can be seen, with increasing N_1 and increasing N_2 the products $L_1 f_S$ and $L_B f_S$ are decreasing and product $L_F f_S$ is increasing. (Equivalently, with increasing $L_F f_S$, the ratio $I_{oDCH}/I_{o\max}$ is

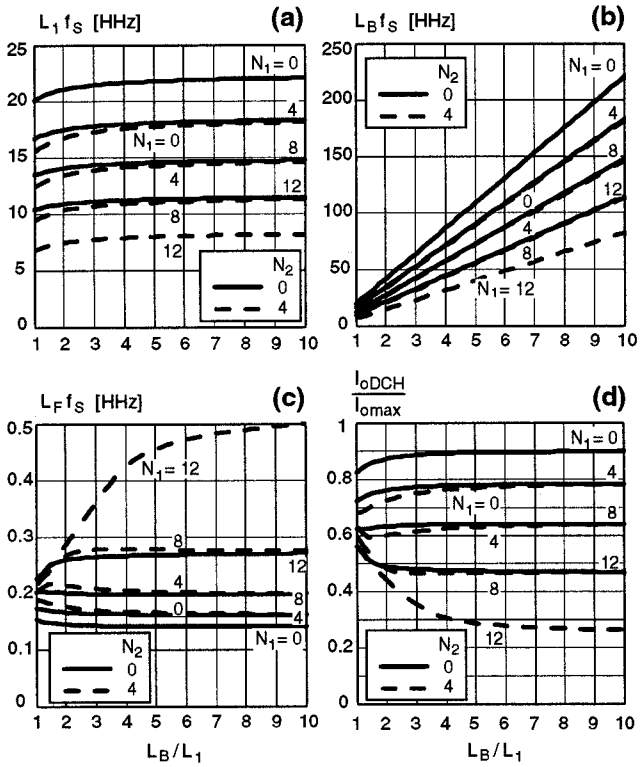


Fig. 8 Design curves for CCM operation of boost inductor
($V_o = 5$ V, $I_{omax} = 20$ A, $N_S = 3$, $N_P = N_R = 34$)

decreasing, which means that L_F operates in CCM in a wider range of the output current.) Also, according to (35) and (36), as N_1 and N_2 increase, the total harmonic distortion of the line current is increasing and the power factor is decreasing (not shown in Fig. 8). Line current waveforms for $N_1 = N_2 = 0$ and $L_B/L_1 = 1.5$, as example, at $V_{i,rms} = 100$ V and 230 V are shown in Fig. 9. The IEC 1000-3-2, Class-D envelopes and the ideal, sinusoidal line current waveform are also shown in Fig. 9. Unlike in the case of the DCM operation, where the line current waveforms at high line and low line are almost identical, in the CCM operation, the line current waveform at high line is significantly distorted compared to that at low line. As a result, the line current waveform in Fig. 9(b) has a reduced margin with respect to the IEC 1000-3-2, Class-D limits. ($THD = 76\%$, $I_{3h}/I_{3h\text{Lim}} \approx 79\%$, $I_{5h}/I_{5h\text{Lim}} \approx 86\%$, $I_{7h}/I_{7h\text{Lim}} \approx 93\%$, $I_{9h}/I_{9h\text{Lim}} \approx 87\%$, and $PF = 0.8$). In fact, the line current is distorted at high line because of the narrow CCM range of L_B; the boundary angle between DCM and CCM operations of L_B is $\theta_{bc} = 69°$. To reduce θ_{bc} at high line, $D_{\min}$ needs to be increased, as follows from (38). Therefore, $N_R < N_P$ should be selected. However, a larger unbalance between N_R and N_P is not desirable because of the increased voltage stress on the switch and the forward diode. Therefore, transformer reset techniques which allow for a larger maximum duty cycle with reasonable stress on the semiconductor components are more suitable for implementation of the forward S^4ICS operating in CCM.

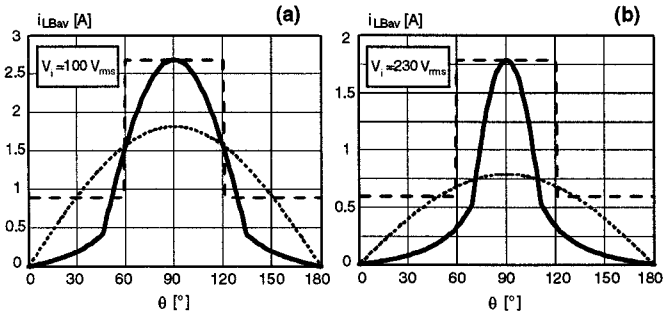


Fig. 9 Line current waveforms in CCM operation of boost inductor
($V_o = 5$ V, $I_{omax} = 20$ A, $N_S = 3$, $N_P = N_R = 34$, $N_1 = N_2 = 0$, $L_B/L_1 = 1.5$)

IV. SUMMARY

A complete design-oriented analysis of the single-stage, single-switch input current shaper which combines the boost-like front end with a dc/dc forward converter is presented. Design equations are derived for both the discontinuous and continuous conduction modes of operation of the boost inductor. The design procedure is demonstrated on a 5 V/20 A, universal line-voltage range (90-265 V_{rms}) converter.

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