A New Three-Level Soft-Switched Converter

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Abstract — **A three-level, constant-frequency, isolated converter which employs a coupled inductor to achieve zero-voltage switching (ZVS) of the primary switches in the entire line and load range is described. Because the coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifiers. The operation and performance of the proposed converter was verified on a 1-kW prototype.**

I. INTRODUCTION

In recent years, multilevel power converters have received a lot of attention due to their suitability for applications with high input voltages [1]. Specifically, multilevel inverters and dc-dc converters can be implemented with semiconductor switches rated at a fraction of the input voltage, which are typically less expensive and more efficient than their high-voltage-rated counterparts. Because the implementation complexity of multilevel converters is increased dramatically by the number of levels, which diminishes the benefits of multilevel conversion, the majority of development efforts in dc-dc multilevel conversion have been focused on three-level converters.

Generally, three-level dc-dc converters feature power conversion with semiconductor switches rated at one-half of the input voltage. Various isolated implementations of three-level dc-dc converters have been described in [2] – [5]. To further enhance their performance, all of these four-primary-switch implementations feature soft switching of all primary switches. Specifically, the implementations in [2] – [4] offer ZVS, whereas the implementation in [5] features ZVS and zero-current switching (ZCS). The major difference among the implementations described in [2] - [5] is in the control of the switches [6]. The implementations in [2] and [3] utilize constant frequency PWM control, whereas the implementations in [4] and [5] employs constant-frequency phase-shift control.

Generally, the major deficiencies of the ZVS implementations described in [2] - [4] are brought about by an increased inductance in the primary circuit that is required to achieve a complete ZVS of all primary switches down to light loads. This inductance, which is obtained by intentionally increasing leakage inductance of the transformer and/or by adding an external inductance in series with the primary of the transformer, has a detrimental effect on the performance. It introduces a circulating current on the primary side, causes a secondary-side loss of duty cycle, and produces severe parasitic ringing on the secondary side of the transformer as it resonates with the rectifier's junction capacitance.

The circulating current caused by excessive energy stored in the inductance employed to extend the ZVS range down to light loads increases the current stress of the primary switches and the primary-side conduction losses at heavy load. The primary-side conduction losses are further increased due to the secondary side duty cycle loss which must be compensated by reducing the turns ratio of the transformer. Furthermore, a smaller turns ratio of the transformer also increases the voltage stress on the secondary-side rectifiers so that rectifiers with a higher voltage rating that typically exhibit a higher conduction loss may be required. Finally, to control the ringing voltage across the output rectifiers, a lossy snubber circuit is required on the secondary side which also reduces the conversion efficiency.

In this paper, a new three-level ZVS converter is introduced. The proposed three-level ZVS converter employs a coupled inductor on the primary side to achieve ZVS in the entire line and load range. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output diode. As a result, the proposed circuit exhibits an increased conversion efficiency.

The performance of the proposed three-level converter circuit was experimentally verified on a 1-kW prototype circuit that was designed to operate from a 750 V_{DC} input and deliver 48 V_{DC} output voltage.

II. THREE-LEVEL ZVS CONVERTER WITH COUPLED INDUCTOR

Figure 1 shows a circuit diagram of the proposed three-level soft-switched dc-dc converter that employs a coupled inductor on the primary side to extend the ZVS range of the primary switches with a minimum circulation energy and conduction loss. The three-level converter in Fig. 1 consists of a series connection of four primary switches Q_1 through Q_4, rail-splitting capacitors C_{IN1} and C_{IN2}, "flying capacitors" C_{S1} and C_{S2}, isolation transformer TR, and coupled inductor L_C. In this circuit, the load is coupled to the converter through a full-wave rectifier connected to the center-tapped secondary of the transformer. In addition, clamping diodes D_{C1} and D_{C2} are used to clamp the voltage of outer switches Q_1 and Q_4, respectively, to $V_{IN}/2$ after the switches are turned off. Finally, blocking capacitor C_B is employed to prevent

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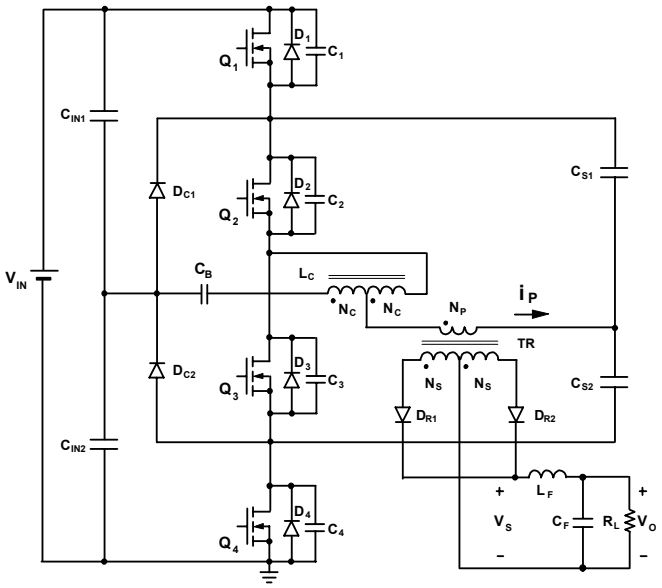


Fig. 1. Proposed three-level ZVS converter with coupled inductor.

transformer saturation in case of a volt-second imbalance on the transformer windings that may be generated by circuit parasitics, a mismatching of the switch components' characteristics, and timing signals.

To facilitate the explanation of operation of the circuit in Fig. 1, Fig. 2 shows its simplified circuit diagram. In the simplified circuit, it is assumed that inductance of output filter L_F is large enough so that during a switching cycle the output filter can be modeled as a constant current source with

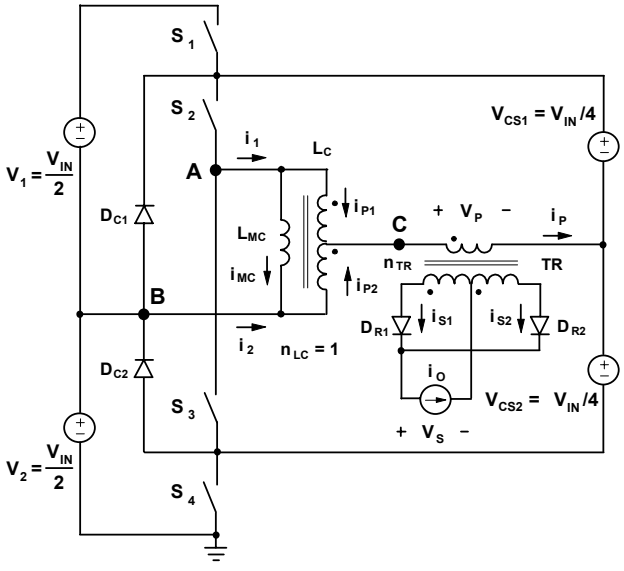


Fig. 2. Simplified circuit diagram of proposed three-level ZVS converter showing reference directions of currents and voltages.

the magnitude equal to output current I_O. Also, it is assumed that the capacitances of capacitors C_{IN1} and C_{IN2}, which form a capacitive divider that splits the input voltage in half, are large so that capacitors C_{IN1} and C_{IN2} can be modeled by voltage sources $V_1=V_{IN}/2$ and $V_2=V_{IN}/2$, respectively. Similarly, it is assumed that the capacitances of capacitors C_{S1} and C_{S2} are large enough so that the capacitors can be modeled as constant voltage sources V_{CS1} and V_{CS2}, respectively. Because the average voltages of the coupled inductor windings and the transformer windings during a switching cycle are zero and for the phase-shift control the outer pair of switches and the inner pair of switches operate with 50% duty cycle, the magnitude of voltage sources V_{CS1} and V_{CS2} in Fig. 2 is equal to $V_{IN}/4$, i.e., $V_{CS1}=V_{CS2}=V_{IN}/4$.

To further simplify the analysis of operation of the circuit in Fig. 1, it is also assumed that the resistance of the conducting semiconductor switches is zero, whereas the resistance of the non-conducting switches is infinite. In addition, the leakage inductances of both transformer TR and coupled inductor L_C, as well as the magnetizing inductance of transformer TR are neglected since their effect on the operation of the circuit is not significant. However, the magnetizing inductance of coupled inductor L_C and output capacitances $C_1 – C_4$ of primary switches are not neglected in this analysis since they play a major role in the operation of the circuit. Consequently, in Fig. 2, coupled inductor L_C is modeled as the ideal transformer with turns ratio $n_{LC}=1$ and with parallel magnetizing inductance L_{MC} across the series connection of windings AC and CB, whereas transformer TR is modeled only by the ideal transformer with turns ratio n_{TR}. It should be noted that magnetizing inductance L_{MC} of inductor L_C represents the inductance measured between terminals A and B with terminal C open.

With reference to Fig. 2, the following relationships between currents can be established:

$$i_P = i_{P1} + i_{P2}\,, \tag{1}$$

$$i_1 = i_{P1} + i_{MC}\,, \tag{2}$$

$$i_2 = i_{P2} - i_{MC}\,. \tag{3}$$

Since the number of turns of winding AC and winding CB of coupled inductor L_C are the same, it must be that

$$i_{P1} = i_{P2}\,. \tag{4}$$

Substituting Eq. (4) into Eqs. (1)-(3) gives

$$i_{P1} = i_{P2} = \frac{i_P}{2}\,, \tag{5}$$

$$i_1 = \frac{i_P}{2} + i_{MC}\,, \tag{6}$$

$$i_2 = \frac{i_P}{2} - i_{MC}\,. \tag{7}$$

As can be seen from Eqs. (6) and (7), currents i_1 and i_2 are composed of two components: primary-current component $i_P/2$ and magnetizing-current component i_{MC}. The primary-current component directly depends on the load current, whereas the magnetizing current does not directly depend on

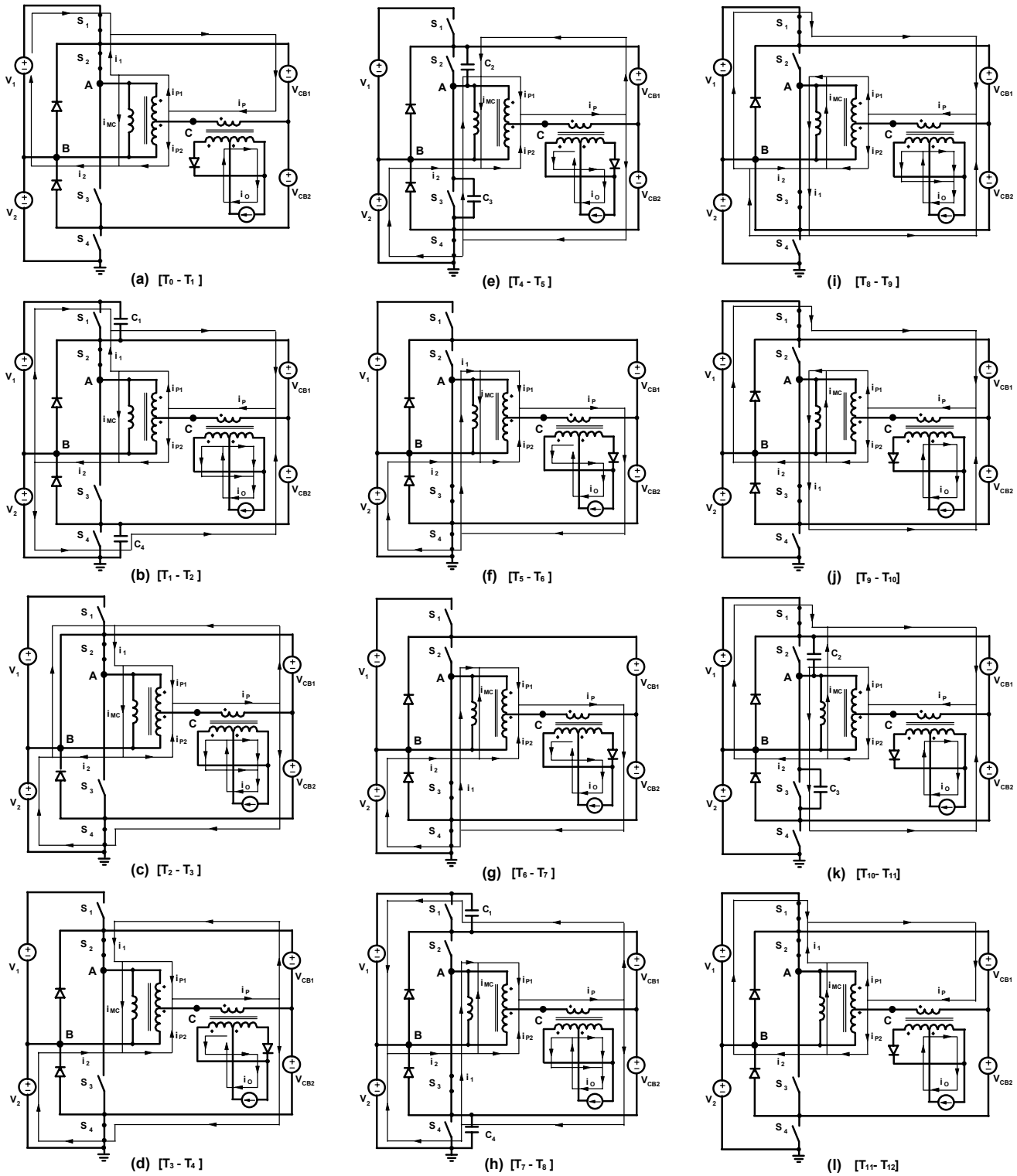


Fig. 3. Topological stages of proposed three-level ZVS converter power stage.

the load, but rather on the volt-second product across the magnetizing inductance. Namely, a change of the magnetizing current with a change in the load current occurs only if the phase shift between the turn on instants of outer switches S_1 and S_4 and respective inner switches S_2 and S_3 is changed to maintain the output regulation. Usually, the change of phase shift with a load change is greater at light loads, i.e., as the load decreases toward no load than at

heavier loads. Since in the circuit in Fig. 1 the phase shift increases as the load approaches zero, the volt-second product of L_{MC} also increases so that the circuit in Fig. 1 exhibits the maximum magnetizing current at no load, which makes it possible to achieve ZVS at no load.

Because magnetizing current i_{MC} does not contribute to the load current, as seen in Fig. 2, it represents a circulating current. Generally, this circulating current and its associated energy should be minimized to reduce losses and maximize the conversion efficiency. Due to an inverse dependence of the volt-second product of L_{MC} on the load current, circuit in Fig. 1 circulates less energy at full load than at light load, and, therefore, features ZVS in a wide load range with a minimum circulating current.

Also from Fig. 2 it can be seen that

$$v_{AB} = v_{AC} + v_{CB} . \quad (8)$$

Since both windings of coupled inductor L_C have the same number of turns, i.e., since the turns ratio of L_C is n_{LC}=1, it must be that

$$v_{AC} = v_{CB} , \quad (9)$$

or

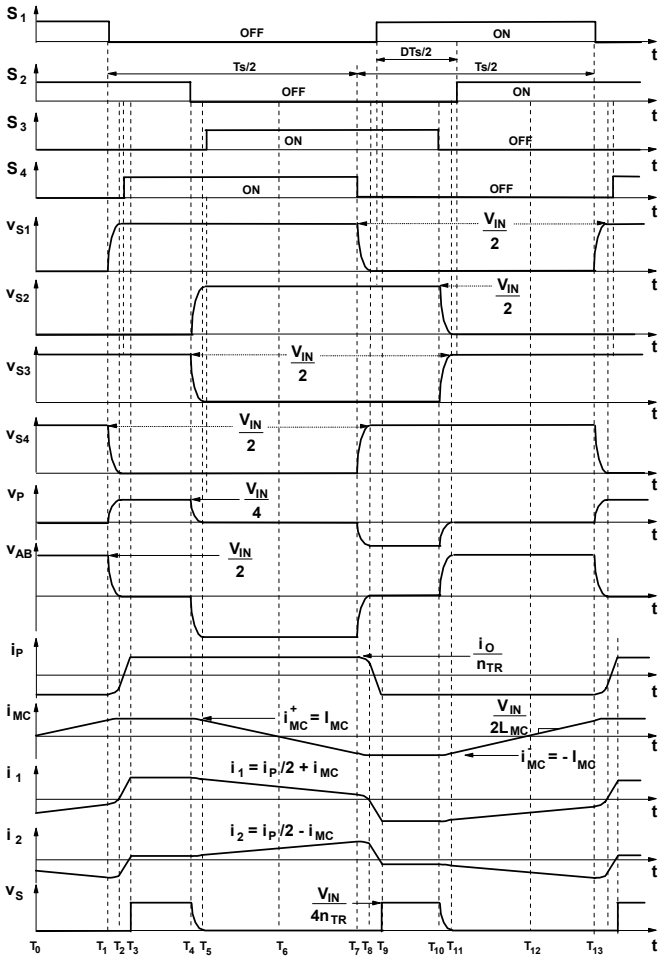


Fig. 4. Key waveforms of proposed three-level ZVS converter.

$$v_{AC} = v_{CB} = \frac{v_{AB}}{2} . \quad (10)$$

Generally for constant-frequency phase-shift control, voltage v_{AB} is a squarewave voltage consisting of alternating positive and negative pulses of magnitude $V_{IN}/2$ that are separated by time intervals with v_{AB}=0. According to Eq. (10) and with reference to Fig. 2, during the time intervals when either of inner switches S_2 and S_3 is closed and when v_{AB}=0, the primary voltage magnitude is $|v_P|=V_{IN}/4$, whereas during time intervals when $|v_{AB}|=V_{IN}/2$, the primary voltage magnitude is $|v_P|$=0.

To further facilitate the analysis of operation, Fig. 3 shows the topological stages of the converter during a switching cycle, whereas Fig. 4 shows key waveforms. As shown in Fig. 4, since during time interval T_0-T_1 switches S_1 and S_2 are closed while switches S_3 and S_4 are open, voltage $v_{AB}=V_1=V_{IN}/2$ so that primary voltage v_P=0. In addition, during this topological stage, whose equivalent circuit is shown in Fig. 3(a), output current I_O flows through output rectifier D_{R2} and the corresponding secondary of the transformer so that primary current $i_P= -I_O/n_{TR}$, where $n_{TR}=N_P/N_S$ is the turns ratio of the transformer, N_P is the number of primary winding turns, and N_S is the number of secondary winding turns. Because the primary current is negative, both currents i_1 and i_2 are also negative as shown in Fig. 4. At the same time, magnetizing current i_{MC} is linearly increasing with slope $V_{IN}/(2L_{MC})$, since voltage v_{AB} is positive and equal to half of the input voltage, i.e., $v_{AB}=V_{IN}/2$. As a result, current i_1 increases while current i_2 decreases. During this interval, voltage v_S which is equal to the secondary winding voltage is zero because primary winding voltage v_P is zero. This stage ends at $t=T_1$ when switch S_1 is turned off.

After switch S_1 is turned off at $t=T_1$, the current which was flowing through the transistor of switch S_1 is diverted to switch's output capacitance C_1, as shown in Fig. 3(b). In this topological stage, current i_2 charges capacitor C_1 and discharges capacitor C_4 at the same rate since the sum of the voltages across capacitors C_1 and C_4 is equal to constant voltage $V_{IN}/2$. As a result, voltage across switch S_1 increases while voltage across switch S_4 decreases, as illustrated in Fig. 4. In addition, during this stage the potential of point A decreases causing a decrease of voltage v_{AB} from $V_{IN}/2$ toward zero and the simultaneous increase of primary voltage v_P from zero toward $V_{IN}/4$, as illustrated in Fig. 4. The positive primary voltage initiates the commutation of output current I_O from rectifier D_{R2} to rectifier D_{R1}. Since the leakage inductance of transformer TR neglected, this commutation is instantaneous. However, in the presence of leakage inductance, the commutation of current from one rectifier to the other takes time. Because during this commutation time both rectifiers are conducting, i.e., the secondary windings of the transformer are shorted, voltage v_S is zero, as shown in Fig. 4.

After capacitor C_4 is fully discharged at $t=T_2$, i.e., after voltage v_{S4} reaches zero, current i_2 continues to flow through antiparallel diode D_4 of switch S_4 and clamp diode D_{C1} instead of through capacitors C_1 and C_4, as shown in Fig. 3(c). Due to positive voltage $V_{IN}/4$ applied across primary winding N_P, currents i_P, i_1, and i_2 begin to increase from negative to positive direction. To achieve ZVS of switch S_4, switch S_4 needs to be turned on during the time interval when its antiparallel diode D_4 is conducting, as illustrated in Fig. 4. The stage in Fig. 3(c) ends at $t=T_3$ when the output current I_O is completely commutated from rectifier D_{R2} to rectifier D_{R1}, i.e., when primary current i_P equals to I_O/n_{TR}.

During time interval $T_3 - T_4$ current i_1, which flows through closed switch S_2, is supplied from voltage source V_{CS1}, whereas current i_2, which flows through closed switch S_4, is supplied from voltage source V_2, as shown in Fig. 3(d). The stage in Fig. 3(d) ends at $t=T_4$ when switch S_2 is turned off. After switch S_2 is turned off, the current which was flowing through the transistor of switch S_2 is diverted to its output capacitance C_2, as shown in Fig. 3(e). In this topological stage, current i_1 charges capacitor C_2 and discharges capacitor C_3 at the same rate since the sum of the voltages across capacitors C_2 and C_3 is equal to constant voltage $V_{CS1}+V_{CS2}=V_{IN}/2$. As a result, voltage across switch S_2 increases while voltage across switch S_3 decreases, as illustrated in Fig. 4. At the same time, the potential of point A starts to decrease and it causes a simultaneous decrease of voltage v_{AB} from zero toward $-V_{IN}/2$ and primary voltage v_P from $V_{IN}/4$ toward zero, as illustrated in Fig. 4. Since the decrease of the primary voltage is reflected into the secondary voltage, voltage v_S also decreases toward zero as shown in Fig. 4. This stage ends at $t=T_5$ when capacitance C_3 is fully discharged and when current i_1 starts flowing through antiparallel diode D_3 of switch S_3, as shown in Fig. 3(f). Because after $t=T_5$ negative voltage $V_{IN}/2$ is applied across magnetizing inductance L_{MC}, magnetizing current i_{MC} starts linearly decreasing toward zero with constant slope $-V_{IN}/(2L_{MC})$, as shown in Fig. 4. After current i_{MC} reaches zero at $t=T_6$, it continues to flow in the negative direction as indicated in Fig. 3(g). This topological stage in Fig. 3(g) ends at $t=T_7$ when switch S_4 is turned off and the converter enters the second half of the switching cycle. The operation during the second half of the switching cycle, i.e., the operation during time interval $T_7 - T_{13}$, is identical to the operation during the described interval $T_1 - T_7$ with the roles of switches S_1 and S_2 and switches S_3 and S_4 exchanged.

As can be seen from current waveforms i_1 and i_2 in Fig. 4, for all four primary switches S_1 through S_4 the magnitude of the current flowing through the switch at the moment of turn-off is the same, i.e.,

$$i_2(t=T_1) = i_1(t=T_4) = i_2(t=T_7) = i_1(t=T_{10}) = \left|\frac{i_P}{2}\right| + \left|I_{MC}\right| = \left|\frac{I_O}{2n_{TR}}\right| + \left|I_{MC}\right|, \quad (11)$$

where, I_O is the load current, n_{TR} is the turns ratio of the transformer, and I_{MC} is the amplitude of magnetizing current i_{MC}.

According to Eq. (11), the commutation of the switches, during which the capacitance of the turned-off switch is charging (voltage across the switch is increasing) and the capacitance of the switch that is about to be turned on is discharging (voltage across the switch is decreasing), is done by the energy stored by both primary current i_P and magnetizing current i_{MC}. While the commutation energy contributed by magnetizing current i_{MC} is always stored in magnetizing inductance L_{MC} of coupled inductor L_C, the commutation energy contributed by current i_P is stored either in the filter inductance of the secondary-side output circuit, or the leakage inductances (not shown in Fig. 1) of transformer TR and coupled inductor L_C. Specifically, for inner switches S_2 and S_3, the commutation energy contributed by i_P is stored in output-filter inductor L_F, whereas for outer switches S_1 and S_4, it is stored in the leakage inductance of the transformer. Since it is desirable to minimize the leakage inductance of transformer TR to minimize the secondary-side parasitic ringing, the energy stored in its leakage inductances is relatively small, i.e., much smaller than the energy stored in output-filter inductance. As a result, in the circuit in Fig. 1, it is easy to achieve ZVS of inner switches S_2 and S_3 in the entire load range, whereas ZVS of the outer switches S_1 and S_4 requires a proper sizing of the magnetizing inductance L_{MC} since at light loads almost the entire energy required to create ZVS condition of outer switches S_1 and S_4 is stored in the magnetizing inductance.

III. DESIGN GUIDELINES

As previously explained, in the proposed three-level ZVS circuit with a coupled inductor, it is more difficult to achieve ZVS of the outer pair of switches than the inner pair of switches because the available energies for creating the ZVS conditions in the two pairs of switches are different. Generally, to achieve ZVS this energy must be at least equal to the energy required to discharge the capacitance of the switch which is about to be turned on and at the same time charge the capacitance of the switch that just has been turned off. At heavier load currents, ZVS is primarily achieved by the energy stored in the leakage inductances of transformer TR. As the load current decreases, the energy stored in the leakage inductances also decreases, whereas the energy stored in inductance L_C increases so that at light loads inductance L_C provides an increasing share of the energy required for ZVS. In fact, at no load, this inductance L_C provides the entire energy required to create the ZVS condition. Therefore, if the value of inductance L_C is selected so that ZVS is achieved at no load and maximum input voltage $V_{IN(max)}$, ZVS is achieved in the entire load and input-voltage range.

Neglecting the capacitances of the transformer's windings, magnetizing inductance L_{MC} necessary to achieve ZVS of the outer switches in the implementations in Fig. 1 is

$$L_{MC} \le \frac{1}{32Cf_S^2}, \qquad (12)$$

where C is the total capacitance across the primary switches (parasitic and external capacitance, if any) in the corresponding switch pairs.

IV. Experimental Results

The performance of the proposed three-level ZVS converter was verified on a 1-kW (48 V/21 A) prototype circuit operating at 100 kHz from a 750 V dc input. As shown in Fig. 5, the experimental circuit that employs a current doubler rectifier was implemented with the following components: switches Q_1-Q_4 = IRFP460LC (500 V, 20 A); primary diodes D_{C1} - D_{C2} = RHRP3060 (600 V, 30 A); output diodes D_{R1} - D_{R2} = BYV74W (400 V, 40 A); primary capacitors C_{S1}, C_{S2}, and C_B = 2.2 μF polypropylene capacitor. The core of transformer TR is a pair of ER42-3C90. The primary and secondary winding of transformer TR consist of eighteen turns and twelve turns of Litz wire (170 strands, AWG #40), respectively. The core of coupled inductor L_C is

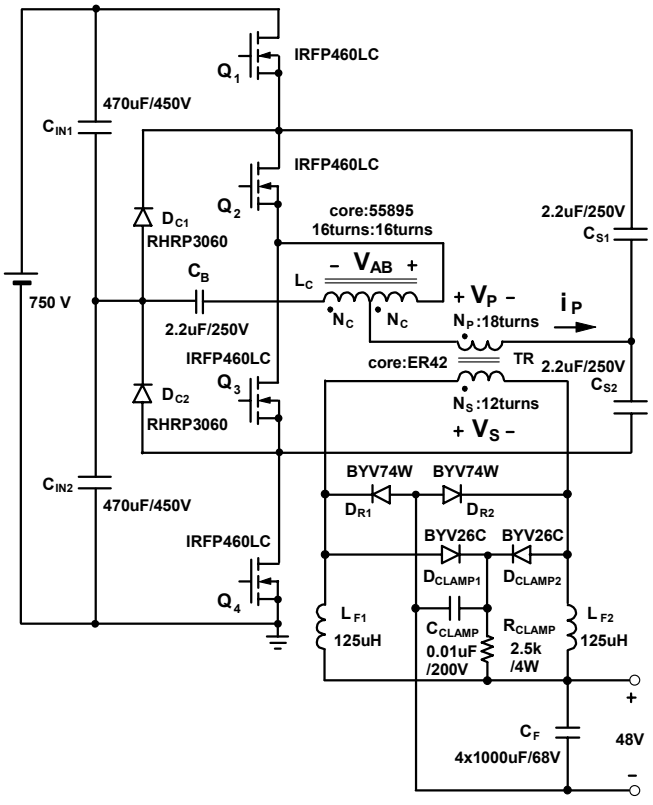
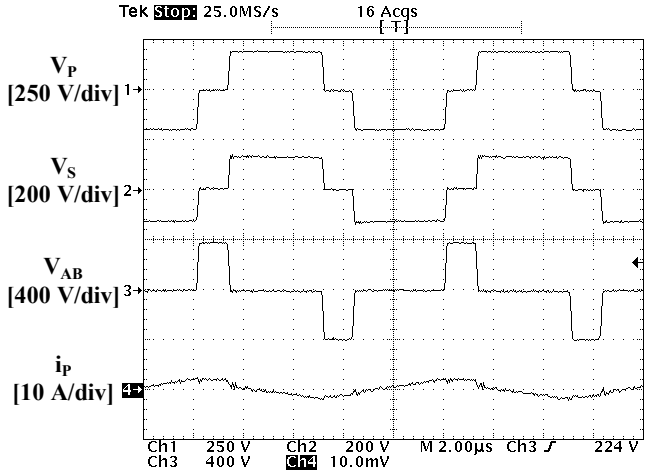
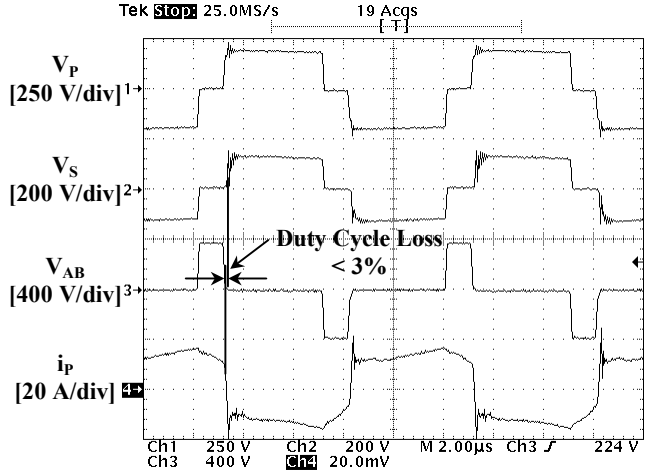


Fig. 5. Circuit diagram of 1-kW experimental prototype built to evaluate performance of proposed three-level ZVS converter.



(a)



(b)

Fig. 6. Measured key waveforms of proposed three-level ZVS converter: (a) at P_O = 50 W; (b) at P_O = 1 kW. From top to bottom: primary voltage V_P [250V/div]; secondary voltage V_S [200V/div]; coupled inductor voltage V_{AB} [400V/div]; primary current i_P [20 A/div]. Time base: 2 μs/div.

MPP 55894. The windings of coupled inductor L_C consist of sixteen turns of Litz wire (170 strands, AWG #40) each. Measured magnetizing inductance L_{MC} of coupled inductor L_C is approximately 76 μH. To control the parasitic ringing on the secondary side caused by the resonance between leakage inductance of the transformer and junction capacitance of the rectifier, the experimental circuit employs a R-C-D clamp circuit that consists of D_{CLAMP1}, D_{CLAMP2}, C_{CLAMP}, and R_{CLAMP}. The loss of the clamp circuit is less than 3 W, which is much lower than the loss of the conventional three-level converter that generally requires a large leakage inductance or even an external inductance to extend the ZVS range. The control circuit was implemented with a UC3895 constant-frequency phase-shift controller.

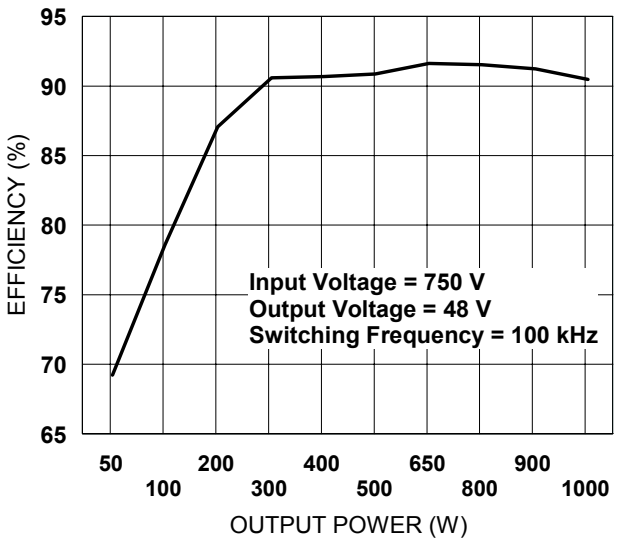


Fig. 7. Measured efficiency of the proposed three-level ZVS converter as function of output power

Figure 6 shows the measured waveforms of the proposed converter at full load and 5% load. The proposed converter has a very small duty cycle loss (< 3 %) even at full load, as well as a small parasitic ringing because of the minimized leakage inductance of the transformer that is less than 2 μH measured on the primary side of the transformer. The efficiency measurements for the proposed topology is summarized in Fig. 7.

V. Conclusion

A new isolated, constant-frequency, three-level ZVS converter which employs a coupled inductor on the primary side to achieve ZVS in a wide range of load current and input voltage with reduced circulating energy and conduction losses has been described. Since this coupled inductor does not appear as a series inductance in the load current path, it does not cause a loss of duty cycle or severe voltage ringing across the output rectifiers. The operation and performance of the proposed circuit was verified on a 1-kW (48-V/21-A) prototype.

References

[1] J.S. Lai and F.Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Trans. Industry Applications*, vol. 32, no. 3, pp. 509 – 517, 1996.

[2] J.R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," *IEEE Trans. Power Electronics*, vol. 8, no. 4, pp. 486 – 492, 1993.

[3] I. Barbi, R. Gules, R. Redl, and N.O. Sokal, "DC/DC converter for high input voltage: Four switches with peak voltage of $V_{in}/2$, capacitive turn-off snubbing, and zero-voltage turn-on," *IEEE Power Electronics Specialists Conf. (PESC) Proc.,* pp. 1 - 7, 1998.

[4] F. Canales, P.M. Barbosa, J.M. Burdio, and F.C. Lee, "A zero-voltage switching three-level DC/DC converter," *IEEE International Telecommunications Energy Conf. (INTELEC) Proc.,* pp. 512 - 517, 2000.

[5] S.J. Jeon, F. Canales, P.M. Barbosa, and F.C. Lee, "A primary-side-assisted zero-voltage and zero-current switching three-level DC-DC converter with phase-shift control," *IEEE Applied Power Electronics Conf. (APEC) Proc.,* pp. 641 - 647, 2002.

[6] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Trans. Power Electronics*, vol. 16, no. 5, pp. 612 – 622, 2001.