The Single-Stage TAIPEI Rectifier

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***Abstract*—A new three-phase, single-stage, isolated zero-voltage-switching (ZVS) rectifier that achieves less than 5% input-current total harmonic distortion (THD) and provides tightly regulated output voltage is introduced. The proposed circuit is obtained by integrating the three-phase, two-switch, ZVS, discontinuous-current-mode (DCM), boost power-factor-correction (PFC) rectifier with the ZVS full-bridge (FB) phase-shift dc/dc converter. The performance evaluation of the circuit was performed on a three-phase 1.8-kW prototype designed for the line-to-line voltage range of 180-264 V_{RMS} and delivering a tightly regulated, selectable, dc output voltage from 220 V to 300 V.**

I. Introduction

Generally, modern off-line power supplies consist of a front-end power-factor-correction (PFC) rectifier followed by an isolated dc-dc converter. In single-phase implementations, the PFC front-end is typically implemented either as a conventional boost converter, an interleaved boost converter, or a "bridgeless" boost converter [1]. In three-phase applications, the six-switch boost converter and Vienna rectifier are the most commonly used front-end topologies [2]. In high-performance applications, the Vienna rectifier is the preferred topology because it offers the highest efficiency with today's commercially available Si semiconductor devices.

The choice of isolated dc/dc output-stage topology is primarily dependent on the power level. At lower power levels, flyback and forward topologies are usually employed, whereas the bridge-type topologies are typically used at power levels over 400–500 W. In today's ac/dc power supplies that need to meet extremely challenging efficiency requirements across the entire load range, the zero-voltage-switching (ZVS) full-bridge (FB) converter with phase-shift control, the two-switch interleaved forward converter, and LLC series-resonant converter are exclusively used as dc/dc output stage. In three-phase applications with nominal line-to-line voltage 380/480 V, where the output voltage of the front end is in the 750-850-V range, the dc/dc output stage is either implemented by connecting inputs of two converters in series and their outputs in parallel, or by employing a three-level dc/dc topology [3]-[5]. Both of these approaches make possible to use 600-V-rated Si MOSFET devices which are more efficient compared to 1200-V-rated IGBTs.

Although the two-stage off-line conversion has demonstrated excellent performance, power supply designers have always been tempted to combine the two stages into a single stage to reduce the cost and/or to increase the power density. For example, various three-phase, single-stage implementations have been introduced in [5]-[10]. Generally, they either integrate a three-phase boost rectifier with an isolated dc/dc stage [5]-[8], or combine three single-phase, single-stage isolated converters into a three-phase isolated converter [9] and [10]. A high PF and low input current THD in the implementations in [5]-[8] were obtained by operating the integrated boost stage in the discontinuous-conduction mode (DCM) where the phase currents naturally follow the respective phase voltages, i.e., without any active current control. Generally, these implementations can achieve current THD from approximately 5% to 15% in the load range from full load down to 50% load. While this is acceptable performance in many applications, it is not good enough for applications in today's computer/telecom power systems which in this load range require THD below 5%.

In this paper, a single-stage three-phase rectifier that maintains current THD below 5% from full load down to 20% load is proposed. The proposed rectifier is derived by integrating the recently proposed three-phase, two-switch, ZVS PFC DCM boost rectifier, shortened to the TAIPEI rectifier [11], with a conventional phase-shift, ZVS FB converter [12]. In addition to exhibiting an excellent THD and PF performance, the rectifier offers ZVS of all switches in a wide output-current range which reduces switching losses and improves efficiency. The performance of the proposed single-stage TAIPEI rectifier was evaluated on a three-phase 1.8-kW prototype designed to operate in the line-to-line voltage range from 180 V_{RMS} to 264 V_{RMS} and deliver a tightly regulated, selectable, output voltage from 220 V to 300 V.

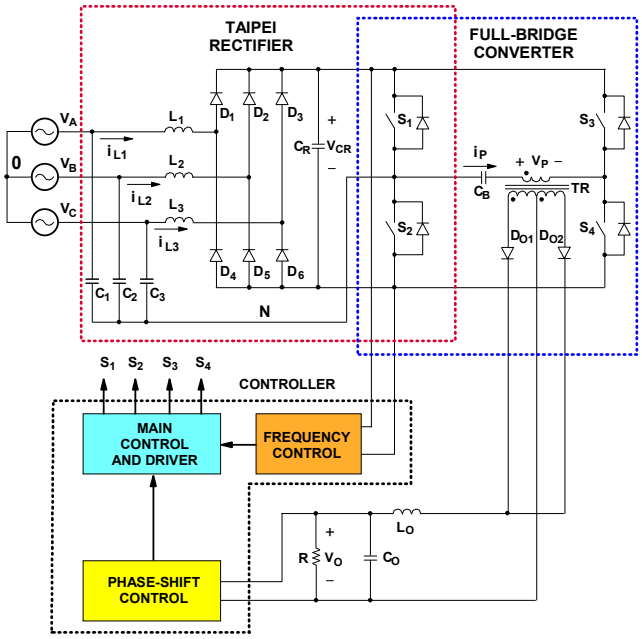

Fig. 1. Proposed single-stage TAIPEI rectifier.

II. THREE-PHASE SINGLE-STAGE TAIPEI RECTIFIER

The circuit diagram of the proposed three-phase, single-stage Taipei rectifier is shown in Fig. 1. In this circuit, switches S_1 and S_2 simultaneously serve as the switches of the boost front end and leading-leg switches of the ZVS FB. At the input side, three boost inductors L_1, L_2, and L_3 are connected to the three-phase power-source terminals along with three differential-mode filter capacitors C_1, C_2, and C_3 connected in Y ("star") configuration. Since for a balanced three-phase power source, the potential of the common node of the filter capacitors, labeled N in Fig. 1, has the same potential as power source neutral 0 that is not physically available or connected in three-wire power systems, node N represents a virtual neutral. Virtual neutral N is connected to the mid-point between two switches S_1 and S_2. As a result of connecting virtual neutral N directly to the mid-point between switches S_1 and S_2, decoupling of the three input currents is achieved. In such a decoupled circuit, the current in each of the three inductors is dependent only on the corresponding phase voltage, which reduces the THD and increases the PF [11]. In addition, the mid-point of the switches do not experience abrupt changes with high dV/dt, which makes it possible for the rectifier to operate with a relatively low common-mode EMI noise.

Switches S_3 and S_4 serve as the lagging-leg switches of the phase-shift FB converter whose primary also includes isolation transformer TR and blocking capacitor C_B. In Fig. 1, the secondary-side of the FB converter is implemented with the center-tapped secondary winding, output diodes D_{O1} and D_{O2}, and output filter L_O - C_O. However, in some applications it may be more appropriate to implement secondary side with a full-bridge rectifier or employ synchronous rectifiers (SRs) instead of the diode output rectifiers.

Since switches S_1 and S_2 operate as the PFC boost switches as well as the leading leg switches of the ZVS FB circuit, the energy required to achieve ZVS of switches S_1 and S_2 is stored both in boost inductors L_1-L_3 and the leakage inductance of transformer TR. Because the inductance of the boost inductors is relatively large, they store enough energy for complete ZVS of switches S_1 and S_2 even at very low power levels. As a result, in the proposed circuit in Fig. 1, the leakage inductance of the transformer can be minimized. This improves the performance of the ZVS FB converter because it minimizes the secondary-side duty-cycle loss and parasitic ringing between the junction capacitance of the secondary-side rectifier and the leakage inductance [12]. The energy required to achieve ZVS of lagging-leg switches S_3 and S_4 is stored in output inductor L_O. Since the inductance of the output-filter inductor is also large, all four switches in the proposed converter can achieve ZVS in a wide input-voltage and load range without an additional energy-storage inductor in series with the transformer primary, which is typically employed in conventional ZVS FB converters to extend the ZVS range.

As illustrated in Fig. 1, to simultaneously achieve low input-current harmonic distortions and tight output-voltage regulation, the proposed single-stage rectifier employs two feedback control loops. A low bandwidth (below several tens of Hz) frequency-controlled loop is used to regulate bus voltage V_{CR} and indirectly shape the discontinuous inductor currents to follow the respective phase voltage with low harmonic distortions. A high bandwidth (in the kHz range) phase-shift control loop is employed to tightly regulate output voltage V_O with negligible rectified-line- and switching-frequency ripple.

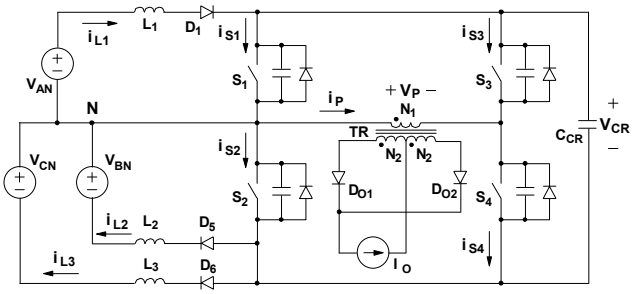

Fig. 2. Simplified circuit diagram of proposed single-stage Taipei rectifier.

It should be noted that the proposed single-stage TAIPEI rectifier is topologically identical to that described by Huang *et al.* in [8]. However, the input-current THD and efficiency performance of the two implementations are dramatically different because of different control approaches. The implementation in [8] regulates only the output voltage with a constant-frequency control that cannot achieve THD below 5% and does not provide ZVS of all four switches.

III. ANALYSIS OF OPERATION

The simplified circuit diagram of the proposed rectifier along with reference directions of currents and voltages is shown in Fig. 2. It should be noted that the model in Fig. 2 is only valid in the 60^0 segment of the line cycle where $V_{AN} > 0$, $V_{BN}<0$, and $V_{CN} <0$. However, the same model is applicable to any other 60^0 segment during which the phase voltages do not change polarity by properly selecting conducting rectifiers in the input six-diode rectifier [11]. The model in Fig 2 also assumes that the voltage across blocking capacitor C_B is much smaller than the voltage across the primary of transform TR, i.e., that the capacitance of the blocking capacitor is large enough so that the capacitor voltage drop caused by the primary current is small. In Fig. 2 the blocking capacitor C_B is represented by a short circuit.

To further facilitate the explanation of operation, Fig. 3 shows topological stages of the circuit in Fig. 2 during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms. As can be seen from the gate-drive timing diagrams for switches S_1 - S_4 in Fig. 4, the switches operate in a complementary fashion with approximately 50% duty cycle and with a short dead time between the turn-off of one switch and the turn-on of the other switch of each leg. Because of this gating strategy, all switches can achieve ZVS. In the proposed single-stage rectifier, the input power is controlled by S_1 and S_2 employing a variable switching

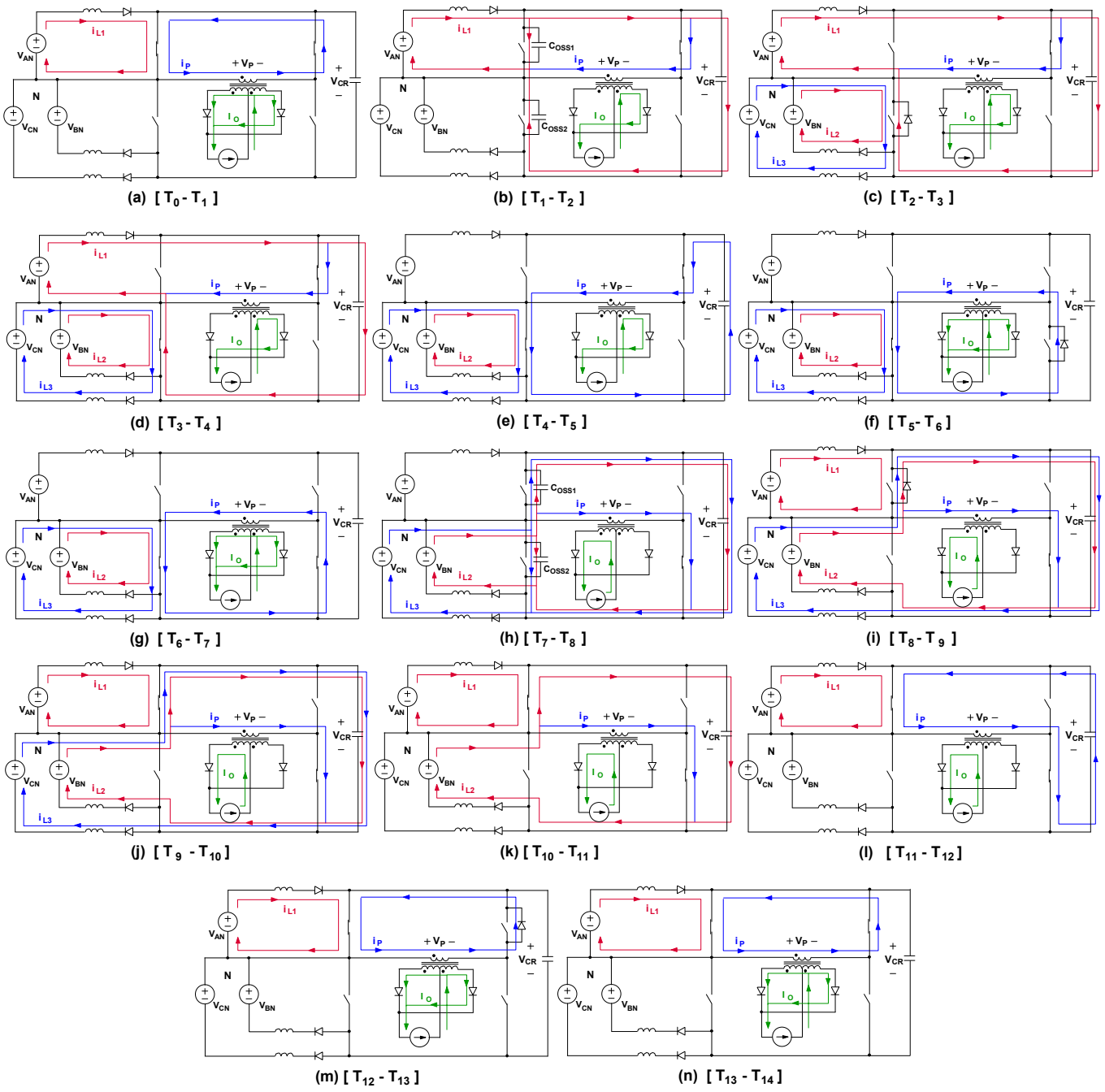

Fig. 3. Topological stages of proposed single-stage TAIPEI rectifier with condition when $V_{AN} > 0$, $V_{BN} < 0$, and $V_{CN} < 0$.

frequency control. The minimum frequency is set at full load and minimum input voltage, whereas the maximum frequency is set at light load and maximum input voltage. The output voltage is tightly regulated by phase-shift control between the S_1-S_2 leg and the S_3-S_4 leg. In this control, the switching transition of switches in the S_3-S_4 leg of the bridge is delayed, i.e., phase shifted, with respect to the switching transition of corresponding switches in the S_1-S_2 leg. By controlling the angle of the delay with a high bandwidth feedback loop, the output voltage is tightly regulated. The rectifier operates in controlled burst mode at light load or no load to avoid unnecessarily high switching frequency.

As shown in Figs. 3(a) and 4, before switch S_1 is turned off at $t=T_1$, inductor current i_{L1} flows through switch S_1. The slope of inductor current i_{L1} is equal to V_{AN}/L_1 and the peak of the inductor current at $t=T_1$ is approximately [11]

$$I_{L1(PK)} = \frac{V_{AN}}{L_1} \times \frac{T_S}{2}, \qquad (1)$$

where V_{AN} is line-to-neutral voltage and T_S the switching period.

During the period between T_0 and T_1, output diodes D_{O1} and D_{O2} conduct output current I_O and the secondary winding of transformer TR is shorted, as shown in Fig. 3(a). During this interval, primary current i_P decreases with the rate $2V_{S(ON)}/L_{LK}$ where L_{LK} is the leakage inductance of transformer TR (not shown in Fig. 3) and $V_{S(ON)}$ is the on-state voltage drop of the switch.

At $t=T_1$, when switch S_1 is turned off, inductor current i_{L1} starts charging the output capacitance of switch S_1, as shown in Fig. 3(b). Because the sum of the voltages across switch S_1 and switch S_2 is clamped to the flying capacitor voltage V_{CR}, the output capacitance of switch S_2 discharges at the same rate as the charging rate of the output capacitance of switch S_1. This period ends when the output capacitance of switch S_2 is fully discharged and the anti-parallel body diode of switch S_2 starts conducting at $t=T_2$, as shown in Fig. 3(c) and Fig. 4. Because the body diode of switch S_2 is forward biased, inductor currents i_{L2} and i_{L3} begin to increase linearly. When the body diode of switch S_2 starts conducting, primary voltage V_P of transformer TR reaches $-V_{CR}$ which makes output diode D_{O1} reverse biased, as shown in Fig. 3(c). During this period, primary current i_P is equal to $-nI_O$, where $n=N_2/N_1$ is the turns ratio of the transformer. At $t=T_3$, switch S_2 is turned on with ZVS and inductor currents i_{L1}, i_{L2}, and i_{L3} are commutated from the antiparallel diode of switch S_2 to the switch, as shown in Fig. 3(d). This period ends when inductor current i_{L1} decreases to zero at $t=T_4$. To maintain DCM operation, the time period between $t=T_3$ and $t=T_4$ must be less than one-half of switching period T_S which means that the rising slope of inductor current i_{L1} should be smaller than its falling slope. As illustrated in Fig. 4, the rising and falling slopes of i_{L1} are V_{AN}/L_1 and $(V_{AN}-V_{CR})/L_1$, respectively. As a result, minimum voltage $V_{CR\,(MIN)}$ across flying capacitor C_R to achieve DCM operation is

$$V_{CR(MIN)} = 2\times V_{AN(PK)} = \frac{2\sqrt{2}}{\sqrt{3}}\times V_{L-L(RMS)}\ , \qquad (2)$$

where $V_{AN\text{-}PK}$ is the peak line-to-neutral voltage.

It should also be noted that because during the T_2-T_4 interval inductor currents i_{L2} and i_{L3} and primary current i_P flow in the opposite direction from inductor current i_{L1}, the average current through switch S_2 is reduced so that the switch in the proposed rectifier exhibits reduced power losses. At time $t=T_5$, switch S_3 is turned off, primary current i_P, that is reflected output current nI_O, charges the output capacitance of switch S_3 to flying capacitor voltage V_{CR} which makes the anti-parallel body diode of switch S_4 to start conducting, as shown in Fig. 3(f). At $t=T_6$, switch S_4 is turned on with ZVS and primary current i_P is commutated from the antiparallel diode of switch S_4 to the switch as shown in Fig. 3(g). During the period between T_5 and T_7, output diodes D_{O1} and D_{O2} conduct output current I_O and the secondary winding of transformer TR is shorted so that primary current i_P increases with the rate $2V_{S(ON)}/L_{LK}$, as shown in Figs. 3(f) and 3(g).

During the period between $t=T_2$ and $t=T_7$, inductor currents i_{L2} and i_{L3} continue to flow through switch S_2 as shown in Fig. 4. The slopes of inductor currents i_{L2} and i_{L3} during this period are equal to V_{BN}/L_2 and V_{CN}/L_3, respectively, and their peaks at the moment when switch S_2 turns off are approximately

$$I_{L2(PK)} = \frac{V_{BN}}{L_2}\times\frac{T_S}{2} \quad \text{and} \qquad (3)$$

$$I_{L3(PK)} = \frac{V_{CN}}{L_3}\times\frac{T_S}{2}. \qquad (4)$$

As it can be seen in Eqs. (1), (3), and (4), the peak of each inductor current is proportional to its corresponding phase voltage, which results in a low THD of the phase currents [11].

After switch S_2 is turned off at $t=T_7$, inductor currents i_{L2} and i_{L3} start to simultaneously charge the output capacitance of switch S_2 and discharge the output capacitance of switch S_1, as shown in Fig. 3(h). This period ends at $t=T_8$ when the output capacitance of switch S_1 is fully discharged and its anti-parallel diode starts conducting, as shown in Fig. 3(i) and Fig. 4. After $t=T_8$, switch S_1 can be turned on with ZVS. In Fig. 4, switch S_1 is turned on at $t=T_9$. As shown in Fig.

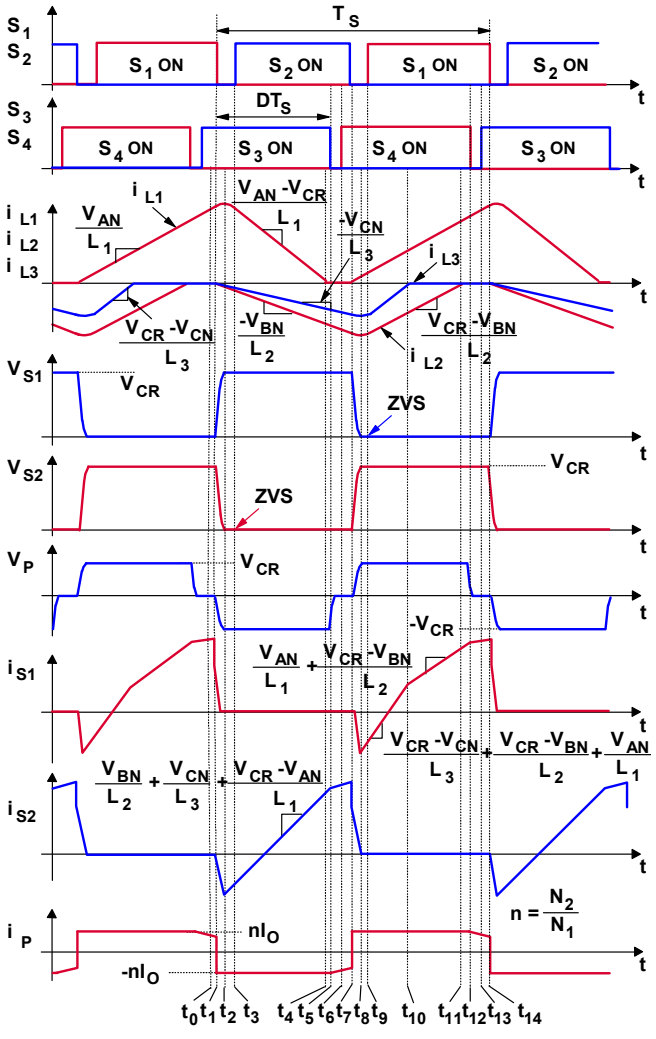

Fig. 4. Key waveforms of proposed single-stage TAIPEI rectifier when $V_{AN} > 0$, $V_{BN} < 0$, and $V_{CN} < 0$.

3(j), once switch S_1 is on, increasing inductor current i_{L1} and primary current i_P flow in the opposite direction from inductor currents i_{L2} and i_{L3} through switch S_1 so that switch S_1 carries only the difference of sum of current i_{L1} and primary current i_P and sum of currents i_{L2} and i_{L3}. This period ends when inductor current i_{L3} decreases to zero at $t=T_{10}$. During period T_{10}-T_{11}, decreasing inductor current i_{L2} continues to flow through switch S_1, as shown in Fig. 3(k). After inductor current i_{L2} reaches zero at $t=T_{11}$, switch S_4 is turned off at $t=T_{12}$ and primary current i_P charges the output capacitance of switch S_4 to V_{CR}. The anti-parallel body diode of switch S_3 starts conducting at $t=T_{12}$, as shown in Fig. 3(m). At $t=T_{13}$, switch S_3 is turned on with ZVS and primary current i_P is commutated from the antiparallel diode of switch S_3 to the switch, as shown in Fig. 3(n), and a new switching cycle begins.

In the proposed rectifier, output voltage V_O is related to the average voltage across flying capacitor $V_{CR(AVG)}$ as

$$V_O = 2 \times n \times D \times V_{CR(AVG)} \ , \qquad (5)$$

where duty cycle D is the phase shift shown in the gate-timing waveforms in Fig. 4. The value of voltage $V_{CR(AVG)}$ is determined by the regulation set point of the low-bandwidth variable-frequency control loop and its minimum value has to meet Eq. (2).

Finally, it should be noted that in the proposed rectifier the input current is not sensed. The input current shaping is obtained naturally by setting the rectifier's output-voltage-control bandwidth much lower than the line frequency, i.e., by maintaining switching period T_S virtually constant during a line cycle. With a constant switching period T_S and 50% duty cycle, the peaks of the inductor currents are proportional to the corresponding phase voltages. For such a triangular current waveform, the line-frequency average-current distortion is predominantly contained in the 3rd harmonic. Since the 3rd harmonic (triplen harmonic) currents cannot flow in a three-wire system, they circulate through capacitors C_1, C_2, and C_3, whereas the remaining harmonics contributes less than 1% of input-current THD, as described in [11].

IV. Experimental Results

The performance of the proposed rectifier was evaluated on a 1.8-kW prototype circuit that was designed to operate from a 180-264 $V_{L\text{-}L(RMS)}$ three-phase input and deliver a tightly regulated selectable output voltage from 220 V to 300 V. The application targeted by this input/output specification was the three-phase, isolated front end for high-voltage (HV) DC distribution power systems.

The prototype circuit was designed with the variable-frequency-control-loop bandwidth of 10 Hz and the phase-shift-control-loop bandwidth of 2 kHz. The low-bandwidth frequency-control loop was used to regulate the flying-capacitor voltage V_{CR} to 400 V. The switching frequency range of the variable-frequency control was between 50 kHz and 300 kHz.

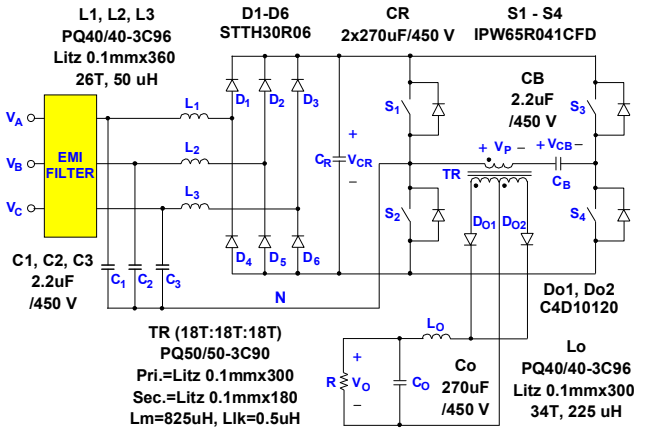

Fig. 5. Experimental prototype circuit of proposed rectifier.

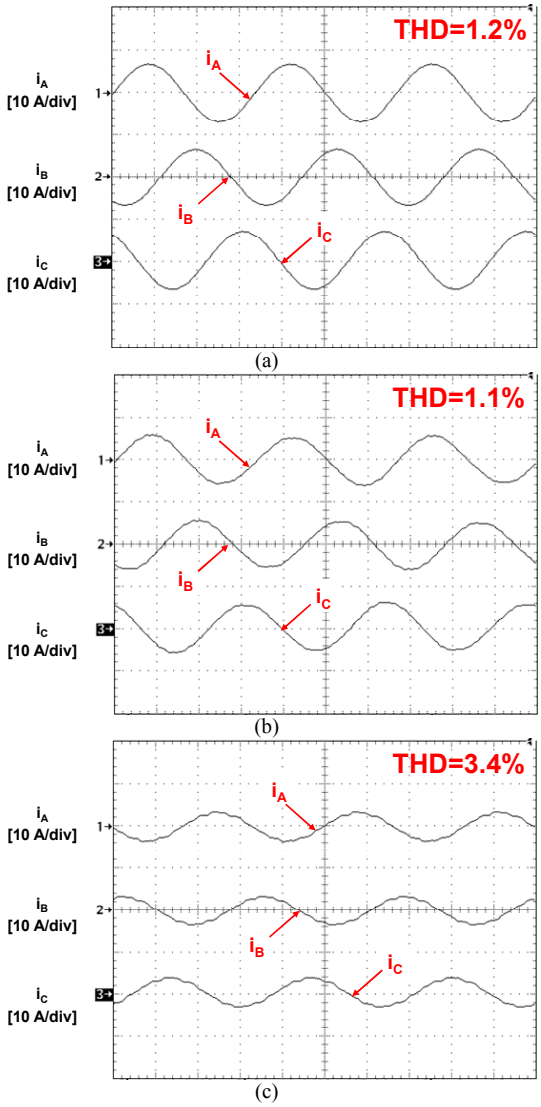

Fig. 6. Measured input current waveforms when rectifier operates from three-phase input voltage 230 $V_{L\text{-}L(RMS)}$ and delivers: (a) 1.8 kW; (b) 1.5 kW; (c) 900 W. Time scale is 5 mS/div.

Figure 5 shows the power-stage schematics along with component information of the experimental prototype circuit. Since the voltage stress of all primary switches S_1 - S_4 is approximately equal to flying capacitor voltage V_{CR} of 400 V, switches that are rated at least 500 V must be used to maintain the desirable design margin of 20%. In the prototype circuit, an IPW65R041CFD MOSFET (V_{DS} = 650 V, R_{DS} = 0.041 Ω, C_{OSS}=400 pF, Q_{rr}=1.9 µC) from Infineon was used for each switch. Since input diodes D_1 - D_6 block the same peak voltage stress and conduct the same peak current (approximately 20 A) as the switches, an STTH30R06 diode (V_{RRM} = 600 V, I_{FAVM} = 30 A) from ST was used for each diode. A C4D10120 SiC diode (V_{RRM} = 1200 V, I_{FAVM} = 10 A) from Cree was used for each output diode because their voltage stress is twice the peak voltage across the primary winding of transformer TR since the turns ratio of transformer TR is n=1.

To obtain the desired inductance of boost inductors L_1, L_2, and L_3 of approximately 50 µH and also to achieve high efficiency at light-load, each inductor was built using a pair of ferrite cores (PQ-40/40, 3C96) with 26 turns of Litz wire (Φ 0.1mm, 360 strands) and approximately 8 mm gap. Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor core. Transformer TR was built using a pair of ferrite cores (PQ-50/50, 3C96) with 18 turns of Litz wire (Φ 0.1mm, 300 strands) for the primary winding and 18 turns of Litz wire (Φ 0.1mm, 180 strands) for the two secondary windings that form the center-tap secondary structure. The measured magnetizing and leakage inductances are 825 µH and 0.5 µH, respectively. Output inductor L_O was built using a pair of ferrite cores (PQ-40/40, 3C96) with 34 turns of Litz wire (Φ 0.1mm, 300 strands) with approximately 1 mm gap. Its measured inductance is 225 µH.

Two parallel connected aluminum capacitors (270 µF, 450 VDC) were used for flying capacitor C_R and a film capacitor (2.2 µF, 450 VDC) was used for each input filter capacitor C_1, C_2, and C_3 as well as for blocking capacitor C_B. An aluminum capacitor (270 µF, 450 VDC) was used for output capacitor C_O.

Figures 6(a)-(c) show the measured input current waveforms of the experimental circuit at the input voltage of 230 $V_{L\text{-}L(RMS)}$ and three different power levels. The measured input-current THDs are approximately 1.2%, 1.1%, and 3.4% at 1.8 kW, 1.5 kW, and 900 W, respectively.

To illustrate the ZVS of the primary switches, Fig. 7 shows drain-to-source voltages V_{S2} and V_{S4} of switches S_2 and S_4 (the ground referenced switches) together with their gate driving voltages $V_{S2\text{-}GATE}$ and $V_{S4\text{-}GATE}$ at full power and for the input voltage of 230 $V_{L\text{-}L(RMS)}$. As it can be seen in Fig. 7, the drain-to-source voltages of the switches become zero before the switches are turned on. Complementary switches S_1 and S_3 (not shown) operate in the same manner.

Figure 8 shows the measured current waveforms of boost inductors L_1, L_2, and L_3 of the experimental circuit at full power, 1.5 kW, and 900 W when it operates from three-phase input voltage 230 $V_{L\text{-}L(RMS)}$. The experimental

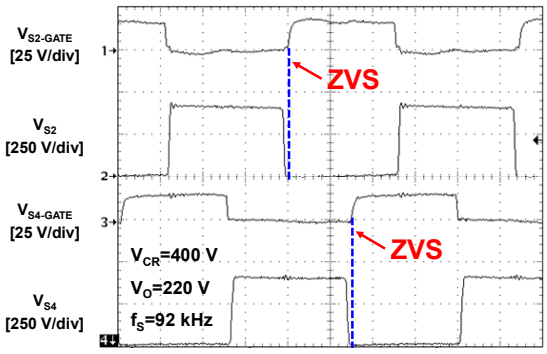

Fig. 7. Measured waveforms of switch voltages V_{S2} and V_{S4} together with their gate driving voltages $V_{S2\text{-}GATE}$ and $V_{S4\text{-}GATE}$ when rectifier delivers full power from three-phase input voltage 230 $V_{L\text{-}L(RMS)}$. Time scale is 2 µS/div.

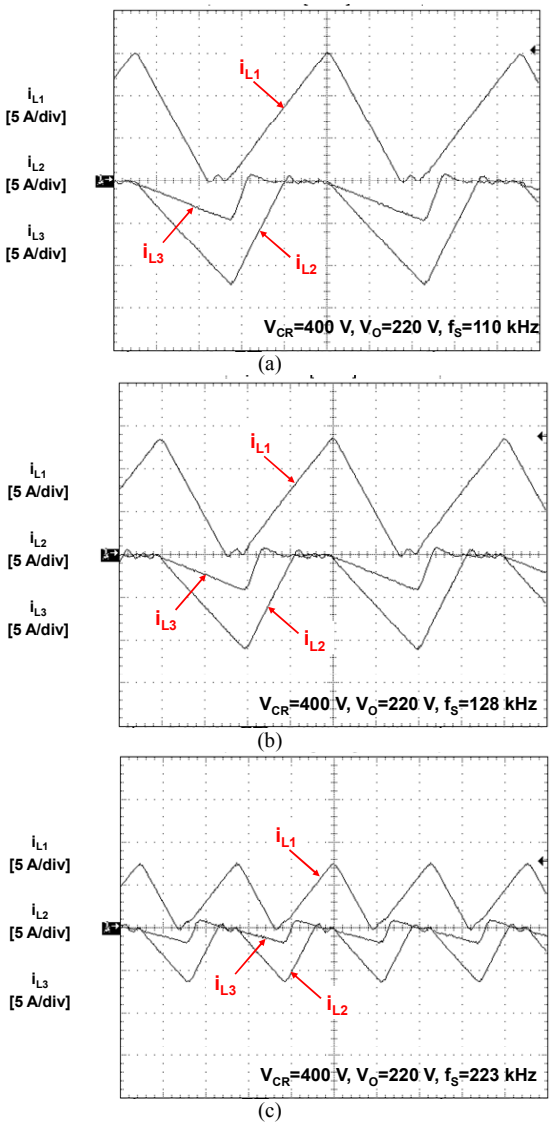

Fig. 8. Measured waveforms of inductor currents i_{L1}, i_{L2}, and i_{L3} when rectifier operates from three-phase input voltage 230 $V_{L\text{-}L(RMS)}$ and delivers: (a) 1.8 kW; (b) 1.5 kW; (c) 900 W. Time scale is 2 µS/div.

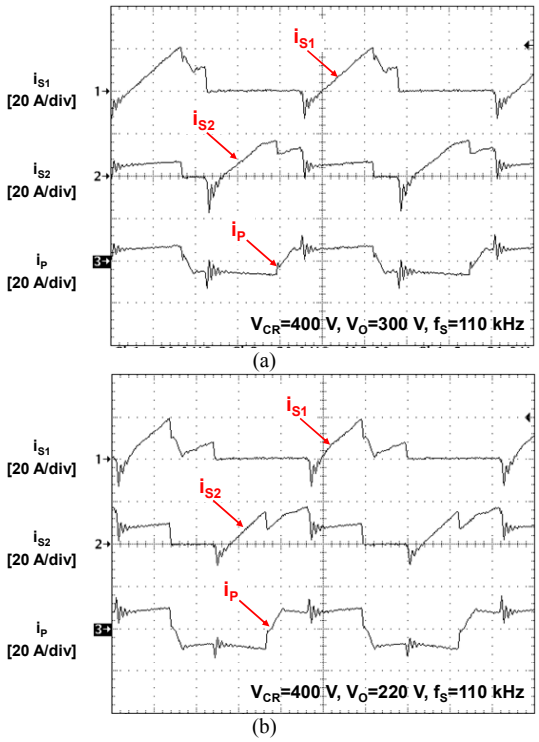

Fig. 9. Measured waveforms of drain currents i_{S1} of switch S_1 and i_{S2} of switch S_2 together with primary current I_P of transformer TR when rectifier delivers full power from three-phase input voltage 230 $V_{L\text{-}L(RMS)}$ and regulates output voltage: (a) 300 V and (b) 220 V. Time scale is 2 μS/div.

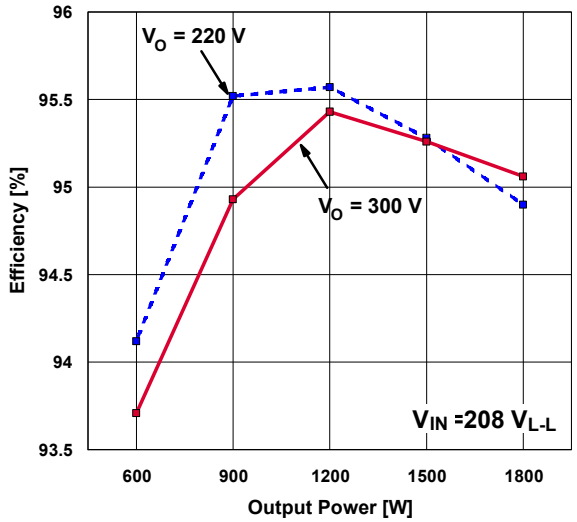

Fig. 10. Measured efficiencies of experimental PFC rectifier prototype as functions of output power.

waveforms are in very good agreement with corresponding ideal waveforms shown in Fig. 4. Figure 9 shows the waveforms of the drain currents of switches S_1 and S_2 along with the waveform of primary current i_P of transformer TR at full power and 230 $V_{L\text{-}L(RMS)}$ for the output voltage regulated at 300 V and 220V. The reason for a noticeable discrepancy between the measured current waveforms of switches S_1 and

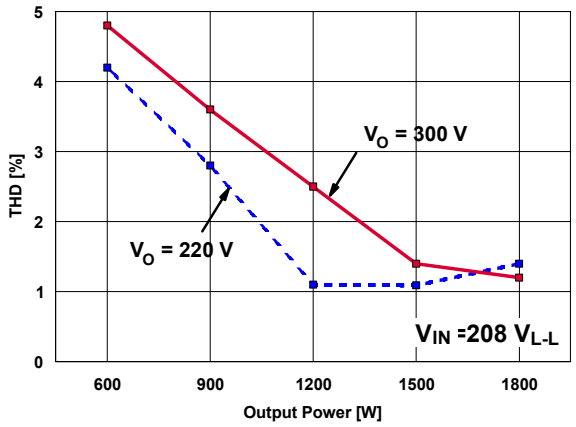

Fig. 11. Measured THDs of experimental PFC rectifier prototype as functions of output power.

S_2 and corresponding ideal waveforms in Fig. 4 is the assumption that the voltage of the blocking capacitor is zero, i.e., modeling the blocking capacitor with a short circuit in Fig. 2. In the prototype circuit, the peak ac voltage across blocking capacitor C_B caused by the primary current flowing through it is around 30 V and its effect cannot be neglected. In fact, this voltage causes a relatively large decrease of the switch currents during the time intervals the secondary winding of the transformer is shorted, i.e., during intervals T_5-T_7 and T_{12}-T_{14} in Fig. 3, because the blocking capacitor voltage resets (decreases) the transformer primary current with a relatively high rate V_{CB}/L_{LK}.

Finally, the measured efficiency and THD of the proposed rectifier as functions of output power at the line-voltage of 230 $V_{L\text{-}L(RMS)}$ are shown in Fig. 10 and Fig. 11, respectively. The measured efficiency is between 94% and 95.5% from full load down to 40% of the full load while the measured THD is below 5% in the entire measured range of power.

V. Summary

In this paper, the three-phase single-stage rectifier that is derived by combining the recently introduced Taipei rectifier and a conventional phase-shift full-bridge converter has been described. The proposed rectifier offers low input-current THD (< 5%) and a tightly regulated, isolated, output voltage and features ZVS of all the switches over the entire input and load range. The evaluation of the proposed converter was performed on a three-phase 1.8-kW prototype operating from the line-to-line voltage range of 180-264-V_{RMS} and delivering a tightly regulated selectable output voltage from 220 V to 300 V. The measured efficiency of the proposed rectifier is between 94% and 95.5% from full load down to 40% load.

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