Universal-Input Single-Stage PFC Flyback with Variable Boost Inductance for High-Brightness LED Applications

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Abstract — **This paper presents a single-stage flyback power-factor-correction circuit with a variable boost inductance for high-brightness light-emitting-diode applications for the universal input voltage (90-270 Vrms). The proposed circuit overcomes the limitations of the conventional single-stage PFC flyback with a constant boost inductance, which cannot be designed to achieve a practical bulk-capacitor voltage level (i.e., less than 450 V) at high line while meeting the IEC 61000-3-2 Class C line current harmonic limits at low line. According to the proposed variable boost inductance method, the boost inductance is constant in the high-voltage range and it is reduced in the low-voltage range, resulting in discontinuous-conduction-mode operation and a low total harmonic distortion (THD) in both the high-voltage and low-voltage ranges. Measurements obtained on a 24-V/91-W experimental prototype are as follows: PF = 0.9873, THD = 12%, and efficiency = 88% at nominal low line (120 V_{rms}); and PF = 0.9474, THD = 10.39%, and efficiency = 91% at nominal high line (230 V_{rms}). The line current harmonics satisfy the IEC 61000-3-2 Class C limits with enough margin.**

I. INTRODUCTION

The technology and performance of high-brightness light-emitting diodes (HB LEDs) has undergone significant improvements driven by new applications in liquid-crystal-display (LCD) backlighting, automobiles, traffic lights, and general-purpose lighting [1]-[3]. As a solid state light source which does not contain mercury, HB LEDs have been widely accepted because of their superior longevity, low-maintenance requirements, and continuously-improving luminance with a great potential to replace existing lighting sources such as incandescent and fluorescent lamps in the future.

For LED drivers with an output power over 25 W in general lighting applications, the line current harmonics have to satisfy the limits set by IEC 61000-3-2 Class C regulations [4]. With passive power-factor-correction (PFC), which uses only inductors and capacitors, it is difficult to meet such requirements, and the size of the components is large.

An LED driver with active PFC, which is implemented with two stages, is shown in Fig. 1. The first stage can achieve a near unity power factor and a low THD at the universal input voltage, while the second stage is used for the dc/dc conversion. However, the circuit in Fig. 1 requires two independently controlled power switches and two control circuits, leading to a high component count, increased cost, and larger size. In low-power lighting applications, where cost is the dominant issue, such an approach loses appeal.

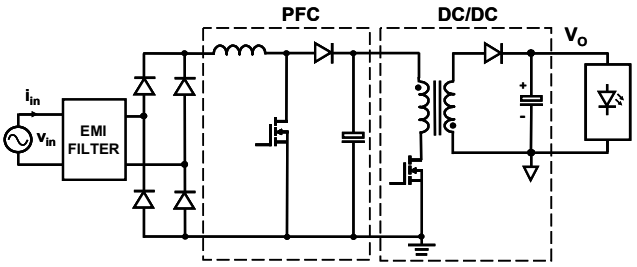


Fig. 1. Conventional two-stage LED driver.

Another active PFC implementation employs a single-stage ac/dc converter [5]-[13], where the PFC stage is integrated with the dc/dc stage, resulting in a reduced complexity and cost. The single-stage PFC ac/dc converter can be implemented without and with a bulk capacitor at the primary side, as illustrated in Figs. 2 and 3, respectively. Although the single-stage PFC circuit in Fig. 2 [5] has the advantage of a low component count, its output voltage has a high ripple at twice the line frequency unless very large output capacitors are used. For an LED load, a small variation in the driving voltage can lead to a large variation in the LED current. A large ripple of the LED current would seriously affect the longevity of the LEDs [12]. Therefore, the approach in Fig. 2 often requires a post-regulator, which adds cost and lowers the efficiency.

The single-stage PFC flyback topology shown in Fig. 3 [11] presents one of the most cost-effective single-stage solutions. In this converter, the PFC stage operates in discontinuous conduction mode (DCM), while the dc/dc stage operates at the DCM/CCM (continuous-conduction-mode) boundary. A low input-current harmonic distortion

can be achieved due to the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle is held relatively constant during a half line cycle. However, voltage V_B across bulk capacitor C_B is not regulated and at high line it can increase to impractical levels. To reduce the bulk capacitor voltage, one terminal of the boost inductor winding is connected to a tapping point of the primary winding of the flyback transformer, which provides a negative magnetic feedback [7]. However, the tapping of the flyback primary winding also results in a zero-crossing distortion of the line current. In fact, as long as the instantaneous line voltage is lower than the voltage at the tapping point, no current is drawn from the input, which reduces the power factor and increases the line-current harmonics.

The single-stage PFC flyback topology shown in Fig. 3 has been successfully applied in adapter/charger applications for the universal line voltage, where the line current harmonics need to meet the IEC 61000-3-2 Class D limits, which are less stringent than the IEC 61000-3-2 Class C limits.

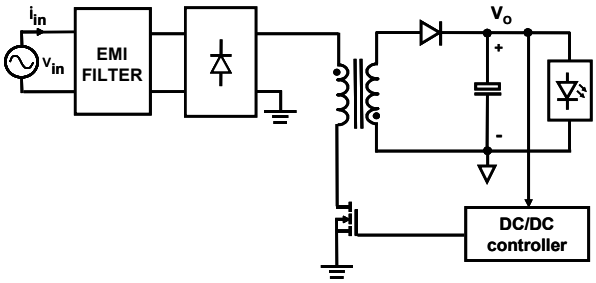


Fig. 2. Single-stage flyback LED driver without energy-storage capacitor at primary side.

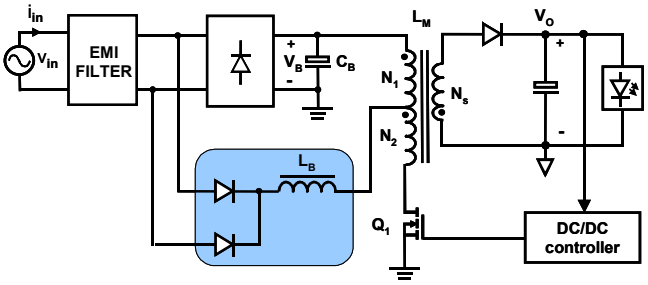


Fig. 3. Single-stage flyback LED driver with energy-storage capacitor at primary side.

It was shown in [14] that the single-stage PFC flyback in Fig. 3 with a constant boost inductance cannot be designed to achieve a practical bulk-capacitor voltage level (i.e., less than 450 V) at high line while meeting the IEC 61000-3-2 Class C line-current harmonic limits at low line. To overcome these limitations, a variable boost inductance is required, i.e., a high boost inductance at high line to limit the bulk-capacitor voltage and a lower boost inductance at low line to ensure DCM operation and a low THD. In fact, at low line, when a constant boost inductance is used, the inductor will enter CCM operation around the peak of the line voltage, and the line current waveform will have a bulge around its peak value [14], resulting in an increased THD. Furthermore, if the bulk-capacitor voltage is slightly lower than the peak of the rectified line voltage, the peak charging of the bulk capacitor through the bridge rectifier will also result in a bulge in the line current waveform [7] with an increased THD.

In this paper, it is shown that by optimizing the tapping point of the primary-winding of the flyback transformer in Fig. 3 and by employing a novel technique to reduce the boost inductance at low line, a high power factor and a low THD with relatively high efficiency can be achieved such that the line current harmonics satisfy the IEC 61000-3-2 Class C limits.

II. Variable Boost Inductance

A. Concept

As voltage V_B across bulk-capacitor C_B in Fig. 3 is not regulated and varies with both the input voltage and output power, the design of the magnetic components significantly affects the bulk-capacitor voltage level. Generally, a higher boost inductance L_B leads to a lower voltage V_B. If the boost inductance increases during steady-state operation, the input power initially decreases because of a lower input current. The difference between the output power and input power has to be supplied from the bulk capacitor, causing a drop of the bulk-capacitor voltage. Meanwhile, as the bulk-capacitor voltage decreases, the duty cycle of main switch Q_1 increases to keep the output voltage regulated, resulting in an increase of the input power until a new balance between the input and output power is reached. A higher boost inductance can limit voltage V_B to an acceptable level and ensure DCM operation at high line. However, at low line, if the boost inductance is larger than the maximum value for DCM operation, the boost inductor will operate in CCM around the peak of the rectified line voltage, resulting in a severe distortion of the line current [14]. Therefore, a variable boost inductance is required, i.e., a high boost inductance at high line and a lower boost inductance at low line.

Various methods for achieving a variable inductance were reported in [15]-[23], but their applications are limited either because of a high power loss [15]-[20], or complexity of the implementation [21]-[22], or because they can only meet IEC 61000-3-2 Class D current harmonic limits [23].

The concept of the variable boost inductance proposed in this paper is shown in Fig. 4. The basic PFC boost inductor is implemented with an EE core and winding N_{LB}. A half core (E) with winding N_{BIAS} is closely attached to the bottom part of the EE core. The boost inductance L_B is controlled by a bias current I_{BIAS}. The control circuit includes switch Q_{BIAS}, a dc bias control circuit, and an input voltage sensing circuit. At low line, switch Q_{BIAS} is open by sensing the input voltage, and the bias current flows through bias winding N_{BIAS}, inducing a magnetic flux Φ_{BIAS} that is added to the main magnetic flux Φ_{LB} at the bottom part of the boost-inductor EE core. As a result, at the bottom part of the EE core, the effective permeability is reduced, and consequently, the boost

inductance is decreased [17]. The reduction of the boost inductance is proportional to the applied bias current. At high line, switch Q_{BIAS} is closed, shorting bias winding N_{BIAS}. As a result, there is no bias current through winding N_{BIAS}, and the boost inductance does not change.

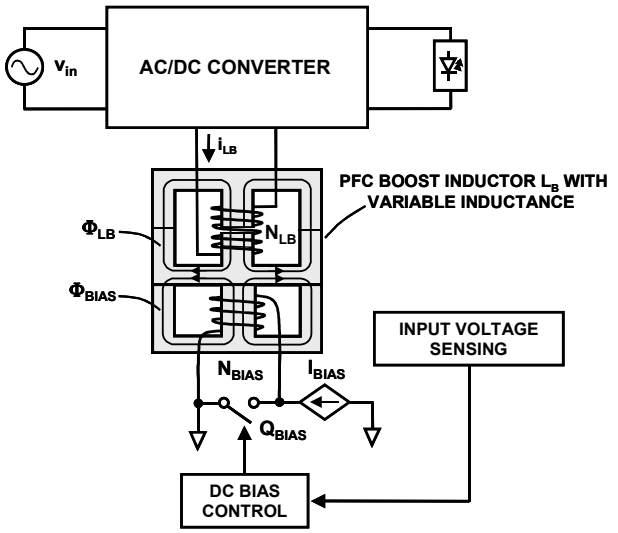


Fig. 4. Concept of proposed single-stage PFC with a variable boost inductance.

B. Control circuit

Figure 5 shows the detailed schematic of the proposed single-stage PFC flyback HB LED driver. The input voltage is sensed by a circuit comprising winding N_3 wound around the boost-inductor EE core, diode D_8, and capacitor C_1. The load current is used as the dc bias current to reduce complexity and loss of efficiency. Switch Q_2 connected in series with the LED load is the bias switch Q_{BIAS} in Fig. 4.

When main switch Q_1 is turned on, diode D_8 is forward biased, peak charging capacitor C_1 with a maximum voltage

$$V_{C1MAX} = (\sqrt{2}V_{IN} - \frac{N_1}{N_P} V_B)\frac{N_3}{N_{LB}}, \quad (1)$$

where N_1, N_P and N_{LB} are the number of turns of the feedback winding, primary winding of the flyback transformer, and the boost-inductor winding, respectively. A proper turns number N_3 is chosen so that the voltage across capacitor C_1 turns on Zener diode ZD_1 only at high line (180-270 Vrms). When ZD_1 is turned on, switch Q_4 is turned on and switch Q_3 is turned off. As a result, the gate-to-source voltage of MOSFET Q_2 is high and Q_2 is turned on. The load current flows through switch Q_2 and the bias current of bias winding N_{BIAS} is approximately zero. Therefore, the boost inductance remains unchanged. It should be noted that the turn-on resistance of switch Q_2 needs to be negligible compared to the resistance of bias winding N_{BIAS} to prevent a substantial current flowing through the bias winding at high line. Otherwise, the effective boost inductance would become lower and voltage V_B would increase to an undesirable level. At low line, the voltage across capacitor C_1 is lower than the turn-on voltage of ZD_1, Q_4 is turned off and Q_3 is turned on. As a result, the gate-to-source voltage of MOSFET Q_2 is low and Q_2 is turned off. The entire load current flows through the bias winding. Therefore, the boost inductance is reduced.

C. Design considerations

The design of the flyback circuit in Fig. 5 without the PFC part is the same as the design of the conventional flyback circuit. Key design parameters of the PFC part of the flyback circuit in Fig. 5 are number of turns N_1 and boost inductance L_B. The design goal is to achieve a proper PFC operation, i.e., the line current to meet the IEC 61000-3-2 Class C limits, and to limit bulk-capacitor voltage V_B below 400 V.

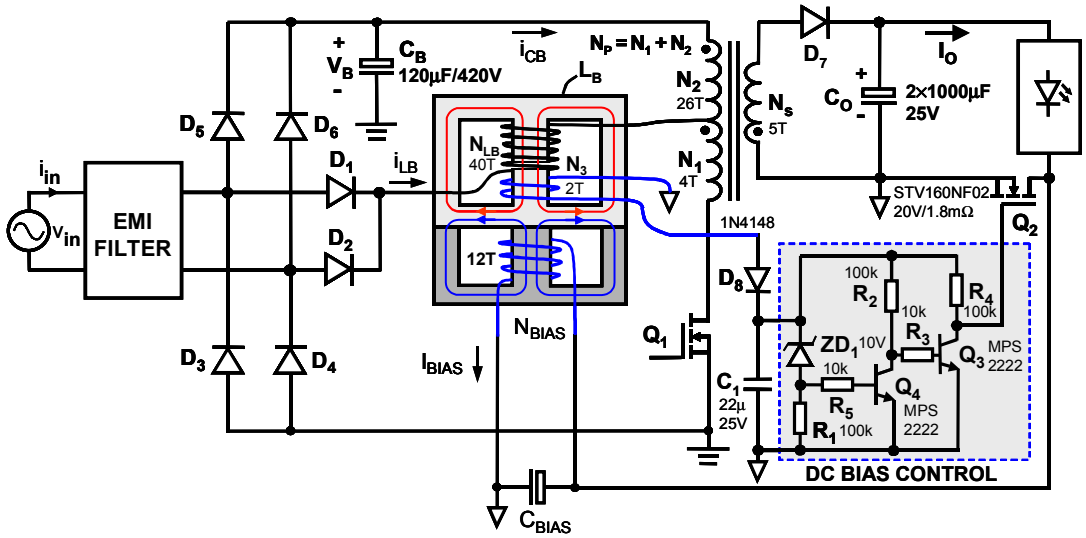


Fig. 5. Schematic of proposed single-stage PFC flyback with a variable boost inductance for HB LED applications.

It was shown in [14] that bulk-capacitor voltage V_B is a function of input voltage v_{IN}, ratio of inductances L_B/L_M, ratio of number of turns N_1/N_P, and output voltage V_o, i.e.,

$$V_B = f(v_{IN}, L_B/L_M, N_1/N_P, V_O). \quad (2)$$

The bulk-capacitor voltage increases with increasing rms value of the line voltage, and it decreases with increasing turns ratio N_1/N_P and increasing ratio of inductances L_B/L_M, as illustrated in Figs. 6 and 7, respectively.

For proper PFC operation, in order to meet the IEC 61000-3-2 Class C limits, the zero-crossing distortion of the line current due to the tapping of the primary winding should be optimized, and the boost inductor should be prevented from operating in CCM.

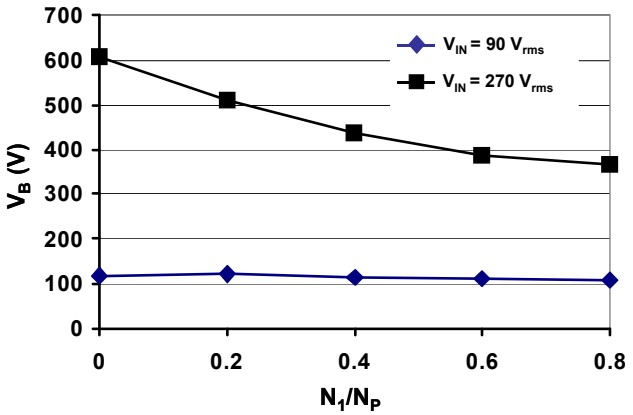


Fig. 6. Calculated voltage V_B vs. ratio N_1/N_P (L_B/L_M=0.25).

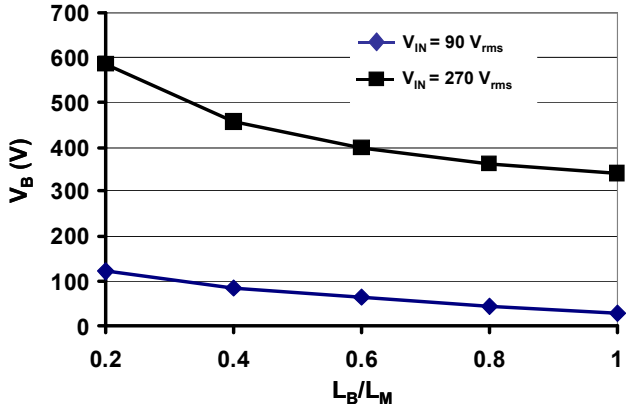


Fig. 7. Calculated voltage V_B vs. ratio L_B/L_M (N_1/N_P=0.133).

Following the same procedure for the analysis of the bulk-capacitor voltage as in [14] and assuming that the boost inductor operates in DCM, the line current waveform and the corresponding THD can be easily calculated. For example, calculated line current waveforms at three different turns ratios N_1/N_P, at nominal low line (V_{IN} = 120 Vrms), are shown in Fig. 8. It follows from Fig. 8 that with increasing turns ratio N_1/N_P the dead-angle of the line current around zero crossing increases, resulting in an increased THD. As another example, Fig. 9 shows calculated THD vs. N_1/N_P for three different values of L_B, at nominal high line (V_{IN} = 230 Vrms). It follows from Fig. 9 that THD significantly increases with increasing N_1/N_P, whereas the presented variation of L_B does not have significant effect on THD. It can be seen in Fig. 9 that for a THD lower than 20%, which is a typical requirement for lighting applications, turns ratio N_1/N_P should be smaller than 0.15.

In order to ensure DCM operation of boost inductor L_B, time T_{RES_LB}, i.e., the time to completely reset the boost-inductor core, should be shorter than the turn-off time, T_{OFF_Q1}, of switch Q_1 around the peak of the line voltage (worst case), i.e.,

$$T_{RES\_LB} \le T_{OFF\_Q1}. \quad (3)$$

In this way, the current flowing through the boost inductor decreases to zero before switch Q_1 is turned on, ensuring a high power factor and a low THD.

The turn-off time, T_{OFF_Q1}, of switch Q_1 operating at CCM/DCM boundary can be expressed as

$$T_{OFF\_Q1} = \left(1 - \frac{V_O N_P / N_S}{V_B + V_O N_P / N_S}\right) T_S, \quad (4)$$

where, T_S is the switching period of switch Q_1.

The time to completely reset the boost-inductor core can be expressed as

$$T_{RES\_LB} = \frac{(v_{IN}^{rec} - N_1 V_B / N_P) N_P V_O / N_S}{[V_B + (1 - N_1/N_P) N_P V_O / N_S - v_{IN}^{rec}](V_B + N_P V_O / N_S)} T_S, \quad (5)$$

where, v_{IN}^{rec} is the instantaneous rectified line voltage.

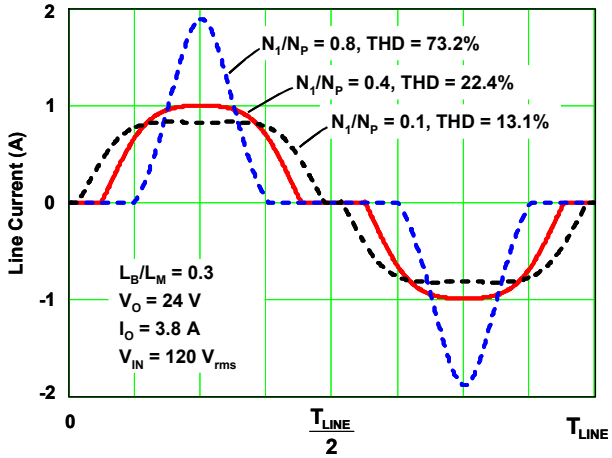


Fig. 8. Calculated line current waveforms for different ratios of N_1/N_P.

Using (2)-(5), the maximum ratio L_B/L_M vs. N_1/N_P that will ensure operation of L_B in DCM can be calculated. In Fig. 10, the calculated maximum ratio L_B/L_M vs. N_1/N_P that will ensure operation of L_B in DCM is presented at nominal low line (120 Vrms). Figure 10 also includes the calculated minimum L_B/L_M vs. N_1/N_P that will ensure limiting the bulk-capacitor voltage below 400 V at the upper end of the low line-voltage range (140 Vrms).

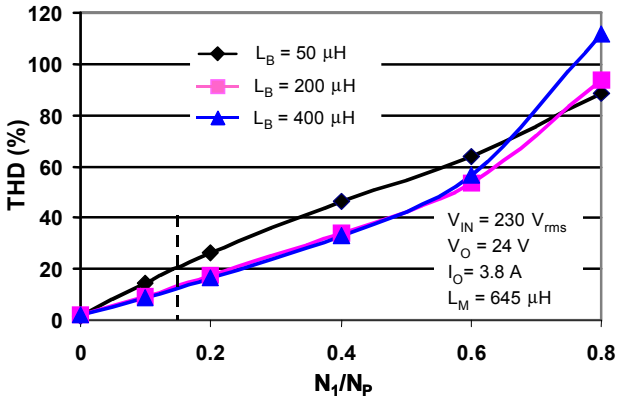


Fig. 9. Calculated THD vs. ratio N_1/N_P at V_{IN} = 230 Vrms.

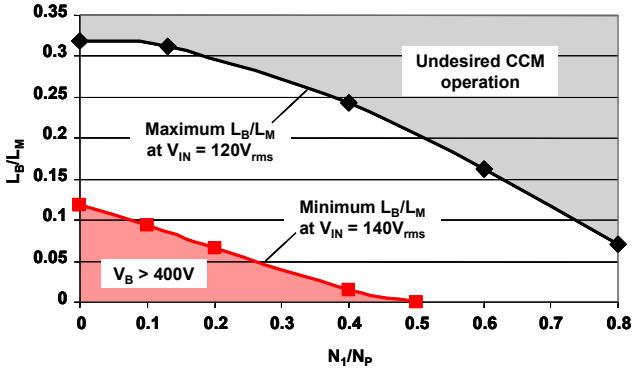


Fig. 10. Desired range for ratio L_B/L_M vs. ratio N_1/N_P in the low line-voltage range.

The calculated maximum and minimum ratios L_B/L_M vs. N_1/N_P in the high line-voltage range are presented in Fig. 11. As follows from Fig. 11, in the high line-voltage range, the possible range of ratio L_B/L_M is much narrower than at the low line-voltage range. It also follows from Fig. 11 that the minimum possible turns ratio N_1/N_P is 0.1.

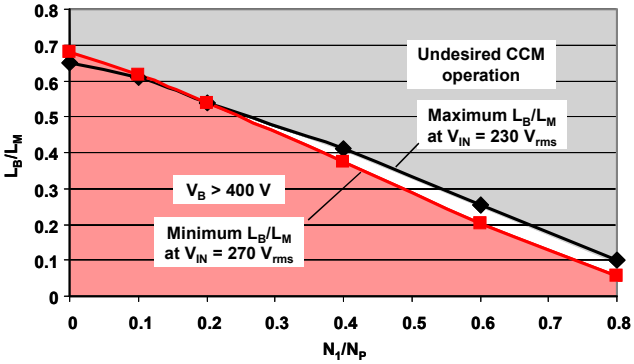


Fig. 11. Desired range for ratio L_B/L_M vs. ratio N_1/N_P in the high line-voltage range.

It can be clearly seen from Figs. 10 and 11 that different ratios of inductances L_B/L_M are required in the low line-voltage range and in the high line-voltage range, i.e., that a variable boost inductance is required in the universal line-voltage range.

Based on the calculated results presented in Figs. 6-9, turns ratio $N_1/N_P = 0.13$ ($N_1 = 4$, $N_P = 30$) is selected for the final design. It follows from Fig. 11 that for $N_1/N_P = 0.13$ in the high line-voltage range, ratio L_B/L_M should be around 0.6, i.e., the desired boost inductance is 390 uH for the selected L_M = 645 uH.

Finally, it follows from Fig. 10 that for $N_1/N_P = 0.13$ in the low line-voltage range, ratio L_B/L_M should be smaller than 0.32, i.e., the desired boost inductance should be smaller than 206 uH for the selected L_M = 645 uH.

III. Experimental Results

To verify the proposed variable boost-inductance technique, a 24-V/91-W single-stage PFC flyback prototype for HB LED applications was built. Figure 12 shows a photograph of the variable boost inductor with a dc bias winding, while Fig. 13 shows the measured boost inductance vs. dc bias current. As shown in Fig. 13, the effective boost inductance drops faster with increasing dc bias current when the turns number N_{BIAS} of the bias winding is higher, and therefore, it requires a lower dc bias current. However, a higher turns number N_{BIAS} leads to a higher resistance, hence, higher winding loss for the same load current. Moreover, a lower boost inductance generally results in a lower overall efficiency of the LED driver. Therefore, turns number N_{BIAS} should be minimized to ensure low-enough boost inductance and DCM operation at low line while maintaining relatively high efficiency. A turns number N_{BIAS} of 12 was selected for the final design. The dc resistance of winding N_{BIAS} is 20 mΩ while the turn-on resistance of bias control switch Q_2 is 1.8 mΩ (<<20 mΩ). At low line, switch Q_2 is turned off, and the entire load current I_O = 3.8 A flows through the bias winding resulting in a power loss of 0.29 W, i.e., a 0.3% decrease of efficiency. At high line, bias switch Q_2 is turned on and bias winding N_{BIAS} is essentially shorted since its dc resistance is much higher than the turn-on resistance of switch Q_2, resulting in a power loss of 22 mW at I_O = 3.8 A.

The measured line voltage and line current waveforms at full load are shown in Fig. 14. At nominal high line (230 Vrms), THD = 10.39%, PF = 0.9474, V_B = 327 V, and efficiency = 91%; while at nominal low line (120 Vrms), THD = 12.24%, PF = 0.9873, V_B = 193 V, and efficiency = 88% were obtained. Figure 15 shows that the measured line-current harmonics are below the IEC 61000-3-2 Class C limits with enough margin. The measured efficiency vs. output power is shown in Fig. 16.

Measurements with an actual LED load were also performed. Four LED strings each with 7 series-connected white LEDs (Philips Lumileds, LXHL-LW3C) were paralleled and directly driven by the proposed PFC flyback prototype with an output voltage of 24 V. The measured LED current and output voltage ripple are shown in Fig. 17. The peak-to-peak output voltage ripple is 30 mV, resulting in a low LED current ripple (1.6% of the average current). Therefore, the proposed PFC flyback circuit is suitable for directly driving LED strings, and no post-regulators are necessary, which is a significant advantage over the conventional PFC flyback circuit without an energy-storage capacitor at the primary side.

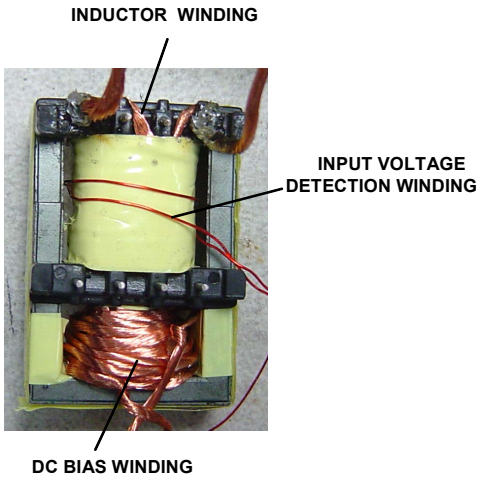


Fig. 12. Photograph of the variable boost inductor.

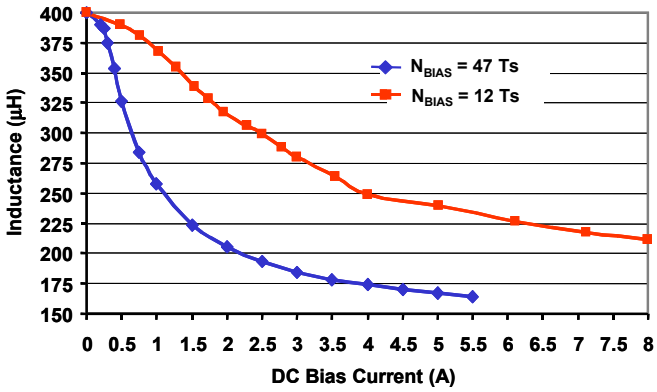
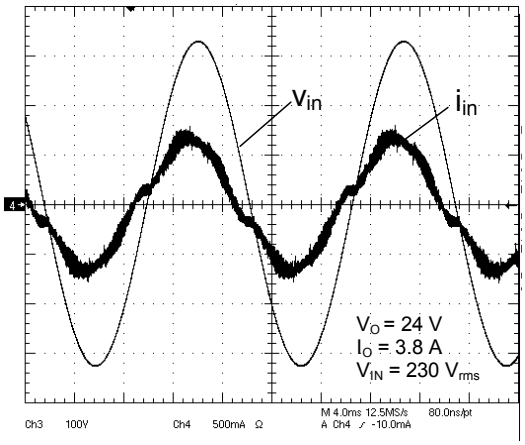
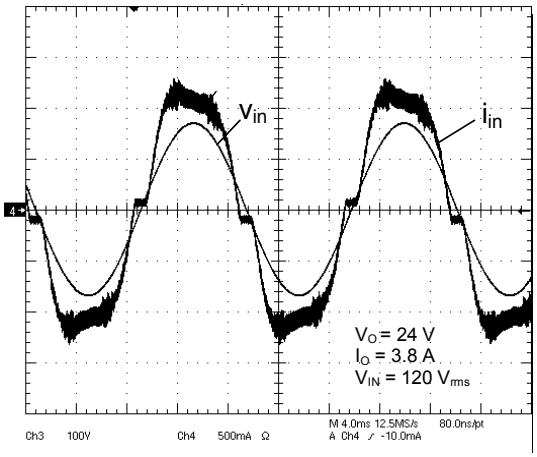


Fig. 13. Measured boost inductance vs. dc bias current.

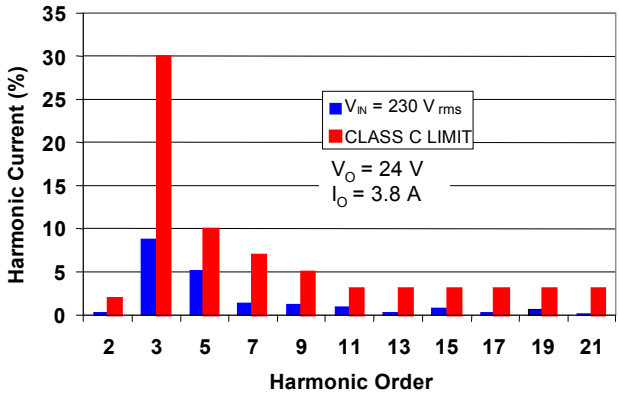


(a)

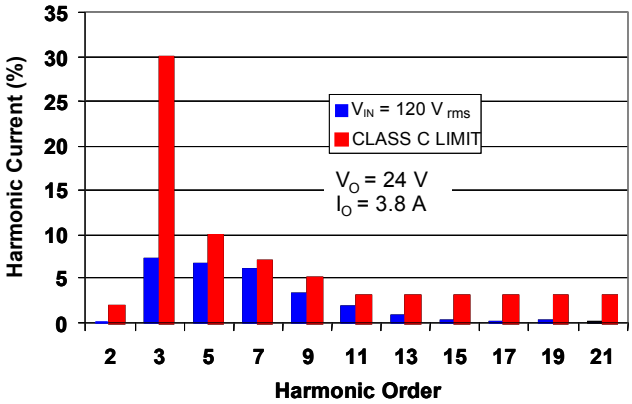


(b)

Fig. 14. Measured line current (500 mA/div.) and line voltage (100 V/div.) waveforms, (a) V_{IN} = 230 Vrms; (b) V_{IN} = 120 Vrms.



(a)



(b)

Fig. 15. Measured line current harmonics, (a) V_{IN} = 230 Vrms; (b) V_{IN} = 120 Vrms.

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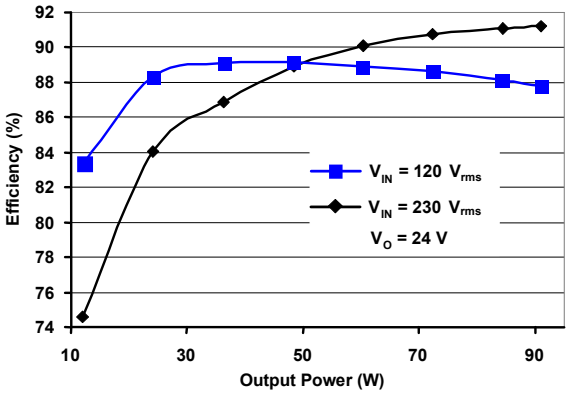

Fig. 16. Measured efficiency vs. output power.

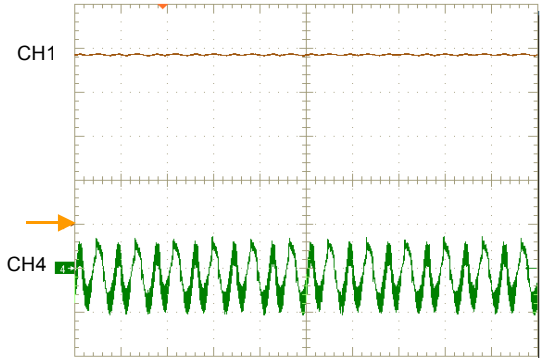

Fig. 17. Measured LED current and output voltage ripple at V_{IN} = 230 Vrms. CH1: LED current (1 A/div.); CH4: Output voltage ripple (20 mV/div.); Time scale: 10 ms/div.

IV. Summary

A single-stage PFC flyback with a variable boost inductance for HB LED applications for the universal input voltage is presented in this paper. Experimental results obtained on a 24-V/91-W prototype show that the proposed PFC converter achieves an efficiency of 88%, a power factor of 0.9873 and a THD of 12.24% at nominal low line (120 Vrms), and an efficiency of 91%, a power factor of 0.9474 and a THD of 10.39% at nominal high line (230 Vrms). Line-current harmonics satisfy the IEC 61000-3-2 Class C limits with enough margin.

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