Bridgeless Buck PFC Rectifier

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***Abstract* — A new bridgeless buck PFC rectifier that substantially improves efficiency at low line of the universal line range is introduced. By eliminating input bridge diodes, the proposed rectifier's efficiency is further improved. Moreover, the rectifier doubles its output voltage, which extends useable energy of the bulk capacitor after a drop-out of the line voltage.**

The operation and performance of the proposed circuit was verified on a 700-W, universal-line experimental prototype operating at 65 kHz. The measured efficiencies at 50% load from 115-V and 230-V line are both close to 96.4%. The efficiency difference between low line and high line is less than 0.5% at full load. A second-stage half-bridge converter was also included to show that the combined power stages easily meet Climate Saver Computing Initiative Gold Standard.

I. INTRODUCTION

Driven by economic reasons and environmental concerns, maintaining high efficiency across the entire load and input-voltage range of today's power supplies is in the forefront of customer's performance requirements. Specifically, meeting and exceeding U.S. Environmental Protection Agency's (EPA) Energy Star [1] and Climate Saver Computing Initiative (CSCI) [2] efficiency specifications have become a standard requirement for both multiple- and single-output off-line power supplies. Generally, the EPA and CSCI specifications define minimum efficiencies at 100%, 50%, and 20% of full load with a peak efficiency at 50% load. For example, for the highest-performance tier of single-output power supplies with a 12-V output, i.e., for the Platinum level power supplies, the required minimum efficiencies at 100%, 50%, and 20% load, measured at 230-V line, are 92%, 94%, and 91% respectively.

In universal-line (90-264-V) applications, maintaining a high efficiency across the entire line range poses a major challenge for ac/dc rectifiers that require power-factor correction (PFC). For decades, a bridge diode rectifier followed by a boost converter has been the most commonly used PFC circuit because of its simplicity and good power factor (PF) performance. However, a boost PFC front-end exhibits 1-3% lower efficiency at 100-V line compared to that at 230-V line. This drop of efficiency at low line can be attributed to an increased input current that produces higher losses in semiconductors and input EMI filter components.

Another drawback of the universal-line boost PFC front end is related to its relatively high output voltage, typically in the 380-400-V range. This high voltage not only has a detrimental effect on the switching losses of the boost converter, but also on the switching losses of the primary switches of the downstream dc/dc output stage and the size and efficiency of its isolation transformer. Because switching losses dominate at light loads, the light-load efficiency of a power supply exhibits a steep fall-off as the load current decreases.

At lower power levels, i.e., below 850 W, the drawbacks of the universal-line boost PFC front-end may partly be overcome by implementing the PFC front-end with a buck topology. As it has been demonstrated in [3], the universal-line buck PFC front end with an output voltage in the 80-V range maintains a high-efficiency across the entire line range. In addition, a lower input voltage to the dc/dc output stage has beneficial effects on its light-load performance because lower-voltage-rated semiconductor devices can be used for the dc/dc stage and because lower input voltage reduces the loss and size of the transformer.

The buck PFC converter operation in both DCM and CCM mode was described first in [4], whereas additional analysis and circuit refinements were described in [5]-[12]. Because the buck PFC converter does not shape the line current around the zero crossings of the line voltage, i.e., during the time intervals when the line voltage is lower than the output voltage, it exhibits increased total harmonic distortion (THD) and a lower power factor (PF) compared to its boost counterpart. As a result, in applications where IEC61000-3-2 and corresponding Japanese specifications (JIS-C-61000-3-2) need to be met, the buck converter PFC employment is limited to lower power levels.

In this paper, a bridgeless buck PFC rectifier that further improves the low-line (115-V) efficiency of the buck front end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. Because the proposed bridgeless buck rectifier also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of a conventional buck PFC rectifier. As a result, the proposed rectifier also shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage still significantly lower than that of the boost PFC counter part.

To verify the operation and performance of the proposed circuit, a 700-W, universal-line experimental prototype operating at 65 kHz was built. The measured efficiencies at 50% load over the input voltage range from 115-V to 230-V

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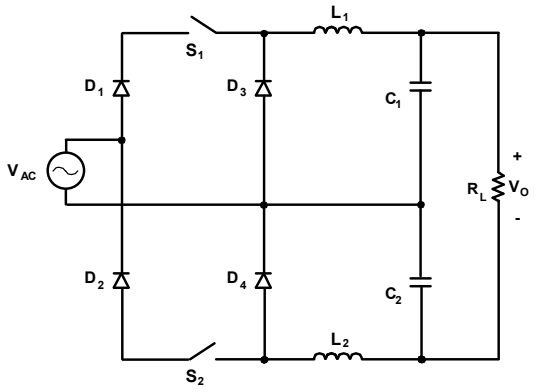

Fig. 1. Proposed bridgeless buck PFC rectifier.

are more than 96%. In addition, the full-load efficiency difference between low line and high line is less than 0.5%. Including a half bridge dc-dc converter 12-V output stage, the measured total efficiency is well above the CSCI Gold Level efficiency targets of 115-V and 230-V line.

II. Bridgeless Buck PFC Rectifier with Voltage Doubler Output

The proposed PFC rectifier, shown in Fig. 1, employs two back-to-back connected buck converters that operate in alternative halves of the line-voltage cycle. The buck converter illustrated in Fig. 2 only operates during positive half cycles of line voltage V_{AC} and consists of a unidirectional switch implemented by diode D_1 in series with switch S_1, freewheeling diode D_3, filter inductor L_1, and output capacitor C_1. During its operation, the voltage across capacitor C_1, which must be selected lower than the peak of line voltage, is regulated by pulse-width-modulation (PWM) of switch S_1. Similarly, the buck converter consisting of the unidirectional switch implemented by diode D_2 in series with switch S_2, freewheeling diode D_4, filter inductor L_2, and output capacitor C_2 operates only during negative half cycles of line voltage V_{AC}, as shown in Fig. 3. During its operation, the voltage across capacitor C_2 is regulated by PWM of switch S_2.

As seen from Figs. 2 and 3, the input current always flow through only one diode during the conduction of a switch, i.e., either D_1 or D_2. Efficiency is further improved by eliminating input bridge diodes in which two diodes carry the input current. An additional advantage of the proposed circuit is its inrush current control capability. Since the switches are located between the input and the output capacitors, switches S_1 and S_2 can actively control the input inrush current during start up.

Output voltage V_O of the PFC rectifier, which is the sum of the voltages across output capacitors C_1 and C_2, is given by

$$V_O = 2DV_{IN} \quad , \qquad (1)$$

where D is the duty cycle and V_{IN} is the instantaneous rectified ac input voltage. Because of the buck topology, the relationship shown in Eq. (1) is valid for input voltages V_{IN} greater than twice the output voltage, i.e., for V_{IN}>2Vo.

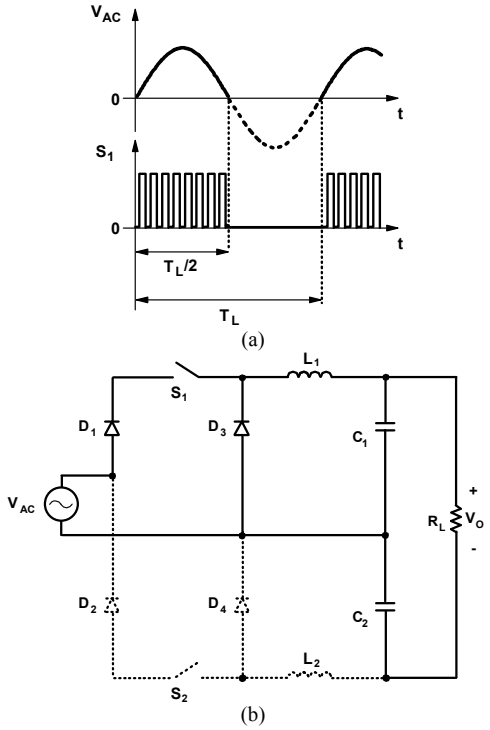

Fig. 2. Operation of the proposed bridgeless buck PFC rectifier during the period when the line voltage is positive.

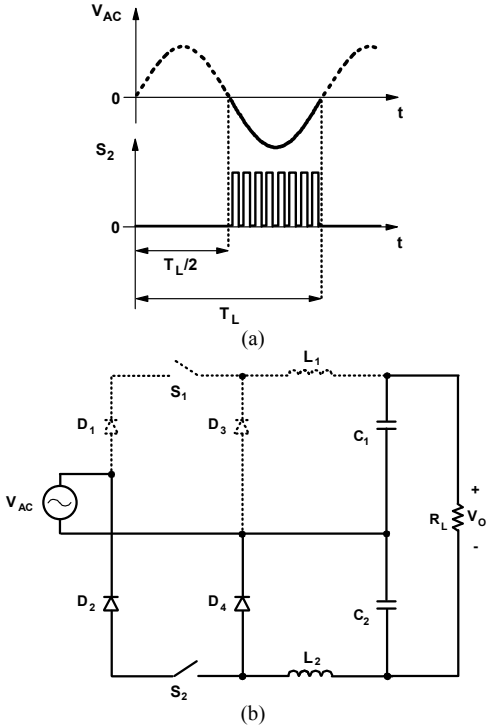

Fig. 3. Operation of the proposed bridgeless buck PFC rectifier during the period when the line voltage is negative.

When input voltage V_{IN} falls below $2V_O$, the converters do not deliver energy from the input to the output so the load current is maintained solely by the output capacitors.

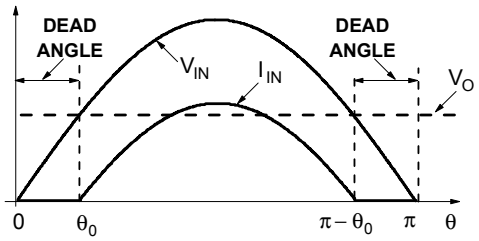

Fig. 4. Ideal input voltage and input current waveforms of a PFC buck rectifier.

Because the PFC buck rectifier does not shape the line current during the time intervals when the line voltage is lower than the output voltage, as shown in Fig. 4, there is a strong trade-off between THD and PF performance and output voltage selection. Namely, the output voltage should be maximized to minimize the size of the energy-storage capacitors for a given hold-up time. However, increasing the output voltage increases the THD and lowers the PF due to the increased dead angle as shown in Fig. 4, i.e., the time the buck converter does not operate during a half-line cycle. It was found that for power levels below 850 W, output voltage should be kept below 160 V to meet the IEC61000-3-2 harmonic requirements.

As demonstrated in [3], the clamped-current-mode control [13]-[15] is an effective, simple, and low-cost approach for controlling the buck PFC converter. The clamped-current-mode control can be easily extended to the bridgeless buck PFC front end since during each half-cycle only one buck converter in the bridgeless PFC operates at a time to regulate the voltage across its corresponding output capacitor.

As known from the general peak-current-mode theory, to ensure the stability of the current loop in the clamped-current-mode control circuit operating in CCM with a duty cycle over 50%, the slope of the compensation (external) ramp S_e should be at least 50% of the maximum down slope of the inductor current $S_{f,max}$, i.e.,

$$S_e = k_S \cdot S_{f,\max}, \quad k_S \geq 0.5 \cdot \tag{2}$$

Furthermore, as described in [3], optimum design cannot be achieved with a single value for k_S, i.e., minimize THD of input current and attain a high PF in the entire universal-input range. In universal-line applications, optimal design can only be achieved by a variable k_S that is increasing with input voltage. As found in [3], the optimal range for k_S is between 1 and 2 for nominal low line (115 V) and between 3 and 5 for nominal high line (230 V).

It also should be noted that the proposed bridgeless PFC rectifier's design criteria, as described in Eq. (2), guarantees the voltage balance of output capacitors C_1 and C_2. In fact, as long as constant k_S is higher than 0.5, the voltage balance of output capacitors C_1 and C_2 is automatically achieved.

Four topological variations of the proposed bridgeless buck PFC rectifier are shown in Fig. 5. As shown in Fig. 5(a), inductors L_1 and L_2 in the PFC rectifier in Fig. 1 can be replaced with a single inductor connected at the midpoint of capacitors C_1 and capacitor C_2 and the return of the input source. Also, the number of magnetic components can be reduced to a single component by coupling inductors L_1 and L_2 in the rectifier in Fig. 1, as shown in Fig. 5(b).

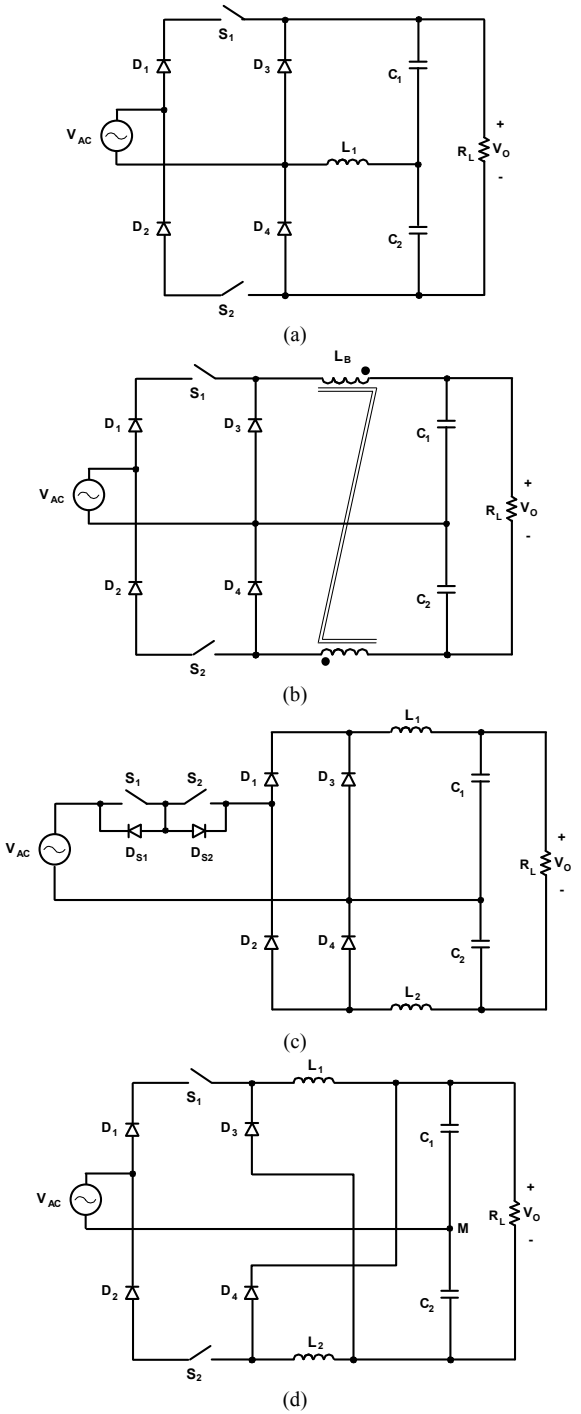

Fig. 5. Topology variations of the proposed bridgeless buck PFC rectifier. The rectifier with (a) a single inductor, (b) a coupled inductor, (c) a bi-directional switch, and (d) non-linear gain.

Another topological variation can be obtained by moving switches S_1 and S_2 in the PFC rectifier in Fig. 1 to the ac side,

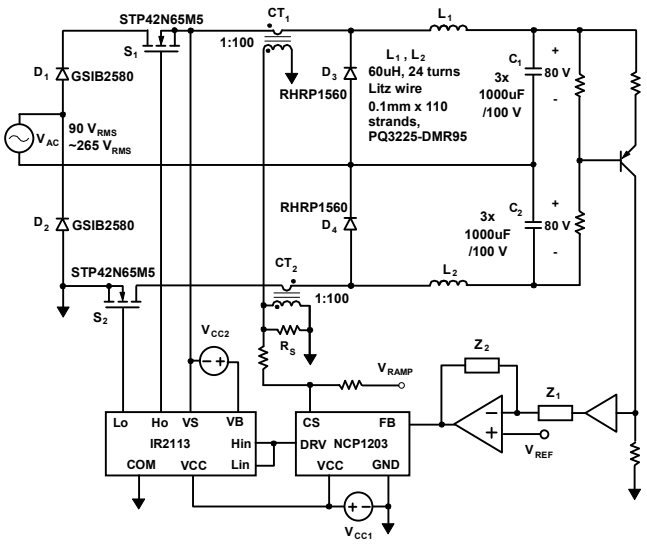

Fig. 6. Experimental prototype circuit of the proposed bridgeless buck PFC rectifier.

as shown in Fig. 5(c). In this implementation, a bi-directional switch is formed by the serial connection of switches S_1 and S_2 with their anti-parallel diodes D_{S1} and D_{S2}.

Yet another variation of the proposed bridgeless buck PFC rectifier is in Fig. 5(d). In this circuit, the anodes of freewheeling diodes D_3 and D_4 are connected directly to the negative and positive output rails, respectively, instead of to the midpoint of the output capacitors as in Fig. 1. It is interesting to note that the circuit in Fig. 5(d) exhibits a non-linear gain characteristic given by

$$V_O = \frac{2D}{1+(1-D)^2} V_{IN} \quad . \tag{3}$$

According to Eq. (3), if duty cycle D is near unity, i.e., when input voltage V_{IN} is close to half of output voltage V_O, the input-to-output gain is similar to that shown in Eq. (1). However, if duty cycle D is near zero, i.e., when input voltage V_{IN} is much greater than output voltage V_O, the input-to-output gain becomes

$$V_O = DV_{IN} \quad , \tag{4}$$

which is similar to the input-to-output gain of a conventional buck converter.

Finally, if reverse voltage blocking switches that allow unidirectional current flow are utilized for switches S_1 and S_2 in Fig. 1 and Figs. 5(a), 5(b), and 5(d), diodes D_1 and D_2 can be eliminated.

III. Experimental Results

The performance of the proposed rectifier in Fig. 1 was evaluated on a 65-kHz, 700-W prototype circuit that was designed to operate from a universal ac-line input (85 V_{RMS}-264 V_{RMS}) with a 160-V output.

Figure 6 shows the schematic diagram and component details of the experimental prototype circuit. Since the drain voltage of switches S_1 and S_2 are clamped to the voltage difference between the input voltage and output capacitor

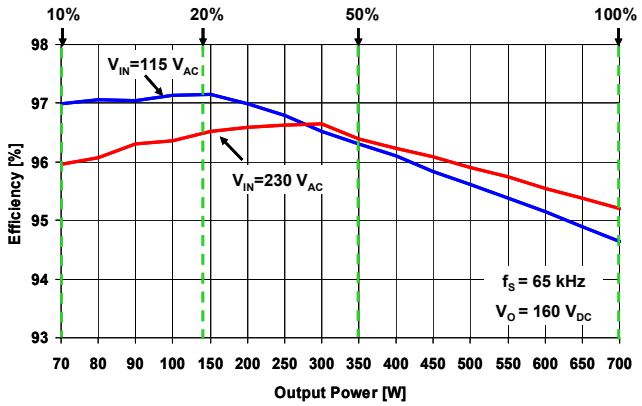

Fig. 7. Measured efficiency of the proposed bridgeless buck PFC rectifier.

voltage, the peak voltage stress on switch S_1 and S_2 can be as high as 380 V, which is the peak input voltage at the maximum line. The peak current stress on switch S, which occurs at full load and low line, is approximately 9 A. Therefore, a STP42N65M5 MOSFET (V_{DSS} = 650 V, R_{DS} = 0.079 Ω) from ST was used for each buck switch. Since output diodes D_3 and D_4 must block both the same peak voltage stress and conduct the same peak current as the switches, an RHRP1560 diode (V_{RRM} = 600 V, I_{FAVM} = 15 A) from Fairchild was used as boost diode D. It should be noted that the employed output diode is a low-cost conventional silicon diode since the reverse-recovery related loss in the proposed rectifier is much smaller than that of its boost counterpart, which frequently uses expensive silicon-carbide diodes. In fact, the voltage across the switches and diodes are much lower than those of a boost rectifier at low line operation, and the turn-on loss and the reverse-recovery-related losses are significantly lower.

To obtain the desired inductance of output inductor L_1 and L_2 of approximately 60 μH and also to achieve high efficiency at light-load, the output inductor was built using a pair of ferrite cores (PQ-3225, DMR95) and 24 turns of Litz wire (0.1mm, 110 strands). Litz wires were employed to reduce fringe effects near the gap area of the inductors.

Three aluminum capacitors (1000 μF, 100 VDC) were used for output capacitors C_1 and C_2 for their ability to meet the hold-up time requirement (20 mS at 50% load and 12 mS at full load).

As shown in Fig. 6, the bulk capacitor voltage that is the voltage across series connected capacitors C_1 and C_2 was regulated by a single controller (NCP1203 from On-Semi). Switches S_1 and S_2 were operated simultaneously by the same gate signal from the PWM controller. Although both switches were always gated, only one switch carried positive current and delivered power to the output, i.e., switch S_1 on which the positive input voltage was induced, as shown in Fig. 2. The other switch on which the negative input voltage is induced, *i.e.*, switch S_2 in Fig. 2, did not influence the operation since diode D_2, which is connected in series with switch S_2, blocked the current. It should be noted that the voltage across each capacitor C_1 or C_2 can be independently

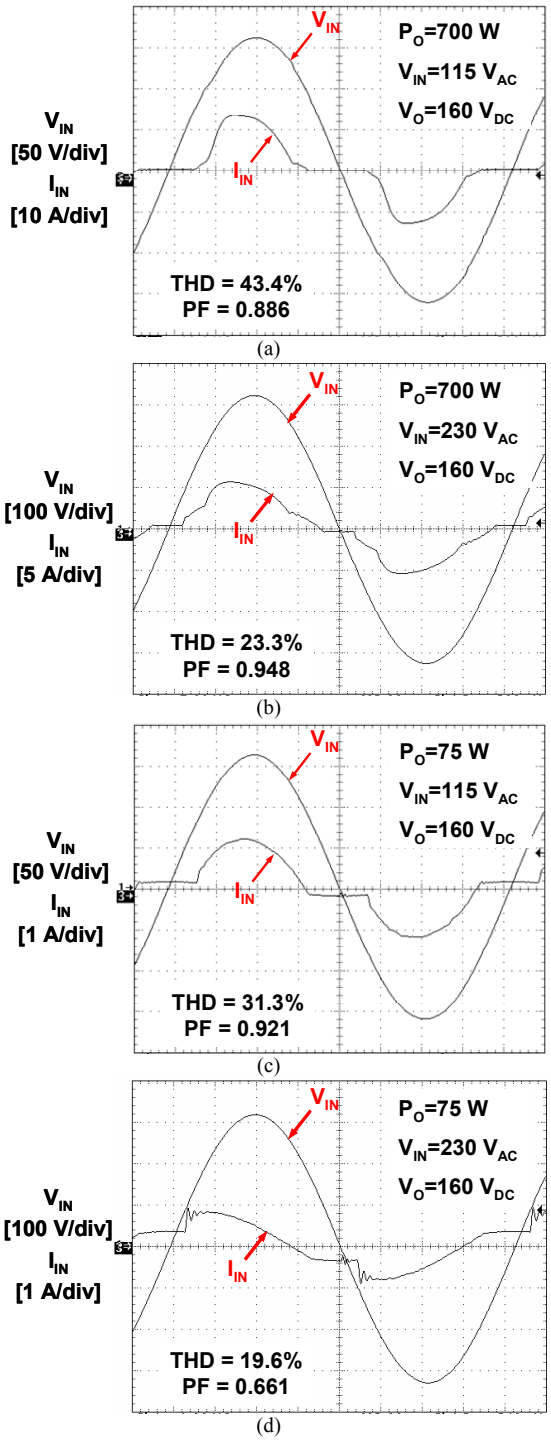

Fig. 8. Measured input voltage and current waveforms of the proposed bridgeless buck PFC rectifier when the output power is 700 W from (a) 115 V_{AC} and (b) 230 V_{AC} input voltage and 75 W from (c) 115 V_{AC} and (d) 230 V_{AC} input voltage.

regulated by two controllers as conceptually described in Figs. 2 and 3.

Figure 7 shows the measured efficiency of the proposed bridgeless buck PFC rectifier. It should be noted that the low-line efficiency is higher than the high-line efficiency over the load range below 40%. The efficiency difference between low line and high line is less than 0.5% over the load range above 50%, which is desirable for thermal optimization.

Figure 8 shows the measured input voltage and input current waveforms of the proposed PFC rectifier when the output power is 700 W and 75 W from low and high line. The

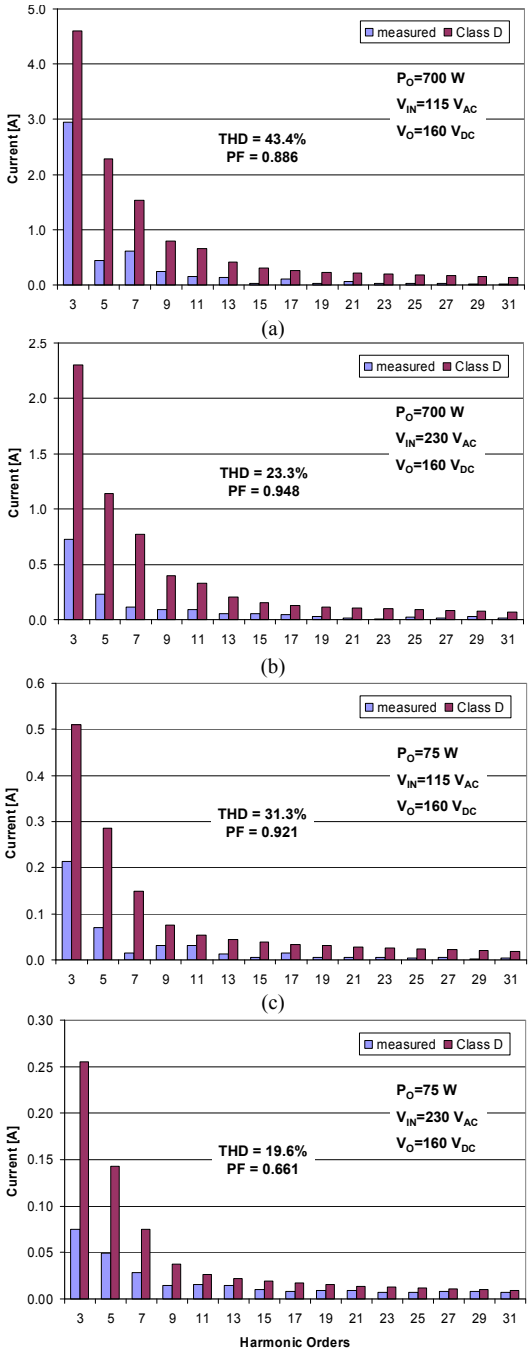

Fig. 9. Measured harmonic components of the input current at 700 W and 75 W output power. Class D requirements of IEC61000-3-2 are also plotted.

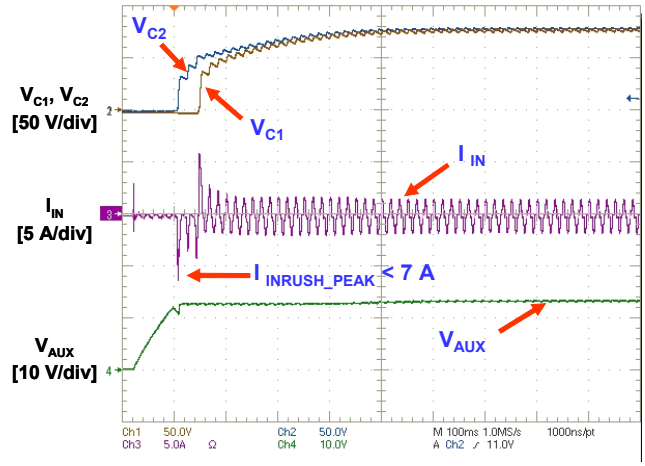

Fig. 10. Measured input current I_{IN}, output capacitor voltages V_{C1}-V_{C2} and control voltage V_{AUX} of the experimental prototype circuit during start up.

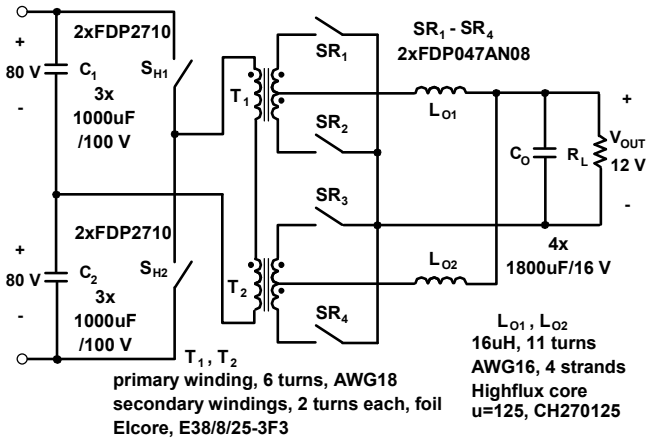

Fig. 11. Experimental half-bridge dc-dc 2nd stage converter. Input capacitors C_1 and C_2 are the same capacitors as the output capacitors of the front-end rectifier shown in Fig. 6.

measured total harmonic distortion (THD) and power factor (PF) of the rectifier are also shown in the figures. Measured harmonic components of the input current at 700 W and 75 W output power are shown in Fig. 9. Class D requirements of IEC61000-3-2 are also compared. All of the harmonic currents meet the related Class D requirements over the entire load and line ranges. Because the input current is actively controlled by switch S_1 and S_2 of the proposed buck rectifier, the inrush current during start up is well controlled as shown in Fig. 10.

To verify the performance of the entire power supply using the proposed front-end rectifier, a conventional half-bridge converter with synchronous rectifiers was implemented as the second stage converter that operates at 65-kHz switching frequency and delivers 12 V_{DC} output voltage. Although any isolated dc/dc converter topology can be used for the second stage, a half-bridge dc/dc converter is a more suitable topology as the second stage converter for the proposed

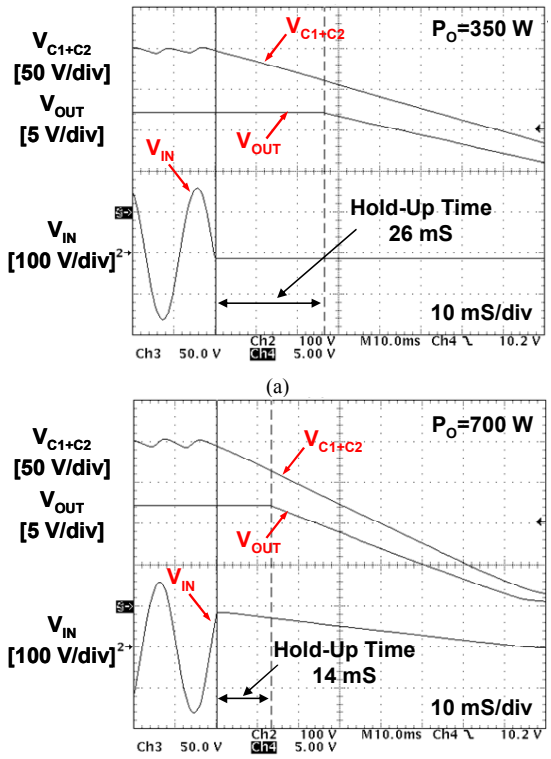

Fig. 12. Measured bulk capacitor voltage V_{C1+C2} that is the voltage across series connected capacitors C_1 and C_2, output voltage V_{OUT}, and ac input voltage V_{IN} at (a) 50% load and (b) 100% load during a hold-up time.

bridgeless buck PFC rectifier because capacitors C_1 and C_2, shown in Fig. 6, are used as two bulk capacitors of the half-bridge converter.

Figure 11 shows the experimental prototype circuit and the employed components. The second-stage half-bridge converter was implemented with two FDP2710 MOSFETs from Fairchild for each of bridge switches S_{H1} and S_{H2} and two parallel FDP047AN08AD MOSFETs from Fairchild for each of synchronous rectifier switches $S_{R1\text{-}R4}$. Transformer TR was built using a pair of ferrite cores (EI 38/8/25-3F3) with six turns of triple-insulated magnet wire (AWG# 18) for the primary winding and two turns of copper foil for each of the secondary windings. Output filter inductors L_{O1} and L_{O2} were built using a toroidal high flux core (CH270125) from Chang-Sung and 11 turns of magnet wire (4×AWG #16). Four low voltage aluminum capacitors (1800 µF, 16 VDC) were used for output capacitor C_O.

Figure 12 show the measured hold-up times at 50% load and full load conditions. Bulk capacitor voltage V_{C1+C2}, which is measured across the series connected capacitors C_1 and C_2 of the front-end rectifier, and output voltage V_{OUT} of the dc-dc second stage converter are shown in Fig. 12 together with input voltage V_{IN}. The measured hold-up times are approximately 26 mS and 14 mS at 50% load and full load conditions, respectively.

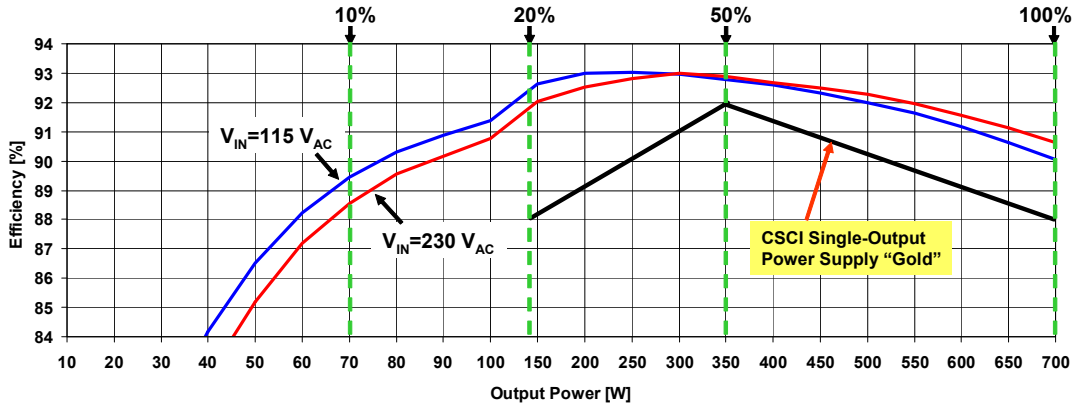

Fig. 13. Measured total efficiency of the proposed bridgeless buck PFC rectifier and half bridge 2nd stage converter. The power supply delivers 12 V dc output from 115 V and 230 V ac inputs. Efficiency requirements of Climate Saver Computing Initiative (CSCI) "gold" specification are also plotted.

The measured total efficiency of the proposed bridgeless buck PFC rectifier and half bridge 2nd stage converter is plotted in Fig. 13. The power supply that delivers 12 V dc output from 115 V and 230 V ac inputs meets the efficiency requirements of CSCI Gold specifications over the entire load and input ranges.

IV. Summary

In this paper, a new bridgeless buck PFC rectifier that substantially improves the efficiency at low line has been introduced. The proposed rectifier doubles the rectifier output voltage, which extends useable energy after a drop-out of the line voltage. Moreover, by eliminating input bridge diodes, efficiency is further improved.

The operation and performance of the proposed circuit was verified on a 700-W, universal-line experimental prototype operating at 65 kHz. The measured efficiencies at 50% load from 115-V and 230-V line are close to 96.4%. The efficiency difference between low line and high line is less than 0.5% at full load. Finally, a half bridge dc-dc converter is added as a second stage converter. The measured total efficiency is well above the CSCI specifications at both 115-V and 230-V line.

Acknowledgement

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